USB 2.0 PCB Guidelines for the ArcticLink® Solution Platform

QuickLogic® Application Note 93

Introduction

This document provides guidelines for component placement and PCB routing of the USB 2.0 portion of the QuickLogic ArcticLink solution platform. Follow the suggested guidelines to minimize signal integrity issues.

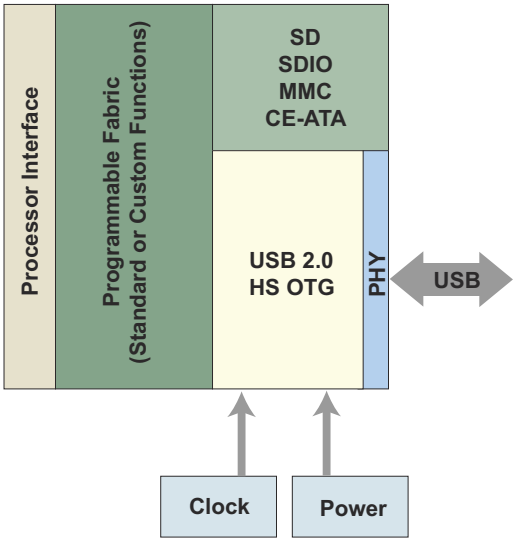
Overview

Figure 1 shows the QuickLogic ArcticLink solution platform including the programmable logic and ASSP parts. In addition to other components, the ASSP part contains a Hi-Speed USB 2.0 On-The-Go (OTG) subsystem that is capable of transferring data at speeds of 480 MHz.

To achieve the maximum speed with the highest signal quality, special attention must be taken during the PCB design around the area of the Hi-Speed USB 2.0 subsystem.

A clean analog power rail and a stable clock must be provided to the USB portion of the ArcticLink solution platform.

Figure 1: ArcticLink Solution Platform Block Diagram

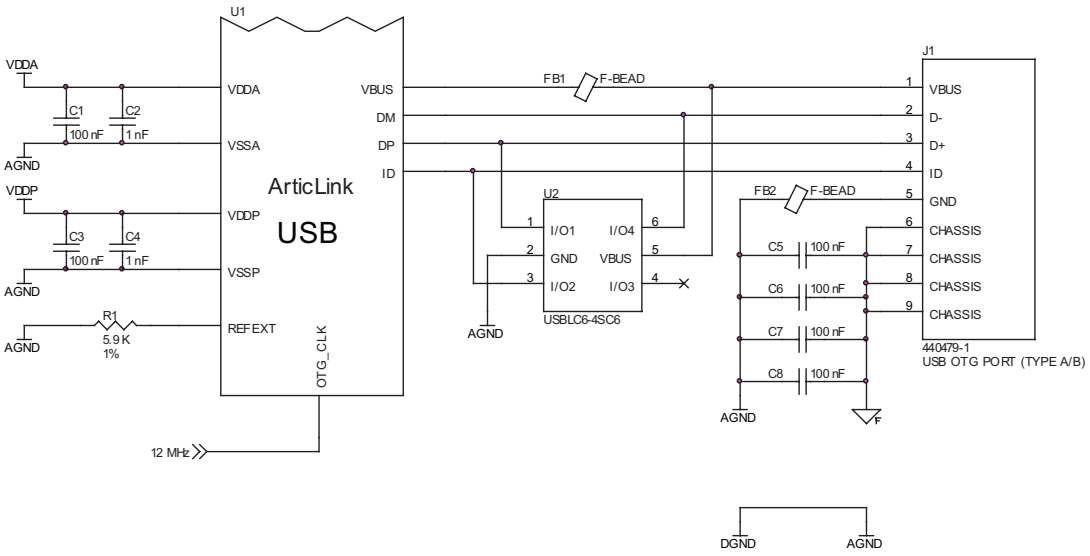


USB OTG Schematic

Figure 2 shows an electrical schematic of the USB OTG area and the component locations relative to each other:

- USB Subsystem
- Power Supply
- Reference Resistor
- Connector

Figure 2: USB OTG Schematic



USB Subsystem

The USB subsystem is comprised of the following components:

- U1- ArcticLink solution platform USB subsystem.
- U2– ESD protection device (e.g., USBLC6-4SC6).
- FB1 and FB2 Ferrite Beads – For cleaning the power line of the externally connected USB device.
- C5,C6,C7, and C8 – Capacitor 100 nF – Decoupling caps for the USB connector.

Power Supply

The power supply for the USB OTG area is comprised of the following components:

- C1 and C2 – Decoupling capacitor 100 nF (ceramic X7R).
- C3 and C4 – Decoupling capacitor (e.g., 1 nF, ceramic X7R) – Analog power rail decoupling caps for the ArcticLink solution platform. Two values are used to cover a wider spectral range.

Reference Resistor

The reference resistor for the USB OTG area is:

- R1 – Resistor 5.9 KΩ (to 1%) – OTG external reference resistor.

Connector

The connector for the USB OTG area is:

- J1 – USB OTG connector (Type A, mini-AB, etc.).

NOTE: Analog and digital ground must be connected on the board at one place only to level potentials and to avoid noise crossing.

Component Placement

The design of the PCB layout requires careful placement of the components as follows:

1. Place the USB OTG connector (J1) on the board.
2. Place the ArcticLink solution platform (U1) on the board no further than 2 to 3 inches from the USB OTG connector.
   - Leave space for ESD protection device (U2) and decoupling components (i.e., C1, C2, etc.).
   - For easier PCB routing, make sure to correctly rotate the ArcticLink solution platform.
   - The USB signals on the ArcticLink solution platform are placed at the edge of the package.
   - Place the ferrite beads (FB1 and FB2) close to USB OTG connector (J1).
3. Place the power-decoupling capacitors close to the ArcticLink solution platform (U1) or USB OTG connector (J1).
   - The lower value capacitors must be placed closer to the components.

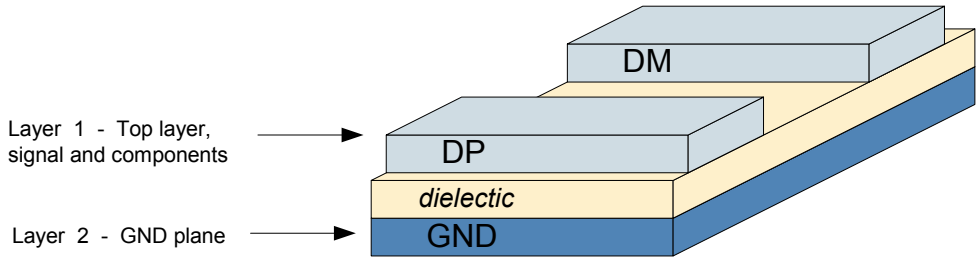
Stack-Up Recommendation

The ArcticLink solution platform can be routed in six layers. To route the ArcticLink solution platform in six layers, QuickLogic recommends the following stack-up:

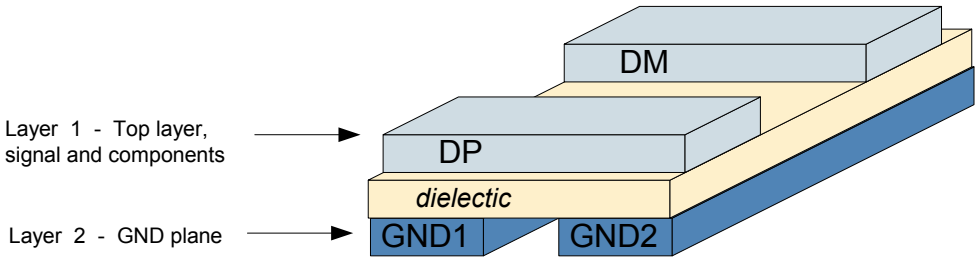
- Layer 1 – Top layer for components and high-speed signals
- Layer 2 – Power plane - GND
- Layer 3 – Inner signal layer routing
- Layer 4 – Inner signal layer routing
- Layer 5 – Power plane – VCC (split between different voltages)
- Layer 6 – Bottom layer for signal routing and passive components

If Hi-Speed USB signals are routed on the top layer, best results will be obtained if Layer 2 is a ground plane. Furthermore, there must be only one ground plane under the Hi-Speed USB signals in order to keep the Hi-Speed USB signals from crossing another ground plane. **Figure 3** shows examples of correct and incorrect power plane configurations on the layer below the top layer DP and DM signals.

Figure 3: Power Plane Configurations



Correct – Layout with USB signals over compact ground plane.



Incorrect – Layout with USB signals over **split** ground plane.

PCB Design Layout Suggestions

To minimize signal integrity issues, follow these PCB design layout suggestions:

1. Route the DP and the DM signals first. To gain the 90 Ω differential impedance, use a dielectric thickness of 4 mils, a trace spacing and a trace width of 7.5 mils to 8 mils.

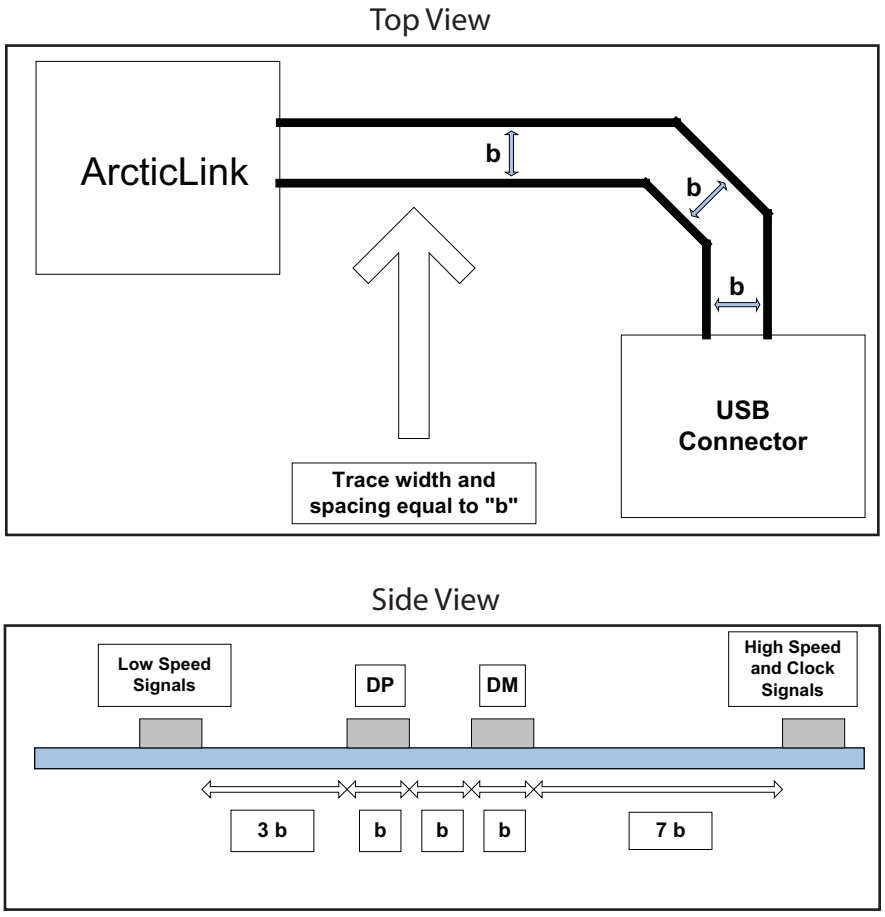
   NOTE: Differential impedance can be controlled by the trace width, the trace spacing and the dielectric thickness.

2. Route the DP and DM signals between the ArcticLink solution platform and the USB OTG connector, and through the ESD device on the top layer, keeping the length difference less than 150 mils. Try to route the signals less than 5 inches in length. Avoid the creation of stubs on these lines. If a stub is unavoidable in the design, stubs must not be longer than 200 mils.
3. Route the power decoupling with thick trace to connect to the power plane.
4. Route the clock lines. Create the clock lines as short as possible with a low capacitance line (5 mils thickness) on the top layer.

5. Route high-speed signals far from the clock line (a minimum of 50 mils distance) to reduce crystal jitter.
6. Route the ferrite beads with thick trace (15 mils is the minimum recommended).

Figure 4 shows an example of data USB line routing, where the DP and DM signals are parallel.

Figure 4: Recommended Trace Width and Spacing



Conclusion

This application note covers component placement PCB routing for the QuickLogic ArcticLink solution platform. Follow the recommendations in this application note to get the optimum signal quality on the USB bus and to minimize problems related to signal integrity. For more references or the latest version of this application note visit the QuickLogic website at www.quicklogic.com.

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Revision History

Revision	Date	Originator and Comments
A	April 2007	First release Vasuki Uttamalingam and Elaine Chan
B	November 2008	Kathleen Murchek Updated contact and trademark info. Added Notice of Disclaimer.
C	April 2008	Kathleen Murchek Updated trademark info..

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