Creating Power-Efficient Designs with the ArcticLink® Solution Platform

QuickLogic® Application Note 94

Introduction

The ArcticLink solution platform is comprised of a Hi-Speed USB OTG controller, 8 Kbyte Scratch Pad SRAM, and MMC/SD/SDIO/CE-ATA host controller. These peripheral devices are fixed function logic and constitute the Application Specific Standard Product (ASSP) portion of the device. These devices, when used in conjunction with the on-chip Programmable Fabric, provide a flexible and versatile platform for interfacing to a variety of mobile application processors.

The purpose of this document is to provide a description of the low power modes in the ASSP portion, and the Very Low Power (VLP) mode in the Fabric portion, of the ArcticLink solution platform. In addition, this document describes how each peripheral block should be configured when selected ASSP cores are suspended.

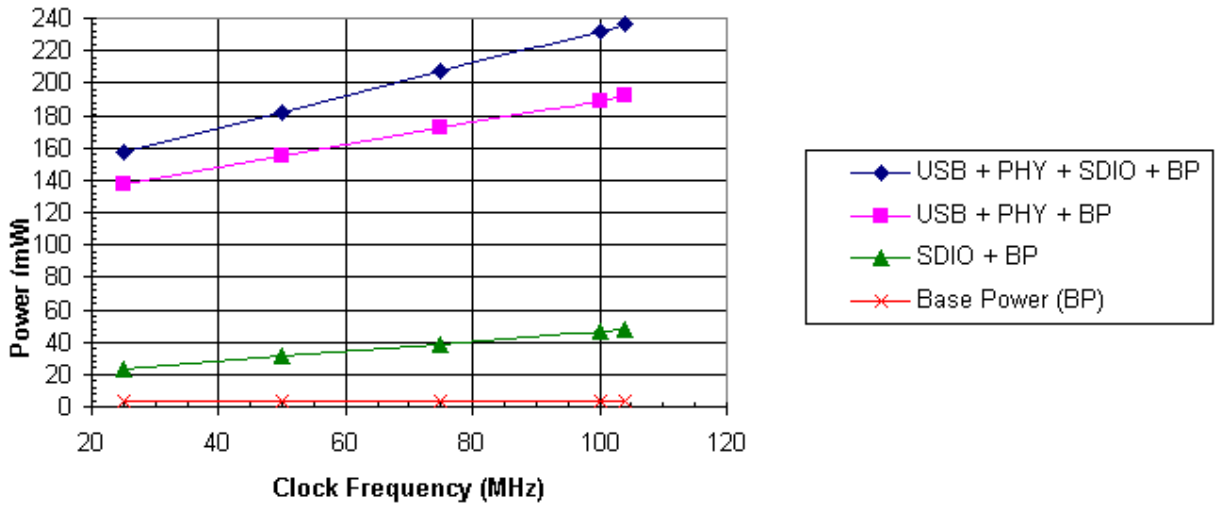
ASSP Side

On the ASSP side, the following fixed function logic components can be independently placed in a low power state when they are not in use:

- USB OTG core
- USB PHY
- MMC/SD/SDIO/CE-ATA core

The power for the various ASSP components as a function of clock frequency is illustrated in **Figure 1**.

Figure 1: ASSP Power vs. Clock Frequency



The data in the Power vs. Clock Frequency graph makes the following assumptions:

- ASSP core voltage is 1.8 V
- General Purpose I/O voltage is 3.3 V
- USB PHY is switching 50% of the time
- The system clock (sys_clk) and fabric clock (fb_clk) are operating at the same frequency
- The SDIO clock (sd_clk) frequency is equal to half the system clock (sys_clk) frequency
- Only the I/O used by the USB and SDIO cores are included in the power consumption calculations

The base power is the sum of the ASSP power when it is in a low power state and the I/O power when it is in an idle state. The individual ASSP components are placed in a low power state by disabling the appropriate clocks in each block. The SDIO and USB power consumption curves include the base power.

For more details on a general power equation for the ArcticLink solution platform see the section Power Versus Operating Frequency in the *ArcticLink Solution Platform Data Sheet* at http://www.quicklogic.com/images/ArcticLink_SP_DS.pdf.

Clock Gating

Disabling (i.e., gating-off) the appropriate clocks, using the following software-controlled ASSP digital logic control registers, suspends the power consuming components on the ASSP side.

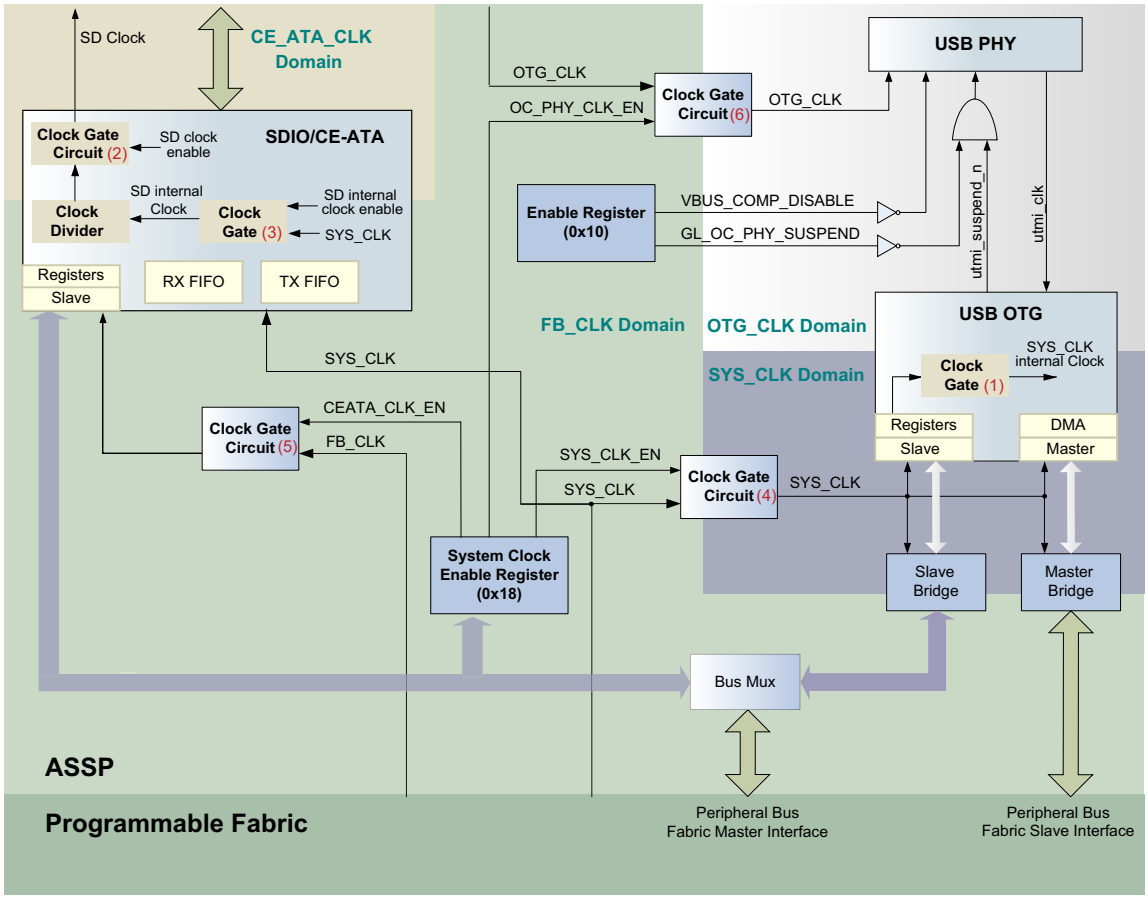
NOTE: The following references that are noted as (n) are in reference to **Figure 2** items (1) through (6).

The internal ASSP clocks that can be enabled and disabled are as follows:

- SYS_CLK "internal" Clock (1): The USB OTG core can be placed in a low power state by gating-off this clock. The *Gate hclk* – bit 1 in the Power and Clock Gating Control Register gates the local USB OTG clock.
- SD Clock (2): The *SD Clock Enable* – bit 2 in the Clock Control Register is used to gate the local SD clock, which is one of the clocks that is gated off in the process of disabling the SDIO/CE-ATA controller.
- SD "internal" Clock (3): The *Internal Clock Enable* – bit 0 in the Clock Control Register is used to gate the SD internal clock which is also one of the clocks that is gated off in the process of disabling the SDIO/CE-ATA controller.
- SYS_CLK (4:This clock can be disabled by writing to the *SYS_CK_EN* – bit 3 in the Global System Clock Enable Register.
- FB_CLK (5): This clock can be disabled by writing to the *CE-ATA_CK_EN* – bit 2 in the Global System Clock Enable Register.
- OTG_CLK (6): The *OC_PHY_CK_EN* – bit 4 in the Global System Clock Enable Register is used to turn off the external 12 MHz clock going to the on-chip USB PHY.

The on-chip clocks and their associated signals are illustrated in **Figure 2**.

Figure 2: Clock Gating Block Diagram



PHY Suspend

The on-chip PHY can be suspended when it is not in use. When the PHY is suspended, the analog and digital logic within the PHY are placed in a reset state. Consequently, the PHY is placed in a low power mode.

To minimize chip power, the on-chip PHY should be suspended if the USB OTG core is operating in ULPI mode or is not in use. The PHY must be disabled when the OTG core switches between ULPI and UTMI modes of operation.

The on-chip USB PHY can be suspended by configuring the appropriate global system registers and registers in the USB OTG core:

- USB Host Port Configuration and Status Register
- Power and Clock Gating Control Register
- Global System Clock Enable Register

To suspend and enable the on-chip USB PHY with no wake-up capabilities, *see* **Disabling and Enabling the On-Chip USB PHY** on page 15.

Fabric Side

The Fabric includes the following components:

- Clock networks
  - In the ArcticLink solution platform there are five global clock networks. Three of these networks are driven by the clock pads. Two of these clock networks are driven by the CCM outputs.
  - All global clock networks and any general routing network can drive ASSP clock signal inputs SYS_CLK and FB_CLK.
  - For more information about the clock networks see *Application Note 92—Clock Networks in the ArcticLink Solution Platform* at http://www.quicklogic.com/images/appnote92.pdf.
- Macros (logic cells, RAMs, etc.)
  - The global clock networks can drive all inputs of the logic cells and RAM cells.
- I/Os
  - There are two main types of I/Os, DDRIO and GPIO. The global clock networks can drive the clock, reset and enable of the INPUT and OUTPUT flip-flops of the I/O cells.
  - The I/Os have several features that support low power, battery operated systems. The I/Os operate at multiple voltages including 1.8 V, 2.5 V, and 3.3 V.
  - The GPIO has a data retention capability that enables the Fabric control signals to be retained when the Fabric goes into a low power mode. The GPIO control signals from the Fabric include the drive strength (P[3:0]), output enable (OEZ), pullup (PBE) and pulldown (PBD) signals.
  - The DDRIO can support multiple output slew and drive strengths that will enable the user to optimize power and performance. To further reduce power, the differential input receiver can be independently powered down when it is not in use.

Very Low Power (VLP) Mode

In VLP mode, the entire ArcticLink solution platform (Programmable Fabric and ASSP blocks) is placed in a very low power state.

Although the ArcticLink solution platform supports a combination of low power modes with the Programmable Fabric and ASSP blocks, VLP mode should only be entered when all ASSP blocks are in a low power state. The ASSP peripheral blocks must be configured *before* the Programmable Fabric is placed in low power mode.

The Programmable Fabric and ASSP peripheral blocks of the ArcticLink solution platform are placed in a low power state using two different control mechanisms:

- In the ASSP block, low power mode is controlled by enabling or disabling the clocks. Clock-gating structures are controlled by software using a set of registers within the ASSP.
- The Programmable Fabric's low power mode is controlled by an external VLP pin. It is assumed that the host processor controlling the ArcticLink solution platform also controls the external VLP signal to the Programmable Fabric's VLP pin.

NOTE: It takes ~250 µs for the Fabric to enter or exit VLP mode.

Fabric to ASSP Port Assertions in VLP Mode

The following Fabric to ASSP port assertions apply in VLP mode:

- All Fabric outputs are asserted low.
- All Fabric clocks are internally turned off and the CCM is in a reset state.
- When exiting VLP mode the CCM will restart and must re-lock.

Fabric Logic Cells, RAMs and I/O Cells in VLP Mode

The following Fabric logic cell, RAM and I/O cell assertions apply in VLP mode:

- All registers and RAM cells retain their data during VLP mode.
- The GPIO PAD output and output enable will retain their previous state, while the input signal to the Fabric will be pulled up to a weak "1".
- The DDRIO PAD outputs will be pulled down to a weak "0", while the differential and single ended input signals will be pulled low.

Peripheral Implications in VLP Mode

The ASSP is configured for VLP mode by disabling its internal clocks which are controlled by software using a set of registers within the ASSP. Instructions on how to do this are given in **Managing Power** on page 7.

- All peripheral blocks must be in a low power state before the Fabric is placed in VLP mode.
- Clock gating structures are used to control the clocks in the ASSP.

Low Power Considerations for Fabric Designs

This section contains the following:

- Clock Gating
- ASSP and RAM Block Chip Selection Management

Clock Gating

The Fabric has three clock input ports. From these clock input ports, the input clocks can drive any of the global clock networks in the Fabric. To conserve power, the input clocks can be dynamically disabled at the clock input port (i.e., clock pad).

The ASSP clocks, SYS_CLK and FB_CLK, can be driven by any of the five global clock networks in the Fabric. Hence, the ASSP clocks can be driven by the clock input ports. If the ASSP clocks are driven by the clock input ports, they can also be dynamically disabled at the clock input ports. The clocks are driven low when they are disabled.

Implications for gating the ASSP clocks at the clock input ports are as follows:

- SYS_CLK
  - The SYS_CLK clock input signal is used entirely within the ASSP and shares no timing relationship with the Programmable Fabric.
  - The SD Clock is derived from the SYS_CLK clock within the SDIO/CE-ATA core. The user must ensure that the SDIO/CE-ATA bus is idle before disabling the clock.

- The master and slave interfaces on the USB OTG core use the SYS_CLK. The user must ensure the master is in the idle state before disabling the SYS_CLK at the clock pad.
- QuickLogic recommends disabling the SYS_CLK within the ASSP, using the appropriate clock control registers, *before* disabling it at the clock pad.

- FB_CLK
  - FB_CLK is synchronous with Programmable Fabric timing.
  - The user must ensure that the Peripheral SRAM buses are in the idle state *before* disabling the FB_CLK at the clock pad.
  - QuickLogic recommends disabling the FB_CLK within the ASSP, using the appropriate clock control register, *before* disabling it at the clock pad.

NOTE: To maximize timing margins between the ASSP clock domain and the Fabric clock networks, QuickLogic recommends that the designer place the input clock on a general purpose I/O. This input can be routed to both the FB_CLK input at the ASSP-Fabric interface and the global clock network multiplexers in the center of the Fabric.

Clock Gating at Clock Pad

To reduce dynamic power consumption each clock pad input can be disabled by programmable control signals (i.e., CLKEN1 and CLKEN2) see **Figure 3**. **Table 1** shows the clock disable logic controlled by the two clock enable signals, CLKEN1 and CLKEN2.

Figure 3: Clock Gating at Clock Pad

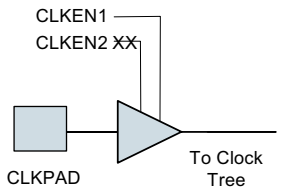


Table 1: Clock Settings

CLKEN1	CLKEN2[a]	Setting
X	0	Permanent disable
0	1	Dynamic disable
1	1	Dynamic enable

a. This signal is not accessible by the user's design, but can be controlled by the QuickLogic software tools.

If the clock input to the Fabric needs to be disabled to save dynamic power, then the Dynamic Clock Disable feature can be used. Once the control signals are disabled the clock will be driven low internally. Clocks can be disabled asynchronously without causing a glitch.

If only part of the Fabric's circuits need to have the clocks stopped, those circuits should use one clock tree, while other parts of the design can be clocked using another clock tree. The stopped clock can be re-enabled safely using the non-stopped logic without causing a glitch.

VLP Mode

In VLP mode, the Fabric clocks are automatically disabled at the clock pad.

ASSP and RAM Block Chip Selection Management

For energy efficient designs, the following chip selects should only be asserted in the clock cycle where there is a read or write access:

- FB_cs[2:0] — located on the Fabric Peripheral bus master interface
- Port1_CS and Port2_CS — located on the embedded RAM block (in fabric) interface

If these chip select ASSP inputs are asserted beyond the requirement of a read or write cycle, functionality will not be hindered; however, the device will draw additional current. Furthermore, avoid tying these chip selects to an asserted static level because power consumption will be increased.

Managing Power

Table 2 shows the combination of low power modes supported by the ArcticLink solution platform.

Table 2: System Power Mode

Mode	ASSP	Fabric	Supported
Power State 1	Active	Active	Yes – device fully operational
Power State 2	Low power	Active	Yes – selected ASSP blocks suspended
Power state 3	Low power	Low power	Yes – VLP Mode
N/A	Active	Low power	No

Examples for placing the Fabric and ASSP blocks in a low power state for Power State 1, Power State 2 and Power State 3 are provided in the following subsections.

Power State 1 – ArcticLink Solution Platform Fully Operational

The device is fully active in Power state 1, if it is not already active the device can be returned to a fully active power state from another suspended state.

Table 3: Power State 1

Mode	ASSP	Fabric	Supported
Power State 1	Active	Active	Yes – device fully operational

To exit from a low power state for an individually suspended block in the ASSP, *see* **Selected ASSP Low Power Mode** on page 8. To resume power for the entire ASSP portion of the device and exit from VLP mode, *see* **Exiting ASSP VLP Mode** on page 18.

Power State 2 – Selected ASSP Cores Suspended

If individual peripheral blocks in the ASSP are not in use, they can be placed in a low power state while still keeping the Programmable Fabric operational. This can be accomplished by disabling the appropriate clocks using the software controlled system registers.

Table 4: Power State 2

Mode	ASSP	Fabric	Supported
Power State 2	Low power	Active	Yes – selected ASSP blocks suspended

Selected ASSP Low Power Mode

The SDIO/CE-ATA, USB OTG and on-chip USB PHY peripheral blocks can be placed in a low power state using similar procedures as described in **Entering ASSP VLP Mode** on page 16.

The following subsections describe how to individually power off and power on the individual ASSP peripherals:

- **Suspending and Resuming the SDIO/CE-ATA Core** on page 8
- **Reduced Power Modes for the USB OTG Core** on page 9
- **Disabling and Enabling the On-Chip USB PHY** on page 15

Suspending and Resuming the SDIO/CE-ATA Core

The procedure to place the SDIO/CE-ATA core in a low power state is similar to one used to place the ASSP in VLP mode. The only difference is that the external FB clock is not disabled.

To enter low power mode:

1. Ensure that the CE-ATA/SDIO bus is idle.
2. Disable the SD clock and the internal core clocks in the CE-ATA/SDIO controller by writing to the following register:

Address	Register Name	Bit	Bit Name	State
0x0000102C	Clock Control Register	2	SD Clock Enable	0
		0	Internal Clock Enable	0

To exit low power mode:

1. Enable the SD clock and internal core clocks in the CE-ATA/SDIO controller by writing to the following register.

Address	Register Name	Bit	Bit Name	State
0x0000102C	Clock Control Register	2	SD Clock Enable	1
		0	Internal Clock Enable	1

Reduced Power Modes for the USB OTG Core

The USB OTG core can be placed in a reduced power state when it is operating as a host or device. Thus, the USB OTG core can be placed in a suspended or low power state, see **Table 5**.

Table 5 shows the low power states of USB OTG core.

Table 5: USB OTG Reduced Power Modes

USB OTG Mode	Enter Low Power State	Exit Low Power State
Host	Suspend	Resume
		Remote Wake-up
	Low Power	Enable
		SRP Resume
Device	Suspend	Resume
		Remote Wake-up
	Low Power	Enable
		SRP Resume

When the USB OTG core is in a low power or suspended state, the internal SYS_CLK clock is disabled. The on-chip USB PHY is also powered off in the low power state; consequently less power is consumed in this state.

In the low power state, the USB OTG core cannot use the resume or remote wake-up functions since the USB PHY is powered off. In this state, the USB OTG core can resume normal operation by the application software or by using the Session Request Protocol (SRP).

When the USB OTG core is suspended, it can continue with normal operation using the resume or remote wake-up functions. The resume function is initiated by the USB OTG application software while the remote wake-up function is initiated by the USB device.

The details of each configuration are described in the following sections:

- **USB Host Mode – Entering Suspend State** on page 10
- **USB Host Mode – Exiting Suspend State with Resume** on page 10
- **USB Host Mode – Exiting Suspend State with Remote Wake-up** on page 11
- **USB Host Mode – Entering Low Power State** on page 11
- **USB Host Mode – Exiting Low Power State** on page 12
- **USB Host Mode – Exiting Low Power State with SRP** on page 12
- **USB Device Mode – Entering Suspend State** on page 13
- **USB Device Mode – Exiting Suspend State with Resume** on page 13
- **USB Device Mode – Exiting Suspend State with Remote Wake-up** on page 14
- **USB Device Mode – Entering Low Power State** on page 14
- **USB Device Mode – Exiting Low Power State** on page 14
- **USB Device Mode – Exiting Low Power State with SRP** on page 15

USB Host Mode – Entering Suspend State

To enter the suspended state:

1. Ensure that the USB bus is idle.
2. Set the USB port to suspend mode by writing to the following register:

Address	Register Name	Bit	Bit Name	State
0x00040440	USB Host Port Configuration and Status	7	Port Suspend	1

3. Suspend the on-chip PHY by writing to the following register.:

Address	Register Name	Bit	Bit Name	State
0x00000010	Global Enable Register	18	GL_OC_PHY_SUSPEND	1

4. Turn off the OTG_CLK going to the on-chip USB PHY by writing to the following register:

Address	Register Name	Bit	Bit Name	State
0x00000018	Global System Clock Enable Register	4	OC_PHY_CK_EN	0

The USB PHY is now in a low power state. The PHY output clock (utmi_clk) to the USB OTG core is disabled in this state.

5. Stop the SYS_CLK "internal" clock within the USB OTG core by writing to the following register:

Address	Register Name	Bit	Bit Name	State
0x00040E00	Power and Clock Gating Control	1	Gate hclk	1

The USB host is in a suspended state.

USB Host Mode – Exiting Suspend State with Resume

When the USB Host is in a suspended state, the application can resume operation using the following procedures:

1. Enable the SYS_CLK "internal" clock within the USB OTG core and on-chip PHY by writing to the following register bits:

Address	Register Name	Bit	Bit Name	State
0x00040E00	Power and Clock Gating Control	1	Gate hclk	0
0x00000010	Global Enable Register	18	GL_OC_PHY_SUSPEND	0

2. Enable the OTG_CLK by writing to the following registers:

Address	Register Name	Bit	Bit Name	State
0x00000018	Global System Clock Enable Register	4	OC_PHY_CK_EN	1

3. Set the Port Resume bit in the host Port Control and Status register:

Address	Register Name	Bit	Bit Name	State
0x00040440	USB Host Port Configuration and Status	6	Port Resume	1

The USB OTG core starts driving Resume signaling.

4. Wait at least 20 ms before clearing the Port Resume bit:

Address	Register Name	Bit	Bit Name	State
0x00040440	USB Host Port Configuration and Status	6	Port Resume	0

The core is in normal operating mode.

USB Host Mode – Exiting Suspend State with Remote Wake-up

When the USB Host is in a suspended state, an external device can remotely wake-up the core. To wake-up the USB Host:

1. The USB device sends the Remote Wake-up signaling to the host. In response, the USB Host generates a Remote Wake-up Detected interrupt.
2. Enable the SYS_CLK clock within the USB OTG core and on-chip PHY by writing to the following register bits:

Address	Register Name	Bit	Bit Name	State
0x00040E00	Power and Clock Gating Control	1	Gate hclk	0
0x00000010	Global Enable Register	18	GL_OC_PHY_SUSPEND	0

After these bits are cleared, the USB OTG core automatically sets the Port Resume bit.

3. Enable the OTG_CLK clock by writing to the following register:

Address	Register Name	Bit	Bit Name	State
0x00000018	Global System Clock Enable Register	4	OC_PHY_CK_EN	1

4. Wait at least 20 ms before clearing the Port Resume bit:

Address	Register Name	Bit	Bit Name	State
0x00040440	USB Host Port Configuration and Status	6	Port Resume	0

The core is in normal operating mode.

USB Host Mode – Entering Low Power State

When the USB Host is in a low power state, the session is ended and it cannot use the remote wake-up or resume operations. To enter low power state:

1. Ensure that the USB bus is idle.
2. Set the USB port to suspend mode by writing to the following register:

Address	Register Name	Bit	Bit Name	State
0x00040440	USB Host Port Configuration and Status	7	Port Suspend	1

3. Clear the Port Power bit. In response, the USB Host core turns off the VBUS.

Address	Register Name	Bit	Bit Name	State
0x00040440	USB Host Port Configuration and Status	12	Port Power	0

4. Set the Stop PHY Clock bit. When this bit is set the USB host asserts the utmi_suspend_n signal, see **Figure 2** on page 3, low to the on-chip PHY.

Address	Register Name	Bit	Bit Name	State
0x00040E00	Power and Clock Gating Control	0	Stop PHY Clock	1

5. Turn off the OTG_CLK going to the on-chip USB PHY writing to the following register.

Address	Register Name	Bit	Bit Name	State
0x00000018	Global System Clock Enable Register	4	OC_PHY_CK_EN	0

The USB PHY is now in a low power state. The PHY output clock (utmi_clk) to the USB OTG core is disabled in this state.

6. Stop the internal SYS_CLK clock within the USB OTG core by writing to the following register:

Address	Register Name	Bit	Bit Name	State
0x00040E00	Power and Clock Gating Control	1	Gate hclk	1

The USB host is in a low power state.

USB Host Mode – Exiting Low Power State

To exit the low power state:

1. Enable the SYS_CLK clock within the USB OTG core and on-chip PHY by writing to the following register:

Address	Register Name	Bit	Bit Name	State
0x00040E00	Power and Clock Gating Control	0	Stop PHY Clock	0
		1	Gate hclk	0

2. Enable the OTG_CLK by writing to the following register.

Address	Register Name	Bit	Bit Name	State
0x00000018	Global System Clock Enable Register	4	OC_PHY_CK_EN	1

3. Set the Port Power bit in the host Port Control and Status register to turn on VBUS:

Address	Register Name	Bit	Bit Name	State
0x00040440	USB Host Port Configuration and Status	12	Port Power	1

The USB Host detects device connection and drives a USB reset. The core is in normal operating mode.

USB Host Mode – Exiting Low Power State with SRP

The SRP (data line pulsing) from the device is detected. The USB Host de-asserts the utmi_suspend_n signal, see **Figure 2** on page 3, to the on-chip PHY. An SRP Request Detected interrupt is generated. To exit the low power state:

1. Enable the SYS_CLK clock within the USB OTG core and on-chip PHY by writing to the following register:

Address	Register Name	Bit	Bit Name	State
0x00040E00	Power and Clock Gating Control	0	Stop PHY Clock	0
		1	Gate hclk	0

2. Enable the OTG_CLK clock by writing to the following register:

Address	Register Name	Bit	Bit Name	State
0x00000018	Global System Clock Enable Register	4	OC_PHY_CK_EN	1

3. Set the Port Power bit in the host Port Control and Status register to turn on VBUS:

Address	Register Name	Bit	Bit Name	State
0x00040440	USB Host Port Configuration and Status	12	Port Power	1

The USB Host detects device connection and drives a USB reset.

4. The core is in normal operating mode.

USB Device Mode – Entering Suspend State

The USB OTG core detects a USB suspend from the host and generates a Suspend Detected Interrupt. To enter the suspend state:

1. Set the Stop PHY Clock bit. When this bit is set the USB OTG core asserts the utmi_suspend_n signal, see **Figure 2** on page 3, low to the on-chip PHY.

Stop the SYS_CLK "internal" Clock within the USB OTG core by writing to the following register bits:

Address	Register Name	Bit	Bit Name	State
0x00040E00	Power and Clock Gating Control	0	Stop PHY Clock	1
		1	Gate hclk	1

2. Turn off the OTG_CLK clock by writing to the following register:

Address	Register Name	Bit	Bit Name	State
0x00000018	Global System Clock Enable Register	4	OC_PHY_CK_EN	0

The on-chip USB PHY is now in a low power state. The PHY output clock (utmi_clk, see **Figure 2** on page 3) to the USB OTG core is disabled in this state. The USB OTG core is in a suspended state.

USB Device Mode – Exiting Suspend State with Resume

When the USB OTG core is in a suspended state, the host can resume operation using the following procedures:

The host transmits the Resume signaling to the USB OTG core. When detected, the core de-asserts the utmi_suspend_n signal, see **Figure 2** on page 3, to the on-chip PHY and generates a Resume Detected interrupt.

1. Enable the SYS_CLK "internal" clock within the USB OTG core and on-chip PHY by writing to the following register bits:

Address	Register Name	Bit	Bit Name	State
0x00040E00	Power and Clock Gating Control	0	Stop PHY Clock	0
		1	Gate hclk	0

2. Enable the OTG_CLK clock by writing to the following register:

Address	Register Name	Bit	Bit Name	State
0x00000018	Global System Clock Enable Register	4	OC_PHY_CK_EN	1

The host finishes the Resume signaling. The USB OTG core is in normal operating mode.

USB Device Mode – Exiting Suspend State with Remote Wake-up

When the USB OTG core is in a suspended state, the external USB host can wake-up the core. To wake-up the core:

1. Enable the SYS_CLK "internal" clock within the USB OTG core and on-chip PHY by writing to the following register:

Address	Register Name	Bit	Bit Name	State
0x00040E00	Power and Clock Gating Control	0	Stop PHY Clock	0
		1	Gate hclk	0

2. Enable the OTG_CLK clock by writing to the following register:

Address	Register Name	Bit	Bit Name	State
0x00000018	Global System Clock Enable Register	4	OC_PHY_CK_EN	1

3. Set the Remote Wake-up bit in the Device Control register. When this bit is set, the USB OTG core starts driving the Remote Wake-up signaling.

Address	Register Name	Bit	Bit Name	State
0x00040804	Device Control Register	0	Remote Wake-up Signal	1

The host drives Resume signaling. The USB OTG core is in normal operating mode.

USB Device Mode – Entering Low Power State

The USB OTG core detects a USB suspend and generates a Suspend Detected interrupt. In response to the interrupt, the host turns off VBUS. To enter low power state:

1. Set the Stop PHY Clock bit. When this bit is set the USB OTG core asserts the utmi_suspend_n signal, see **Figure 2** on page 3, low to the on-chip PHY.
2. Stop the SYS_CLK "internal" clock within the USB OTG core by writing to the following register bits:

Address	Register Name	Bit	Bit Name	State
0x00040E00	Power and Clock Gating Control	0	Stop PHY Clock	1
		1	Gate hclk	1

The USB PHY is now in a low power state. The PHY output clock (utmi_clk, see **Figure 2** on page 3) to the USB OTG core is disabled in this state.

The USB host is in a low power state.

USB Device Mode – Exiting Low Power State

When a new session is detected (bsessvld is high), the USB OTG core deasserts the utmi_suspend_n signal, see **Figure 2** on page 3, to the on-chip PHY. A New Session Detected interrupt is generated.

To exit the low power state:

1. Enable the SYS_CLK "internal" clock within the USB OTG core and on-chip PHY by writing to the following register:

Address	Register Name	Bit	Bit Name	State
0x00040E00	Power and Clock Gating Control	0	Stop PHY Clock	0
		1	Gate hclk	0

The USB OTG core detects USB reset. The core is in normal operating mode.

USB Device Mode – Exiting Low Power State with SRP

1. Enable the SYS_CLK "internal" clock within the USB OTG core and on-chip PHY by writing to the following register:

Address	Register Name	Bit	Bit Name	State
0x00040E00	Power and Clock Gating Control	0	Stop PHY Clock	0
		1	Gate hclk	0

2. Set the SRP Request bit. In response, the USB OTG core drives the data line and VBUS pulsing.

   The host turns on VBUS, detects device connection and drives a USB reset. The core is in normal operating mode.

Disabling and Enabling the On-Chip USB PHY

If the on-chip USB PHY is not used, it can be disabled and placed in a low power state. This may be necessary when the USB OTG core utilizes the ULPI interface with an external PHY.

To place the on-chip USB PHY into a low power state:

1. Set the USB PHY in the suspended state by writing to the following register:

Address	Register Name	Bit	Bit Name	State
0x00000010	Global Enable Register	18	GL_PHY_SUSPEND	1

2. Turn off the analog blocks (i.e., VBUS Comparator) in the on-chip USB PHY by writing to the following register:

Address	Register Name	Bit	Bit Name	State
0x00000010	Global Enable Register	17	VBUS_COMP_DISABLE	1

3. Turn off the OTG_CLK clock going to the on-chip USB PHY by writing to the following register:

Address	Register Name	Bit	Bit Name	State
0x00000018	Global System Clock Enable Register	4	OC_PHY_CK_EN	0

   The USB PHY is now in a low power state, and the USB PHY output clock (utmi_clk) to the USB OTG core is disabled.

   At this point, the USB OTG core can switch operation to the ULPI interface.

To bring the on-chip USB PHY out of a low power state:

1. Turn on the OTG_CLK clock going to the on-chip USB PHY by writing to the following register:

Address	Register Name	Bit	Bit Name	State
0x00000018	Global System Clock Enable Register	4	OC_PHY_CK_EN	1

2. Turn on the analog blocks (i.e., VBUS Comparator) in the on-chip USB PHY by writing to the following register:

Address	Register Name	Bit	Bit Name	State
0x00000010	Global Enable Register	17	VBUS_COMP_DISABLE	0

3. Bring the USB PHY out of the suspended state by writing to the following register.

Address	Register Name	Bit	Bit Name	State
0x00000010	Global Enable Register	18	GL_PHY_SUSPEND	0

The USB PHY output clock (utmi_clk) to the USB OTG core is enabled in this state.

At this point, the USB OTG core can switch operation to the internal PHY interface.

Power State 3 – ArcticLink Solution Platform in VLP mode

In VLP mode, the ArcticLink solution platform is placed in a low power state, see **Table 6**.

Table 6: Power State 3

Mode	ASSP	Fabric	Supported
Power State 3	Low power	Low power	Yes – VLP Mode

The Programmable Fabric and ASSP peripheral blocks are placed in low power state using different mechanisms.

The Programmable Fabric uses the VLP input signal to control the internal power consumption. By contrast, the ASSP is placed in a low power state by gating off the clocks, see **Entering ASSP VLP Mode** on page 16. These clock-gating structures are controlled by software using a set of registers within the ASSP.

NOTE: The ASSP must be configured before the Programmable Fabric is placed in a low power state.

Entering ASSP VLP Mode

Complete the following steps to enter VLP mode for the ASSP.

1. Stop the ASSP peripherals as follows:
   - **Suspending the SDIO/CE-ATA Core** on page 16
   - **Stopping the OTG Core and USB PHY** on page 17
2. Set the external VLP signal to 0. This will put the Fabric in a low power state. In this state, all Fabric to ASSP signals are asserted low, and all Fabric clock pad signals are gated off.

Suspending the SDIO/CE-ATA Core

To minimize power usage during VLP mode, the CE-ATA/SDIO clock should be disabled. The external host processor must perform the following sequence of events on the CE-ATA core to enter VLP mode:

1. Ensure that the CE-ATA/SDIO bus is idle.
2. Disable the SD clock and the internal core clocks in the CE-ATA/SDIO controller by writing to the following register:

Address	Register Name	Bit	Bit Name	State
0x0000102C	Clock Control Register	2	SD Clock Enable	0
		0	Internal Clock Enable	0

3. The CE-ATA/SDIO core will be in a low power state. At this time, the external system clock (FB_CLK) can be disabled by writing to the Global System Clock Enable Register:

Address	Register Name	Bit	Bit Name	State
0x00000018	Global System Clock Enable Register	2	CE_ATA_CK_EN	0

Stopping the OTG Core and USB PHY

In VLP mode, the on-chip USB PHY and USB OTG core must be placed in a low power state.

In this state, the USB OTG core cannot use the resume or remote wake-up operations.

The external host processor must perform the following sequence of events to place the USB PHY and USB OTG core in a low power state:

1. Ensure that the USB bus is idle.
2. Set the USB port to suspend mode by writing to the following register:

Address	Register Name	Bit	Bit Name	State
0x00040440	USB Host Port Configuration and Status	12	Port Power	0
		7	Port Suspend	1
		2	Port Enable	0

3. Configure the USB OTG core to place the on-chip USB PHY into the suspended state (i.e., assert the utmi_suspend_n signal low, see **Figure 2** on page 3).

Address	Register Name	Bit	Bit Name	State
0x00040E00	Power and Clock Gating Control	0	Stop PHY Clock	1

Alternatively, the on-chip USB PHY can be suspended independently of the USB OTG core by asserting the GL_OC_PHY_SUSPEND bit.

Address	Register Name	Bit	Bit Name	State
0x00000010	Global Enable Register	18	GL_OC_PHY_SUSPEND	1

4. Turn off the analog blocks (i.e., VBUS Comparator) in the on-chip USB PHY by writing to the following register:

Address	Register Name	Bit	Bit Name	State
0x00000010	Global Enable Register	17	VBUS_COMP_DISABLE	1

5. Turn off the OTG_CLK clock going to the on-chip USB PHY by writing to the following register:

Address	Register Name	Bit	Bit Name	State
0x00000018	Global System Clock Enable Register	4	OC_PHY_CK_EN	0

The USB PHY is now in a low power state.

The PHY output clock (utmi_clk, see **Figure 2** on page 3) to the USB OTG core is disabled in this state. This places the USB OTG core in a low power state.

6. Stop the SYS_CLK "internal" clock within the USB OTG core by writing to the following register:

Address	Register Name	Bit	Bit Name	State
0x00040E00	Power and Clock Gating Control	1	Gate hclk	1

7. The USB OTG core will be in the suspended state. At this time, the external SYS_CLK clock (outside the core) can be gated off, by writing to the Global System Clock Enable Register.

Address	Register Name	Bit	Bit Name	State
0x00000018	Global System Clock Enable Register	3	SYS_CK_EN	0

Setting this bit to 0 turns off the SYS_CLK clock to all peripheral blocks in the ASSP.

Exiting ASSP VLP Mode

Complete the following steps to exit the ASSP VLP mode:

1. Set the external VLP signal to 1. This brings the Fabric out of the low power state.

NOTE: It takes approximately 250 µs before the Fabric to ASSP signals return to their normal state. The processor must wait 250 µs after the assertion of the VLP signal before proceeding to the next step.

2. Start the following ASSP peripherals as described by their subsections:
   - **Starting the SDIO/CE-ATA Core** on page 18
   - **Starting the OTG Core and USB PHY** on page 18

Starting the SDIO/CE-ATA Core

The external host processor must perform the following sequence of events to exit VLP mode:

1. Enable the system clock (FB_CLK) by writing to the following register:

Address	Register Name	Bit	Bit Name	State
0x00000018	Global System Clock Enable Register	2	CE_ATA_CK_EN	1

2. Enable the SD clock and internal core clocks in the CE-ATA/SDIO controller by writing to the following register.

Address	Register Name	Bit	Bit Name	State
0x0000102C	Clock Control Register	2	SD Clock Enable	1
		0	Internal Clock Enable	1

3. The CE-ATA core will be in normal mode.

Starting the OTG Core and USB PHY

To exit the VLP mode, the external processor must perform the following sequence of events:

1. Enable the external OTG_CLK clock and the system SYS_CLK clock by writing to the Global System Clock Enable Register:

Address	Register Name	Bit	Bit Name	State
0x00000018	Global System Clock Enable Register	4	OC_PHY_CK_EN	1
		3	SYS_CK_EN	1

2. Enable the SYS_CLK "internal" clock within the USB OTG core by writing to the following register:

Address	Register Name	Bit	Bit Name	State
0x00040E00	Power and Clock Gating Control	1	Gate hclk	0

3. Enable the on-chip USB PHY by writing to the following USB OTG register:

Address	Register Name	Bit	Bit Name	State
0x00040E00	Power and Clock Gating Control	0	Stop PHY Clock	0

Setting this bit to 0, will instruct the USB OTG core to de-assert the utmi_suspend_n signal, see **Figure 2** on page 3. Consequently, the USB PHY will exit the suspended state.

Address	Register Name	Bit	Bit Name	State
0x00000010	Global Enable Register	18	GL_OC_PHY_SUSPEND	0

4. Turn on the analog blocks (i.e., VBUS Comparator) in the on-chip USB PHY by writing to the following register:

Address	Register Name	Bit	Bit Name	State
0x00000010	Global Enable Register	17	VBUS_COMP_DISABLE	0

5. Configure the USB OTG core to start driving the Resume signaling, by writing to the following register:

Address	Register Name	Bit	Bit Name	State
0x00040440	USB Host Port Configuration and Status	12	Port Power	1
		6	Port Resume	1
		2	Port Enable	1

6. The host processor clears the Port Resume bit after ~ 20 ms.

Address	Register Name	Bit	Bit Name	State
0x00040440	USB Host Port Configuration and Status	6	Port Resume	0

The USB OTG core enters normal operating mode.

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Revision History

Revision	Date	Originator and Comments
A	May 2007	First release
B	July 2007	Michael Yee and Elaine Chan Updated Power vs. Clock Frequency graph.
C	November 2008	Kathleen Murchek Updated contact and trademark info. Added Notice of Disclaimer.
D	May 2009	Kathleen Murchek Updated trademark info.

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