

# Visual Enhancement Engine (VEE) 2.0 and Display Power Optimizer (DPO) 2.0 Data Sheet



**Proven System Block (PSB) for QuickLogic® Customer Specific Standard Products (CSSPs)**

## Features

QuickLogic CSSPs are architected from a unique combination of semiconductor solution platforms and PSBs based on customer requirements. This data sheet represents a specific PSB that is available for inclusion in a CSSP. To discuss options for adding this PSB to an existing CSSP, or architecting a new CSSP, contact your QuickLogic Customer Solution Architect (CSA).

The main features of the VEE 2.0 and DPO 2.0 PSBs are:

- Adapts display data, in real-time, to improve the viewing experience on mobile displays
- Significantly improves viewing image/video quality under low backlight or bright ambient light conditions
- Displays enhanced video simultaneously with graphic/text content without distortion or degradation
- Uses QuickLogic's patented ViaLink™ technology to enable flexible configurations for different processors, displays and usage cases
- Significantly extends battery life when playing video on mobile devices
- Documented battery life extensions of up to 41% using only ambient light adjustments; when Intelligent Brightness Control feature is used, battery life extensions of up to 50% (content-dependant)
- Compatible with popular types of mobile displays including Liquid Crystal Display (LCD), SuperLCD, Organic Light Emitting Diode (OLED), Active Matrix Organic Light Emitting Diode (AMOLED), Pico Projectors and more

## Overview

Today's consumers demand multimedia experiences whenever and wherever they want it. Mobile handsets and tablets are gaining more popularity as portable multimedia centers. As voice, navigation, productivity and entertainment converge, multimedia continues to be one of the key market drivers. The ability to watch mobile television, view movies, and play video games are key product differentiators.

However, one common problem for mobile multimedia devices is the viewing of video or other imagery under bright or uneven ambient light conditions. If the display is viewed outdoors, its effective dynamic range is dramatically reduced. Under bright sunshine, content is often not viewable. The common solution is to increase the brightness of the display. Unfortunately, doing so increases power drain and diminishes the battery life.

QuickLogic's VEE technology enables a television-quality visual experience on portable devices, while dramatically reducing the brightness of the display, improving battery life. This technology delivers the next generation of mobile entertainment experience by adapting display data, in real-time, to improve the ability to view video on mobile displays under low backlight or in bright ambient light conditions. QuickLogic's proven VEE solution greatly enhances image and video quality for handset users by compressing the dynamic range to match the characteristics of the display, resulting in a substantially better viewing experience. VEE 2.0 and DPO 2.0 technology is available as QuickLogic PSB options in the ArcticLink® II solution platform.



## VEE 2.0 and DPO 2.0 PSB Architecture

Figure 1 illustrates the QuickLogic VEE 2.0 and DPO 2.0 architecture.

Figure 1: VEE 2.0 and DPO 2.0 Architecture

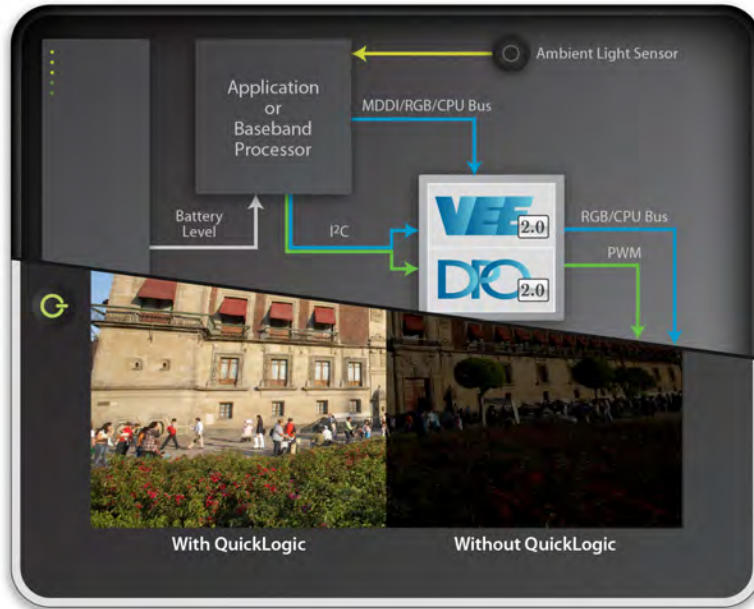
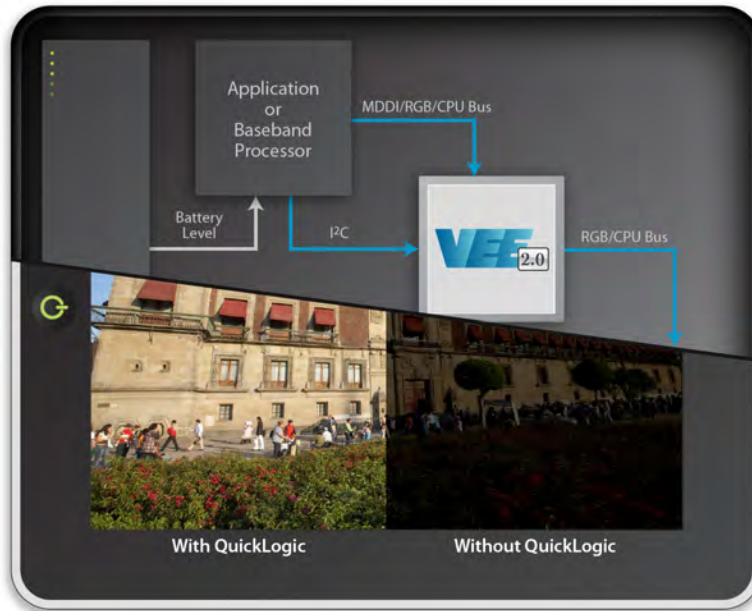


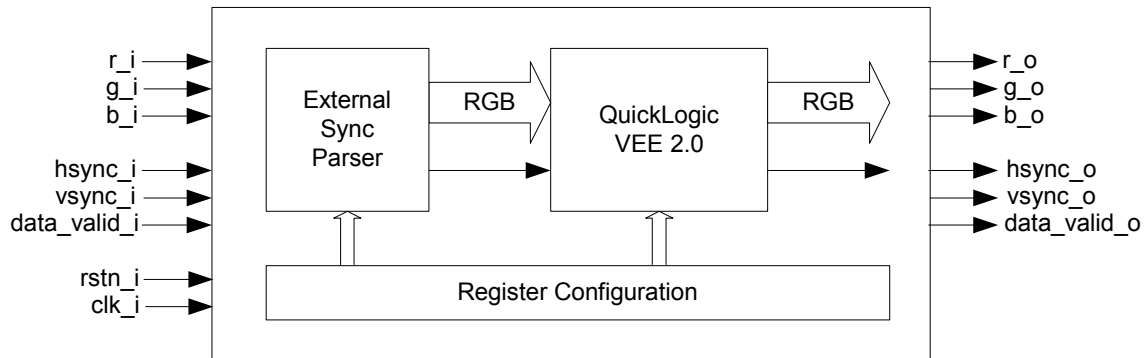
Figure 2 illustrates the QuickLogic VEE 2.0 architecture.

Figure 2: VEE 2.0 Architecture



The QuickLogic VEE 2.0 operates on RGB video format and can accept various color depths and sample rates. Figure 3 shows an example of RGB video format.

Figure 3: VEE 2.0 RGB Video Format



The video control signals [hsync, vsync and data\_valid] polarities can be adjusted as described in **Registers and Descriptions** on page 16. The processing engine can be bypassed through register setting. The external sync parser is responsible for generating internal video bit stream for the VEE 2.0.

The behavior parameters are controlled by the register configurations described in **Registers and Descriptions** on page 16 which is programmed through a CPU bus interface or an I<sup>2</sup>C-compatible interface that can be tailored depending on the processor.

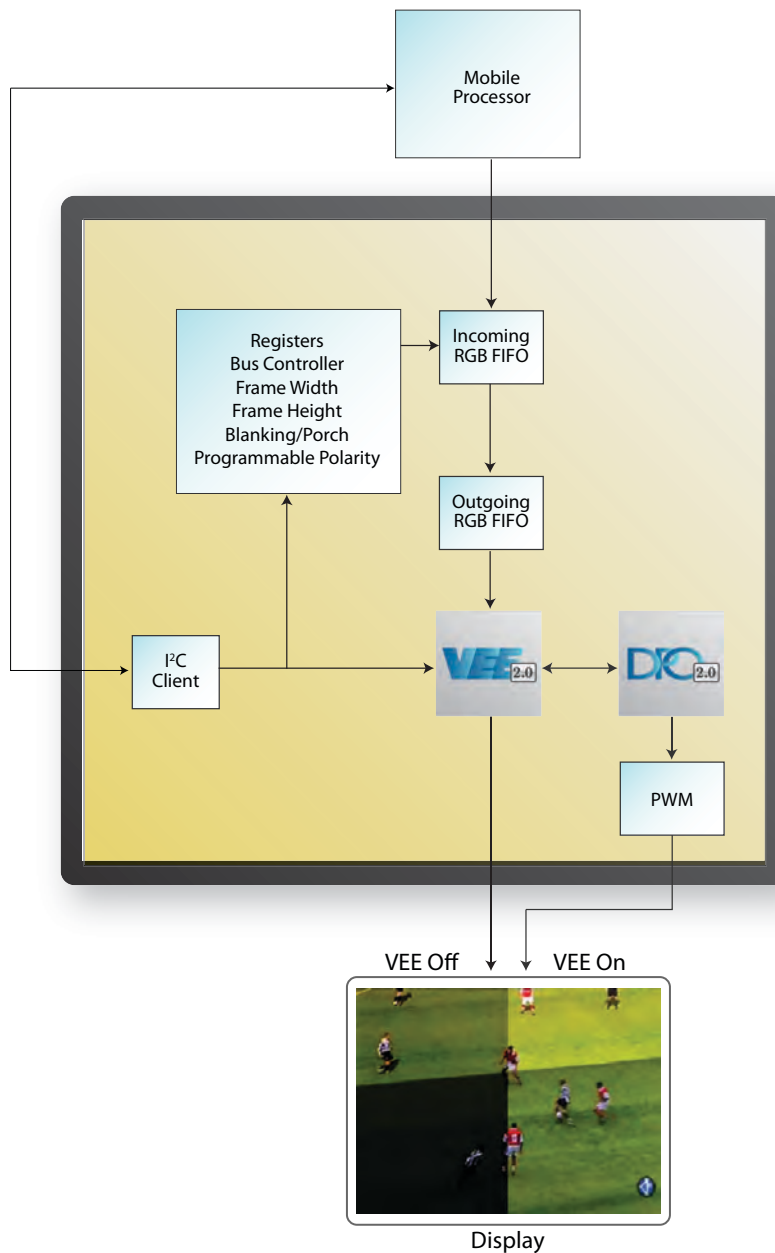
The core supports standard RGB (up to 24-bit) video I/O according to the ITU: BT656 specification. Output data format is the same as input and is synchronous. Total latency is 26 pixel clock cycles.

## Functional and Module Description

The VEE 2.0 and DPO 2.0 PSBs consist of the following functional blocks as shown in **Figure 4**.

- VEE 2.0
- DPO 2.0
- Pulse Width Modulator (PWM)

Figure 4: PSB Block Diagram





## Key Parameters of VEE

There are three fundamental parameters:

- *Strength*: Sets the overall degree of DRC. It is directly related to the ratio between the dynamic range of source and output device.
- *Variance*: Sets the spatial sensitivity of the algorithm, or the area in which iridix samples to generate the tone curve for each pixel. Measurements have established a default value that matches most closely the effect of the human visual system. However, other values can be chosen in applications where, for example, maximum detail visibility is required and most natural appearance is of secondary importance.
- *Asymmetry*: Sets the weighting given by the transform to dark areas compared to bright areas (shadows versus highlights). Measurements have established a default value that matches most closely the effect of the human visual system (which enhances dark regions much more strongly than bright ones). However, other values can be chosen, such as those which enhance shadows and highlights symmetrically.

## Dynamic Range Compression

All consumer devices employ DRC to render a source image or video stream suitable for display on an output device. Dynamic range is broadly defined as the difference in intensity between the darkest and brightest of a scene. The human eye can capture a very wide dynamic range of five orders of magnitude. However, typical displays can reproduce information over a range of only a few hundred counts or less. The dynamic range capability of a display is governed by the display technology (LCD, Plasma Display Panel (PDP), or OLED), the power or brightness, the amount of screen reflection and the ambient lighting conditions. Therefore, to retain as much information from a real-world scene after digital capture, transmission and display, dynamic range must be compressed at each step along the process. In some applications, dynamic range expansion may be required.

Furthermore, even if the display has a DRC equal to or exceeding that of the original video, DRC is still required to produce natural-looking video. Because the human eye can apply very strong DRC, a displayed video will only look natural and realistic if the same kind of processing is applied. If the display is large enough that the video fills the viewer's visual field, the eye can apply this processing itself. However, the most common use case in portable devices is that the display fills only the central portion of the field of view. The eye cannot perform this processing optimally and therefore digital processing must be substituted.

## Algorithm Background

ORMIT was developed as a result of research into biological visual systems, with particular emphasis on the human. Pre-existing models to ORMIT suffered from a number of limitations, in particular in the generation of artifacts, lack of adaptivity to different scenes, and computational complexity. The key aims in the development of ORMIT were to:

- Develop a set of algorithms that model the dynamic range processing performed by the human visual system
- Overcome clear deficiencies in existing algorithms and models
- Provide a mathematical framework suitable for efficient implementation in digital devices

iridix has been proven to be:

- Non-linear
- Adaptive (meaning that the transform is calculated based on a statistical analysis of the source image)
- Space-variant (meaning that the transform is sensitive to different regions of an image)
- Optimized in QuickLogic's VEE implementation to handle video content with ultra-low power consumption and virtually no CPU overhead

In effect, iridix automatically generates and applies a different tone curve transform to every pixel in the input video based on global user parameters which control its general behavior.

Most current consumer devices use transforms which are non-linear, fixed (non-adaptive) and uniform (space-invariant). A familiar example is gamma correction, commonly used in consumer devices. More sophisticated systems employ tone curve correction, and in some cases (adaptive) histogram-based correction. Transforms, while well-established and straightforward to implement, suffer from considerable drawbacks such as:

- Damage to regions of the source image which are already well-balanced (leading to over-saturation if applied strongly)
- Loss of contrast which tends to produce undesired color changes that require compensation

Acceptable image quality is achieved only if these transforms are applied weakly. As a result, important visual information is lost between capture and display in conventional systems, and videos do not look as natural as possible. To overcome these limitations, an adaptive, space-variant transform must be used. However, constructing such a transform that performs reliably and without artifacts under all conditions is not a trivial task. Such algorithms tend to suffer from:

- Halo
- Edge and color artifacts
- Unstable black and white points
- Excessive computational complexity

iridix is one of several space-variant algorithms (for a recent review of others, see Ledda et al., *ACM Transactions on Graphics (TOG) V24, Issue 3 (2005)*). However, iridix is to date the only method that has found successful application in digital imaging products, due to its combination of high image quality, lack of artifacts, ability to achieve strong DRC, and high efficiency. The current version is the result of years of intensive development based on the core algorithms, and is robust, high-quality and well-proven. iridix provides strong enhancement of dark and bright areas of a video, while leaving mid-tones unchanged. iridix DRC is powerful enough to compress a 16-bit original image into an 8-bit format with no loss of image detail.

The principal factor limiting the strength of iridix processing is the signal-to-noise ratio of the source video. The basic algorithm does not distinguish between video detail and noise; noise in very dark or bright areas may be rendered visible after processing. Practical implementations of iridix include a gain control feature which limits the strength of processing in different intensity ranges, so that noise is always kept outside the visible range.

More recent developments and additions to the core iridix algorithms have been the incorporation of modules for non-linear space-variant color correction, noise reduction, and preservation of fine detail. To further improve display quality, VEE technology has been supplemented by additional image and video enhancement blocks such as dithering, hue rotation, color correction, and non-linear sharpness filtering.

## **DPO 2.0 Technology and Intelligent Brightness Control**

How to conserve power when playing back video content has also become a significant issue when designing mobile media devices. As displays typically consume 30% to 60% of the total system power, there has been a tremendous amount of research put into methods of reducing display power. A common solution is to lower the brightness level of the display. Unfortunately, this solution significantly diminishes the viewing experience since most details are lost due to the lowered contrast ratio.

While the VEE uses statistical information gathered pixel-by-pixel, frame-by-frame to adjust the value of individual pixels, DPO uses that same information to adjust the backlight. The ability to provide a unique tone curve for each pixel, as well as have tight control over the display backlight, gives greater flexibility than the global adjustments of alternative implementations. The QuickLogic approach results in greater power savings and the entirely new capability of adapting to a bright environment. DPO seamlessly integrates with the QuickLogic VEE, ensuring longer battery life and an excellent visual experience by coupling the PWM driving the display backlight with the display content processing parameters of the VEE technology.

The DPO system block combines information from an on-system ambient light sensor to dynamically adjust display brightness to achieve optimal battery life. Additionally, DPO offers a unique 'Intelligent Brightness Control' feature that allows for additional reduction in display brightness when the displayed content is of lower contrast and dynamic range, such as a movie being streamed or mobile television.

Intelligent Brightness Control does not negatively impact display viewability, preserving the user experience. To prevent flickering when the contrast ratio and dynamic range of the display content changes, the CSSP can be programmed to adjust display brightness with a more natural 'breathing' effect, where the brightness is changed gradually over the course of a few seconds (implementation-dependant).

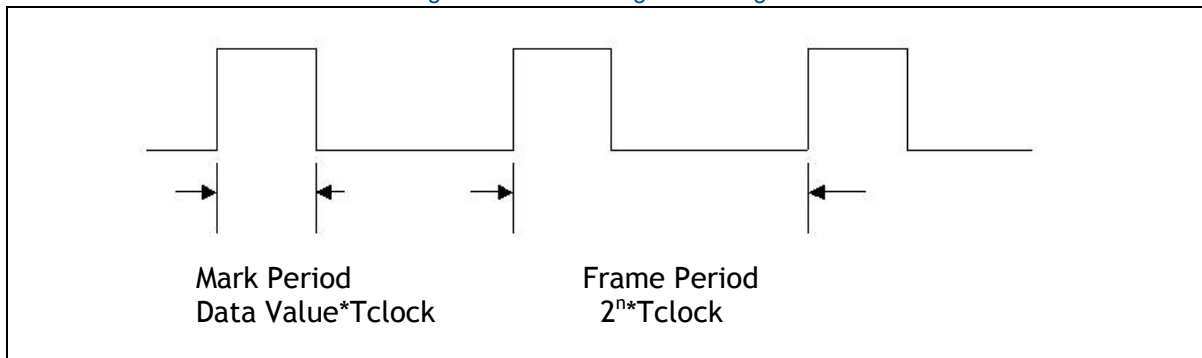
## Pulse Width Modulator Controller

The PWM is intelligently controlled by the DPO block has following features:

- 16-bit register to load count, based on which PWM width is to be generated
- Configurable PWM\_clk prescale factors of /1 to /1024 of the system clock
- Duty Cycle = Mark Period/Frame Period = Data Value/ $2^n$
- Mark Period = Data value\*Tclock
- Frame Period = Tclock\* $2^n$
- 16-bit PWM Core,  $n = 16$

**Figure 6** shows the PWM timing block diagram.

Figure 6: PWM Timing Block Diagram



## Interface List and Description

Table 1 summarizes the PSB interface signals.

Table 1: QuickLogic VEE 2.0 Pin Table

Signal Name	Signal Direction	Signal Description
<b>System Pins</b>		
reset_n	I	System reset (active low)
<b>CPU Interface Pins<sup>a</sup></b>		
cs_n	I	CPU chip select (active low)
we_n	I	CPU write enable (active low)
oe_n	I	CPU read enable (active low)
addr[7:1]	I	CPU address bus
data[7:0]	I/O	CPU data bus
<b>LCD Input Pins</b>		
Dclk_in	I	Input Pixel clock
data_valid_i	I	Start of input video frame
vsync_i	I	Vertical sync for input video data
hsync_i	I	Horizontal sync for input video data
r_i(7:0)	I	8-bit red component of input video data
g_i(7:0)	I	8-bit green component of input video data
b_i(7:0)	I	8-bit blue component of input video data
<b>LCD Output Pins</b>		
Dclk_out	O	Output Pixel clock
data_valid_o	O	Start of output video frame
vsync_o	O	Vertical sync for output video data
hsync_o	O	Horizontal sync for output video data
r_o(7:0)	O	8-bit red component of output video data
g_o(7:0)	O	8-bit green component of output video data
b_o(7:0)	O	8-bit blue component of output video data

a. See Table 2 for the I<sup>2</sup>C-compatible interface.

Table 2 provides a list of the signals and descriptions for the I<sup>2</sup>C-compatible interface.

Table 2: I<sup>2</sup>C-Compatible Interface Pin Table

Signal Name	Signal Direction	Signal Description
SCL	I	I <sup>2</sup> C-compatible command input
SDA	I/O	I <sup>2</sup> C-compatible data input/output

## Memory Maps

### Conventions

#### Read/Write Registers

Read/Write registers are registers with a single address defined. The fields of these registers can be defined with one or more of the attributes given in **Table 3**.

Table 3: Read/Write Registers

Access Tag	Name	Meaning
r	Read	This field can be read by the user/sw.
w	Write	This field can be written by the user/sw.
u	Update	This field can be updated by hardware.

#### Set and Clear Registers

A Set and Clear register has two addresses defined: “Set Address” and “Clear Address”. For write operations, these two addresses show different behavior. A “one” written to a bit position in the “Set Address” causes the corresponding bit position in the register to be set, while a “zero” leaves the corresponding bit position in the register unaffected. Alternately, a “one” written to a bit position in the “Clear Address” causes the corresponding bit position in the register to be cleared, while a “zero” leaves the corresponding bit position in the register unaffected. The fields of these registers can be defined with one or more of the attributes given in **Table 4**. For a read operation on any of these two addresses, the current value of the register is returned.

Table 4: Set and Clear Registers

Access Tag	Name	Meaning
r	Read	This field can be read by the user.
s	Set	This field can be set by the user.
c	Clear	This field can be cleared by the user.
u	Update	This field can be updated by hardware.

#### Reserved Fields

All reserved fields are ignored on read and set as zeros during write operations unless otherwise specified.

#### Reserved Registers

Addresses within the address space that are reserved return zeros on read and writes are ignored unless otherwise specified.

#### Register Field Notation

In descriptions that refer to specific register fields/bits, the notation RrRr.fff is used where RrRr refers to the register and fff refers to the referenced field/bit within that register.

In a 32-bit register, bit number 31 is the most significant bit (MSB) and bit number 0 the least significant bit (LSB).

## System Description

### Register Interfaces and I/O Configurations

All register interfaces visible to software are 32-bits.

### Address Maps

The register accesses are possible from the F2A. **Table 5** gives the register maps for the interface of the peripherals.

Table 5: F2A Address Map

Module	21	20	19:0
Common Registers in Register Control Block	0	0	0x30000 to 0x3FFFF
Clock and Reset Registers	0	0	0x20000 to 0x2FFFF
VEE Registers	0	0	0x00000 to 0x0FFFF
Intelligent Brightness Control Registers	1	0	2x00000 to 2x0FFFF

## Register Maps

### Common Registers

Table 6: Common Register Map

Register Offset	Register Name	Reset Value	Description
0x0004	Image Effect Register	0x0000_0000	This is the Image Effect register used by Read address generator and outgoing FIFO block.
0x0008	Reserved	0x0000_0000	Reserved
0x0018	PWM Control Register	0x0000_0000	This is the control register used by the PWM block.
0x001C	PWM Width Register	From Anti-fuse	This is the PWM-related parameters to be used by the PWM block.
0x0020	VEE Configuration Register	0x0000_0000/Anti-fuse	VEE configuration register.
0x0100	Use Case Register	From Anti-fuse	This is the address for use case-related information register.
0x0104	Video Parameter Register	From Anti-fuse	This is the Video Parameter register used for information such as RGB type, RGB data, etc.
0x010C	Reserved	0x0000_0000	Reserved
0x0114	Error Status Register	0x0000_0000	This is the Error Status register used to indicate different error conditions.
0x0118	Error Mask Register	0x0000_0000	Masks the Error Status register bits. Can be used to selectively enable error indications required.
0x0124	Reserved	0x0000_0000	Reserved
0x0134	Configuration Done Register	0x0000_0000	Used for indicating configuration is done.
0x0138	Reserved	0x0000_0000	Reserved

## Clock and Reset Block Registers

Table 7: Clock and Reset Block Register Map

Register Offset	Register Name	Reset Value	Description
0x0000	Global Clock Register	0x0000_01FF	Module-based clock enable control register.
0x0004	VLP Control1 Register	From Anti-fuse	VLP-related control1 register.
0x0008	VLP Control2 Register	0x0000_1E00	VLP-related control2 register.
0x000C	Clock Selection Register	0x0004_70nn (n – Anti-fuse)	Clock MUX selection and on/off control.

## VEE Block Registers

Table 8: VEE Block Register Map

Address Offset	Name	Reset Value	Description
0x00000	VEE Control Register 0	0x07	Turns the VEE processing ON and OFF. Also preserves local contrast in small areas.
0x00004	VEE Internal Debug Register	0x1F	Reserved. Always set to 0x1F.
0x0000C	Compensation Register	0x60	Sets the magnitude of the VEE algorithm.
0x00010	Variance Register	0x22	Influences spatial and intensity filtering behavior.
0x00014	Slope Register	0x20	Prevents small dark areas from becoming darker after the VEE processing.
0x0001C	Sharpen Control Register 0	0x3A	Control image sharpening intensity.
0x00020	Sharpen Control Register 1	0x1A	
0x00024	Upper Horizontal Position Register	0x00	Sets up the back porch interval for the horizontal synchronization input signal.
0x00028	Lower Horizontal Position Register	0x00	
0x0002C	Upper Vertical Position Register	0x00	Sets up the back porch interval for the vertical synchronization input signal.
0x00030	Lower Vertical Position Register	0x00	
0x00034	Upper Frame Width Register	0x00	Sets up the maximum boundary for the processed image width.
0x00038	Lower Frame Width Register	0xF0	
0x0003C	Upper Frame Height Register	0x02	Sets up the maximum boundary for the processed image height.
0x00040	Lower Frame Height Register	0x80	
0x00044	Control Register 0	0x03	Controls the data space.
0x00048	Control Register 1	0XE5	Controls the behavior of the video control synchronization and data validation signals.
0x0004C	Visual Enhancement Enable Register	0x0F	Controls the visual enhancement enable registers.
0x00050	Black Level Register	0x00	Controls the Black Level value.
0x00054	White Level Register	0xFF	Controls the White Level value.

Table 8: VEE Block Register Map (Continued)

Address Offset	Name	Reset Value	Description
0x00060	Amplification Limits Register	0x66	Restricts the luminance space in which the VEE processing can adaptively generate tone curves for each pixel
0x00064	Dithering Mode Register	0xX2	Sets the level of dithering.
0x00080	Upper Look-Up Data Register	0x00	Loads the RAM blocks internal to the QuickLogic CSSP with appropriate look-up tables for the VEE algorithm.
0x00084	Lower Look-Up Data Register	0x00	
0x00088	Look-Up Address Register	0x00	
0x0008C	Look-Up Write Enable Register	0x00	
0x003FC	VEE ID Register	0x22	Contains the VEE version identification.
0x000C0	m_11	0x40	Transforms overall colors. Color space conversion block.
0x000C4	m_12	0x00	
0x000C8	m_13	0x00	
0x000CC	m_21	0x00	
0x000D0	m_22	0x40	
0c000D4	m_23	0x00	
0x000D8	m_31	0x00	
0x000DC	m_32	0x00	
0x000E0	m_33	0x40	
0x000E8	offset_r	0x80	
0x000EC	offset_g	0x80	
0x000F0	offset_b	0x80	

## Intelligent Brightness Control Registers

Table 9: Intelligent Brightness Control Register Map

Register Offset	Register Name	Reset Value	Description
0x220000	Intelligent Brightness Control Register	0x0000	Turns on/off Intelligent Brightness Control block.
0x220004	Minimum Intensity Register	0x00C0	Minimum intensity of display brightness.
0x220008	Clip Count Register [15:0]	0x1000	Indicates how many pixels in a frame can be saturated.
0x22000C	Clip Count Register [31:16]	0x0000	Indicates how many pixels in a frame can be saturated.
0x220010	Falling Step Size Register	0x1000	Maximum change allowed in any one period when decreasing brightness.
0x220014	Rising Step Size Register	0x0200	Maximum change allowed in any one period when increasing brightness.

## Registers and Descriptions

### Common Registers

#### Image Effect Register

Register Offset: 0x0004

Reset Value: 0x0000\_0000

Name	Access Tag	Bit	Description
Reserved	rw	1:0	Reserved
Reserved	r	31:2	Reserved

#### Row Number Register

Register Offset: 0x0008

Reset Value: 0x0000\_0000

Name	Access Tag	Bit	Description
Reserved	ru	9:0	Reserved
Reserved	ru	10	Reserved.
Reserved	r	31:11	Reserved

#### PWM Control Register

Register Offset: 0x0018

Reset Value: 0x0000\_0000

Name	Access Tag	Bit	Description
rPWMEEn	rw	0	Enables the PWM block.
Reserved	r	31:1	Reserved

#### PWM Width Register

Register Offset: 0x001C

Reset Value: From Anti-fuse

Name	Access Tag	Bit	Description
rPWMWidth	rw	15:0	This is the 16-bit value to be used by the PWM module to calculate the pulse width (duty cycle). (From Anti-fuse)
Reserved	r	31:16	Reserved

### VEE Configuration Register

Register Offset: 0x0020

Reset Value: 0x0000\_1FC0/Anti-Fuse

**NOTE:** The bits [1:0] and bits [5:3] have Anti-fuse values during reset.

Name	Access Tag	Bit	Description
rVEEBypassMode	rw	1:0	Decodes the VEE bypass mode. 10 – RGB-in to RGB-out with the VEE bypass 01 – Video from outgoing FIFO block with the VEE bypass 00 – VEE data output 11 – Reserved (From Anti-fuse)
Reserved	r	2	Reserved
rINVDE	rw	3	Controls polarity of RGB data enable. 0 – Normal DE 1 – Invert DE (From Anti-fuse)
rINVSync	rw	4	Controls polarity of VSync. 0 – Normal VSync 1 – Invert VSync polarity (From Anti-fuse)
rINVHSync	rw	5	Controls polarity of HSync. 0 – Normal HSync 1 – Invert HSync polarity (From Anti-fuse)
rVEE_Ena_Mask	rw	12:6	Used for debugging purposes.
Reserved	r	31:13	Reserved

### Use Case Register

Register Offset: 0x0100

Reset Value: 0x0000\_0000/Anti-fuse

**NOTE:** The bits [2:0] and bit [5] has Anti-fuse values during reset.

Name	Access Tag	Bit	Description
Reserved	r	0	Reserved
rUseCase	rw	2:1	00 – RGB-In to RGB-Out 01 – Reserved 10 – Reserved 11 – Reserved
Reserved	r	4:3	Reserved
Reserved	r	5	Reserved
rInVsyncPolarity	rw	6	Indicates the Polarity for Vsync: 0 – Active high 1 – Active low

Name	Access Tag	Bit	Description
rInvHsyncPolarity	rw	7	Indicates the Polarity for Hsync: 0 – Active high 1 – Active low
rInvDEPolarity	rw	8	Indicates the Polarity for Data enable: 0 – Active high 1 – Active low
Reserved	r	31:9	Reserved

### Video Parameter Register

Register Offset: 0x0104

Reset Value: From Anti-fuse

Name	Access Tag	Bit	Description
Reserved	rw	11:0	Reserved
Reserved	r	31:12	Reserved

### Burst Length Register

Register Offset: 0x010C

Reset Value: 0x0000\_0000

Name	Access Tag	Bit	Description
Reserved	rw	16:0	Reserved
Reserved	r	31:17	Reserved

### Error Status Register

Register Offset: 0x0114

Reset Value: 0x0000\_0000

**NOTE:** For the error output to fabric to be generated, set the Error Status bit and the corresponding Error Mask register bit to '1'.

Name	Access Tag	Bit	Description
Reserved	rcu	3:0	Reserved.
Reserved	ru	8:4	Reserved.
rIncomingFIFO Overwrite	rcu	9	Indicates overwrite in the Incoming RGB FIFO. A write of 1'b1 by software will clear this bit. Software must clear this bit only after reading the address at which the overwrite has occurred.
Reserved	rcu	10	Reserved.
Reserved	rcu	11	Reserved.
Reserved	rcu	12	Reserved.
Reserved	rcu	13	Reserved.

Name	Access Tag	Bit	Description
Reserved	r	15:14	Reserved
rIntFb1	rcu	16	Interrupt 1 from fabric. A write of 1'b1 by software will clear this bit.
rIntFb2	rcu	17	Interrupt 2 from fabric. A write of 1'b1 by software will clear this bit.
rIntFb3	rcu	18	Interrupt 3 from fabric. A write of 1'b1 by software will clear this bit.
rIntFb4	rcu	19	Interrupt 4 from fabric. A write of 1'b1 by software will clear this bit.
Reserved	r	31:20	Reserved.

### Error Mask Register

Register Offset: 0x0118

Reset Value: 0x0000\_0000

Name	Access Tag	Bit	Description
Reserved	rw	3:0	Reserved
Reserved	r	8:4	Reserved
Reserved	rw	9	Reserved
Reserved	rw	10	Reserved.
Reserved	rcu	11	Reserved.
Reserved	rcu	12	Reserved.
Reserved	rcu	13	Reserved.
Reserved	r	15:14	Reserved
rIntFb1	rcu	16	Interrupt 1 mask.
rIntFb2	rcu	17	Interrupt 2 mask.
rIntFb3	rcu	18	Interrupt 3 mask.
rIntFb4	rcu	19	Interrupt 4 mask.
Reserved	r	31:20	Reserved

### Incoming RGB FIFO Overflow Address Register

Register Offset: 0x0124

Reset Value: 0x0000\_0000

Name	Access Tag	Bit	Description
Reserved	ru	31:0	Reserved.

### Configuration Done Register

Register Offset: 0x0134

Reset Value: 0x0000\_0000

Name	Access Tag	Bit	Description
rConfigDone	rw	0	This bit is set by software only when the configuration of following registers is completed: - Use Case register - Video Parameter register - Display Attributes register - Xwidth and Ywidth registers Software ensures that before any of the above registers are programmed the configuration done bit is cleared by software.
Reserved	r	31:1	Reserved

### FIFO Flush Register

Register Offset: 0x0138

Reset Value: 0x0000\_0000

Name	Access Tag	Bit	Description
Reserved	rw	1:0	Reserved.
Reserved	r	31:2	Reserved

## Clock and Reset Block Registers

### Global Clock Register

**NOTE:** All clock and reset block registers offset is relative to the Clock and Reset module base address.

Register Offset: 0x0000

Reset Value: 0x0000\_01ff

Name	Access Tag	Bit	Description
rGlobal_clock_enable	rw	0	Global clock enable. If set, the clocks are enabled.
rVEE_enable	rw	1	Clock enable for the VEE block. If set, clock is enabled.
Reserved	rw	2	Reserved.
Reserved	rw	3	Reserved.
rPWM_enable	rw	4	Clock enable for the PWM block. If set, clock is enabled.
Reserved	rw	5	Reserved.
Reserved	rw	8:6	Reserved, must be set to '0'.

Name	Access Tag	Bit	Description
rVLP_Ctrl_Sel	rw	9	Selects the VLP control set register: 0 – Ctrl Set2 is selected 1 – Ctrl Set1 is selected
Reserved	rw	10	Reserved.
Reserved	r	31:11	Reserved

### VLP Control Set1/2 Register

Register Offset: 0x0004 (Set 1) and 0x0008 (Set 2)

Reset Value: From Anti-fuse (Set 1) and 0x0000\_1E00 (Set 2)

Name	Access Tag	Bit	Description
rFB_VLP_Ctrl	rw	1:0	00 – FB_core: VLP Mode IOs: VLP mode 01 – FB_core: Active IOs: VLP mode 10 – FB_core: Active IOs: Active 11 – Reserved
rGPIO_VLP_CTRL	rw	2	Used in conjunction with rFB_VLP_CTRL. To be gated and passed only if FB_VLP_Ctrl is 01 or 10.
Reserved	rw	3	Reserved.
rPWM_enable	rw	4	VLP mode enable for the PWM block. If set VLP mode is disabled.
Reserved	rw	5	Reserved.
Reserved	rw	6	Must always be set to '0'.
Reserved	rw	11:7	Reserved.
Reserved	rw	13:12	Must always be set to '1'.
Reserved	r	31:14	Reserved.

## Clock Selection Register

Register Offset: 0x000C

Reset Value: 0x0004\_70nn (n – Anti-fuse)

Name	Access Tag	Bit	Description
Reserved	r	2:0	Reserved.
Reserved	r	3	Reserved.
rPWMCkSel	r	7:4	Indicates the division factor for the PWM clock: 0000 – /1 0001 – /2 0010 – /4 ..... 1010 – /1024 1011-1111 – Reserved
Reserved	rw	8	Reserved.
Reserved	rw	9	Reserved.
Reserved	rw	10	Reserved.
rPixelClkMuxGate	rw	11	If set, switches off the pixel_clk. This is used for changing the pixel_clk selection.
Reserved	rw	12	Reserved.
rPixClkoutEn	rw	13	If set, the clock pixel_clk_out to Fabric is switched on.
Reserved	rw	16:14	Reserved.
invert_pixel_clk_out	rw	17	If set, inverts the pixel_clk_out.
Reserved	rw	18	Reserved, must be set to '0.
Reserved	r	31:19	Reserved.

## VEE Block Registers

### VEE Control Register 0

This register turns the VEE processing ON and OFF. When the VEE is OFF, video data passes to the output without any changes. This register also preserves local contrast in small areas. There are two versions of customer implementation, weak and strong.

Register Offset: 0x00000

Reset Value: 0x07

Name	Access Tag	Bit(s)	Description
VEE_control_1_0	RW	0	Switches the VEE functionality on and off: 1 – ON 0 – OFF
		2:1	Local contrast strength: 0x0 – OFF 0x1 or 0x2 – weak local contrast 0x3 – strong local contrast
		7:3	Reserved

### VEE Internal Debug Register

This register is used for internal debugging.

Register Offset: 0x00004

Reset Value: 0x1f

Name	Access Tag	Bit(s)	Description
Reserved	RW	7:0	Always set to 0x1F.

### VEE Compensation Register

The VEE Compensation register allows the software to set the degree to which the algorithm compensates for reduced display brightness or increased ambient light.

Register Offset: 0x0000C

Reset Value: 0x60

Name	Access Tag	Bit	Description
compensation_reg	RW	2:0	Unused : "000"
		7:3	Compensation value

### VEE Variance Register

The VEE Variance register influences spatial and intensity filtering behavior. Decreasing of the filtering passes will progressively increase the spatial sensitivity or intensity selectivity of the algorithm. The default value of 0x22 is generally suitable, so the variance can be left as 0x22.

Register Offset: 0x00010

Reset Value: 0x22

Name	Access Tag	Bit	Description
variance_reg	RW	7:0	Variance value

### VEE Slope

Slope restriction is a supplementary module preventing small dark areas from becoming darker after the VEE processing. The default value of 0x20 is generally suitable, so the slope can be left as 0x20.

Register Offset: 0x00014

Reset Value: 0x20

Name	Access Tag	Bit(s)	Description
slope_reg	RW	7:0	Slope restriction value

### Sharpen Control 0

The Sharpen Control registers control image sharpening intensity. This register (Sharpen Control 0) sets up the first coefficient of the filter and switches ON/OFF the filtering algorithm. The Sharpen Control 1 register sets up the second coefficient of the filter.

Register Offset: 0x0001C

Reset Value: 0x3A

Name	Access Tag	Bit(s)	Description
sharpen_cntl_reg0	RW	4:0	Filter coef1
		5	Sharpening filter on/off
		7:6	"00"

### Sharpen Control 1

The Sharpen Control registers control image sharpening intensity. The Sharpen Control 0 register sets up the first coefficient of the filter and switches ON/OFF the filtering algorithm. This register (Sharpen Control 1) sets up the second coefficient of the filter.

Register Offset: 0x00020

Reset Value: 0x1A

Name	Access Tag	Bit(s)	Description
sharpen_cntl_reg1	RW	4:0	Filter coef2
		7:5	"000"

### Horizontal Position Register [11:8] (Upper)

The horizontal position registers set up the back porch interval for the horizontal synchronization input signal in pixel time units (i.e., pixel clock cycles).

Register Offset: 0x00024

Reset Value: 0x00

Name	Access Tag	Bit(s)	Description
hs_pos_reg[11:8]	RW	3:0	HS position upper

### Horizontal Position Register [7:0] (Lower)

See Horizontal Position Register [11:8] description.

Register Offset: 0x00028

Reset Value: 0x00

Name	Access Tag	Bit(s)	Description
hs_pos_reg[7:0]	RW	7:0	HS position lower

### Vertical Position Register [11:8] (Upper)

The vertical position registers set up the back porch interval for the vertical synchronization input signal in pixel time units (i.e., pixel clock cycles).

Register Offset: 0x0002C

Reset Value: 0x00

Name	Access Tag	Bit(s)	Description
vs_pos_reg[11:8]	RW	3:0	Vertical initial position, upper bits.

### Vertical Position Register [7:0] (Lower)

See Vertical Position Register [11:8] description.

Register Offset: 0x00030

Reset Value: 0x00

Name	Access Tag	Bit(s)	Description
vs_pos_reg[7:0]	RW	7:0	Vertical initial position, lower bits.

### Frame Width Register [11:8] (Upper)

The frame width registers set up the maximum bounds for the processed image width. The value of this register depends upon the resolution of the LCD screen being used. For the frame width, find the pixel width of the screen, and divide this number by two. For example, a 640(H) x 480(W) screen has a width of 480 pixels. Divided by two gives the value 240, which is 0xF0 in hex.

Register Offset: 0x00034

Reset Value: 0x00

Name	Access Tag	Bit(s)	Description
frame_width_reg[11:8]	RW	3:0	Frame width, upper bits.

### Frame Width Register [7:0] (Lower)

See Frame Width Register [11:8] description.

Register Offset: 0x00038

Reset Value: 0xF0

Name	Access Tag	Bit(s)	Description
frame_width_reg[7:0]	RW	7:0	Frame width, lower bits.

### Frame Height Register [11:8] (Upper)

The frame height registers set up the maximum bounds for the processed image height. The value of this register depends upon the resolution of the LCD screen being used. For the frame height, use the pixel height of the screen. For example, a 640(H) x 480(W) screen has a height of 640 pixels, which is 0x280 in hex.

Register Offset: 0x0003C

Reset Value: 0x02

Name	Access Tag	Bit(s)	Description
frame_height_reg[11:8]	RW	3:0	Frame height, upper bits.

### Frame Height Register [7:0] (Lower)

See Frame Height Register [11:8] description.

Register Offset: 0x00040

Reset Value: 0x80

Name	Access Tag	Bit(s)	Description
frame_height_reg[7:0]	RW	7:0	Frame height, lower bits.

### Control Register 0

This register controls the data space.

Register Offset: 0x00044

Reset Value: 0x03

Name	Access Tag	Bit(s)	Description
control_reg0	RW	1:0	Data space: 0x2 – YUV 0x3 – RGB
		7:2	Reserved

### Control Register 1

This register controls the behavior of the video control synchronization and data validation signals. The Horizontal Polarity bit chooses the active edge of the RGB horizontal synchronization input signal. If Horizontal Polarity is equal to a logical one then the rising edge will be used to start measuring the horizontal time interval. If Horizontal Polarity is equal to a logical zero then the falling edge will be used. The Horizontal Phase register selects the phase of the RGB horizontal synchronization signal. This option may be useful when the horizontal sync active edge occurs in interleaved video streams. If this were the case then data and sync signals would not be aligned and a shift between the data and the horizontal sync might occur. To avoid this situation one can correct the condition by altering the value of the Horizontal Phase register. Both the field correction and field generation registers can be left at their default values.

Register Offset: 0x00048

Reset Value: 0xE5

Name	Access Tag	Bit(s)	Description
control_reg1	RW	0	hs_polarity – 1
		1	vs_polarity – 1
		2	field_generation – 1
		3	hs_phase – 0
		5:4	field_correction – 10
		6	direct_active – 1
		7	dvi edge (rising/falling) – 0 Bit 7 is for board verification only

### Visual Enhancement Enable Register

This register controls the visual enhancement functional block enables.

Register Offset: 0x0004C

Reset Value: 0x0F

Name	Access Tag	Bit(s)	Description
pwd_reg	RW	0	VEE 1 – enabled 0 – disabled
		1	Sharpen 1 – enabled 0 – disabled
		2	Color matrix 1 – enabled 0 – disabled
		3	Gamma 1 – enabled 0 – disabled
		7:4	Reserved

### Black Level Register

The value in this register is represented in 6.2 format. In this format, a number with a fractional part is represented as follows: the upper 6 bits represent the integer part, and the least significant 2 bits represent the fractional part (such that bits “10” equal 1/2). Video data is considered to have maximum range from 0 to 255.

The value stored in the Black Level Register is used as zero level for the VEE processing in all unsigned data channels. In the case of YUV data, Black Level is used only for the Y channel. In the case of RGB data, the same Black Level is subtracted from all three R, G and B Channels. For example, normal ITU656 video data, according to the standard, should have Black Level = 16. For this type of video, write 40h into the Black Level Register. Data below the Black Level will not be processed and remains unchanged.

Register Offset: 0x00050

Reset Value: 0x00

Name	Access Tag	Bit(s)	Description
black_level_reg	RW	7:0	black_level_reg / 4 = Black Level

### White Level Register

The value in this register is represented in 6.2 format. In this format, a number with a fractional part is represented as follows: the upper 6 bits represent the integer part, and the least significant 2 bits represent the fractional part (such that bits “10” equal ½). Video data is considered to have maximum range from 0 to 255.

The value stored in the White Level Register is used as a White Point for the VEE processing in all unsigned data channels, the Black Level is used as a starting point. In the case of YUV data, the Black Level is used only for the Y channel. In the case of RGB data, the White Level is used for all three R, G and B Channels. For example, normal ITU656 video data, according to the standard, the White Level = 240 and the Black Level = 16. For this type of video, write C3h into the White Level Register. The formula for the White Level register value is:

White and Black level in formula have range 0 – 255.

Register Offset: 0x00054

Reset Value: 0xFF

Name	Access Tag	Bit(s)	Description
white_level_reg	RW	7:0	$255 - ((255 - \text{white\_level\_reg}) / 4) = \text{White Level}$

### Amplification Limits Register

This register is used to restrict the luminance space in which the VEE processing can adaptively generate tone curves for each pixel.

Register Offset: 0x00060

Reset Value: 0x66

Name	Access Tag	Bit(s)	Description
ampl_limit_reg	RW	3:0	Dark limit
		7:4	Bright limit

### Dithering Mode Register

This register sets the level of dithering. When the number of color gradations of a display device is small (for example 6 bit per color) a pixel dithering can make gradients look smother. There can be a situation when the VEE output signal is 10 bits but the signal needs to be compressed into 8 bits. The best way for this is to use dithering of the least significant bits and then truncate these bits. The dithering can be performed by the VEE processing. However, the truncation must be done by a hardware designer outside the VEE processing.

Two least significant bits (D1, D0) of this register are responsible for strength of dithering. Higher bits are not used. There are four possible levels of dithering.

Register Offset: 0x00064

Reset Value: 0xX2

Name	Access Tag	Bit(s)	Description
dither_reg	RW	1:0	Dithering mode: 0x0 – No dithering 0x1 – One least significant bit of the output signal is dithered 0x2 – Two bits are dithered 0x3 – Three bits are dithered
		7:2	Reserved.

### Look-Up Table Data Registers

The Look-Up Table Data Registers are used to load the RAM blocks internal to the QuickLogic CSSP with appropriate look-up tables (LUTs) for the VEE algorithm. For loading the LUT data, there are four registers; two data registers, one address register, and a write enable register.

The sequence to write a single word is:

1. Write the high byte to the high byte register.
2. Write the low byte to the low byte register.
3. Write the address to the address register.
4. Write to the write enable register

The addresses for the table are:

- 0x80 to load the high byte of data
- 0x84 to load the low byte of data
- 0x88 to load the address
- 0x8C to load the write enable

**NOTE:** The Look-Up Tables are pre-initialized. Do not changes these values without contacting QuickLogic for more information first. Changing these values can lead to improper VEE calibration.

### Look-Up Table Data Register [15:8]

The required LUT values are included in the drivers supplied by QuickLogic.

This register contains the upper byte of data to be loaded into the LUTs.

Register Offset: 0x00080

Reset Value: 0x00

Name	Access Tag	Bit(s)	Description
lut_data_reg[15:8]	WO	7:0	Write only, reads 0x55

### Look-Up Table Data Register [7:0]

This register contains the lower byte of data to be loaded into the LUTs.

Register Offset: 0x00084

Reset Value: 0x00

Name	Access Tag	Bit(s)	Description
lut_data_reg[7:0]	WO	7:0	Write only, reads 0x55

### Look-Up Table Address Register

This register contains the local address where data is to be loaded.

Register Offset: 0x00088

Reset Value: 0x00

Name	Access Tag	Bit(s)	Description
lut_addr_reg[7:0]	WO	7:0	Write only, reads 0x55

### Look-Up Table Write Enable Register

This register specifies which LUT is to be loaded.

Register Offset: 0x0008C

Reset Value: 0x00

Name	Access Tag	Bit(s)	Description
lut_we_reg	RW	0	Reserved
		1	Asymmetry write enable
		2	Sharpening write enable
		3	Gamma write enable
		7:4	Reserved

### VEE ID Register

This register contains the VEE version identification.

Register Offset: 0x003FC

Reset Value: 0x22

Name	Access Tag	Bit(s)	Description
VEE_ID_rev	RO	7:0	VEE version identification. Read only

### Color Matrix Registers

These registers are used to transform overall colors. Color Matrix coefficient registers are in fixed point format 2.6.

Overall color transform can be defined as follows:

$$M = \begin{pmatrix} m_{11} & m_{12} & m_{13} \\ m_{21} & m_{22} & m_{23} \\ m_{31} & m_{32} & m_{33} \end{pmatrix}$$

$$\begin{pmatrix} y\_or\_r \\ u\_or\_g \\ v\_or\_b \end{pmatrix} = M \cdot \begin{pmatrix} r \\ g \\ b \end{pmatrix} + \begin{pmatrix} offset\_r \\ offset\_g \\ offset\_b \end{pmatrix}$$

where offsets are signed integers with 'zero point' = 0x80. For example 0x7F = -1

Register Offset: 0x000C0, 0x000C4, 0x000C8, 0x000CC, 0x000D0, 0x000D4, 0x000D8,  
0x000DC, 0x000E0

Reset Value: 0x40, 0x00, 0x00, 0x00, 0x40, 0x00, 0x00, 0x00, 0x40

Name	Access Tag	Bit(s)	Description
m_11	RW	7:0	Color space conversion block.
m_12	RW	7:0	
m_13	RW	7:0	
m_21	RW	7:0	
m_22	RW	7:0	
m_23	RW	7:0	
m_31	RW	7:0	
m_32	RW	7:0	
m_33	RW	7:0	

Register Offset: 0x000E8, 0x000EC, 0x000F0

Reset Value: 0x80, 0x80, 0x80

Name	Access Tag	Bit(s)	Description
offset_r	RW	7:0	Offset values for R, G and B.
offset_g	RW	7:0	
offset_b	RW	7:0	

## Intelligent Brightness Control Registers

### Intelligent Brightness Control Register

The Intelligent Brightness Control register turns on/off Intelligent Brightness Control block.

Register Offset: 0x220000

Reset Value: 0x0000

Name	Access Tag	Bit(s)	Description
Intelligent Brightness Control	RW	1:0	Turns on/off Intelligent Brightness Control block. 0 = On 1 = Off
Reserved	RW	15:2	Reserved.

### Minimum Intensity Register

Sets the display minimum brightness.

Register Offset: 0x220004

Reset Value: 0x00C0

Name	Access Tag	Bit(s)	Description
Minimum Intensity	RW	7:0	Intensity level.
Reserved	RW	15:8	Reserved.

### Clip Count Register

The Clip Count registers indicates how many pixels in a frame can be saturated.

Register Offset: 0x220008 and 0x22000C

Reset Value: 0x1000 and 0x0000

Name	Access Tag	Bit(s)	Description
Clip Count	RW	15:0	Indicates how many pixels in a frame can be saturated.
		31:16	

### Falling Step Size Register

The Falling Step Size register indicates the maximum change allowed in any one period when decreasing the brightness.

Register Offset: 0x220010

Reset Value: 0x1000

Name	Access Tag	Bit(s)	Description
Falling Step Size	RW		Indicates the maximum change allowed in any one period when decreasing the brightness.

### Rising Step Size Register

The Rising Step Size register indicates the maximum change allowed in any one period when increasing the brightness.

Register Offset: 0x220014

Reset Value: 0x0200

Name	Access Tag	Bit(s)	Description
Rising Step Size	RW		Indicates the maximum change allowed in any one period when increasing the brightness.

## Supported Operating Systems

Figure 10 shows the operating systems currently supported.

Table 10: Supported Operating Systems

Operating System	Android 3.0 and Below	Linux 2.6.28	WinMobile 6.x	WinMobile 7
Supported	Yes	Yes	Contact QuickLogic	Contact QuickLogic

## Power Consumption

### Programmable Fabric Power Consumption

The ultra low power programmable fabric developed by QuickLogic is ideal for implementing customized display subsystem control and connectivity solutions, additional memory and peripheral subsystem functionality custom logic and processor interfaces. The dynamic power consumption varies depending on the operating conditions and what functions are used in the fabric.

## Platform Power Consumption

**Table 11** shows the logic power consumption. **Table 12** shows the VCCIO power consumption. The following assumptions apply:

- RGB out Load = 10 pF
- RGB toggle rate = 20%

Table 11: Power Consumption

VCC (V)	Display	Horizontal	Vertical	Pixel Clock Max. MHz (VESA with Margin)	VEE Power (mW)	DP0 2.0 Power
1.8	VGA	640	480	25	57	TBD
	WVGA	800	480	31	70	TBD
	FWVGA	854	480	33	74	TBD
	SVGA	800	600	40	88	TBD
	W-SVGA	1024	600	51	107	TBD
	XGA	1024	768	68	139	TBD
	WXGA	1280	768	84	160	TBD
	WXGA	1366	768	85	171	TBD

Table 12: VCCIO Power Consumption

Resolution	Horizontal Pixels	Vertical Pixels	Pixel Clock (VESA with Margin)	Color Depth	I/O Power (mW) VCCIO = 3.3 V
VGA	640	480	25	18	16
				24	19
WVGA	800	480	31	18	19
				24	23
FWVGA	854	480	33	18	20
				24	24
SVGA	800	600	40	18	23
				24	28
W-SVGA	1024	600	52	18	29
				24	36
XGA	1024	768	68	18	37
				24	46
WXGA	1280	768	84	18	46
				24	57
WXGA	1366	768	85	18	49
				24	61

## Contact Information

Phone: (408) 990-4000 (US)  
(647) 367-1014 (Canada)  
+(44) 1932-21-3160 (Europe)  
+(886) 2-2345-5600 (Asia)

E-mail: [info@quicklogic.com](mailto:info@quicklogic.com)

Sales: [America-sales@quicklogic.com](mailto:America-sales@quicklogic.com)  
[Europe-sales@quicklogic.com](mailto:Europe-sales@quicklogic.com)  
[Asia-sales@quicklogic.com](mailto:Asia-sales@quicklogic.com)  
[Japan-sales@quicklogic.com](mailto:Japan-sales@quicklogic.com)

Support: [www.quicklogic.com/support](http://www.quicklogic.com/support)

Internet: [www.quicklogic.com](http://www.quicklogic.com)

## Revision History

Revision	Date	Originator and Comments
A	July 2011	Paul Karazuba and Kathleen Bylsma

## Notice of Disclaimer

QuickLogic is providing this design, product or intellectual property "as is." By providing the design, product or intellectual property as one possible implementation of your desired system-level feature, application, or standard, QuickLogic makes no representation that this implementation is free from any claims of infringement and any implied warranties of merchantability or fitness for a particular purpose. You are responsible for obtaining any rights you may require for your system implementation. QuickLogic shall not be liable for any damages arising out of or in connection with the use of the design, product or intellectual property including liability for lost profit, business interruption, or any other damages whatsoever. QuickLogic products are not designed for use in life-support equipment or applications that would cause a life-threatening situation if any such products failed. Do not use QuickLogic products in these types of equipment or applications.

QuickLogic does not assume any liability for errors which may appear in this document. However, QuickLogic attempts to notify customers of such errors. QuickLogic retains the right to make changes to either the documentation, specification, or product without notice. Verify with QuickLogic that you have the latest specifications before finalizing a product design.

## Copyright and Trademark Information

Copyright © 2011 QuickLogic Corporation. All Rights Reserved.

The information contained in this document is protected by copyright. All rights are reserved by QuickLogic Corporation. QuickLogic Corporation reserves the right to modify this document without any obligation to notify any person or entity of such revision. Copying, duplicating, selling, or otherwise distributing any part of this product without the prior written consent of an authorized representative of QuickLogic is prohibited.

QuickLogic and ViaLink are registered trademarks; and the QuickLogic logo is a trademark of QuickLogic. Other trademarks are the property of their respective companies.