

••••• **Programmable Solution Platform Including Hi-Speed Universal Serial Bus (USB) 2.0 On-The-Go (OTG) and SD/SDIO/MMC/CE-ATA**

## Device Highlights

### Hi-Speed USB 2.0 OTG Controller

- Single port OTG with embedded high-speed PHY
- Optional 12-signal ULPI interface
- Full-speed CEA-936-A mini-USB analog carkit interface
- Dedicated DMA controller
- High-speed up to 480 Mbits/sec.

### SD/SDIO/MMC/CE-ATA Host Controller

- SD/SDIO 1-bit or 4-bit up to 52 MHz with Secure Digital High Capacity (SDHC) support
- CE-ATA 1-bit, 4-bit or 8-bit up to 52 MHz
- MMC 1-bit, 4-bit or 8-bit up to 52 MHz
- High-speed and flexible to support multiple storage options and SDIO peripherals

### ASSP/FPGA Interface

- 8 Kbytes scratchpad memory
- Flexible Host interface for USB and SD/SDIO/MMC/CE-ATA ports
- DMA and power management functions
- Direct memory aperture for peripheral subsystems

### Flexible Programmable Fabric

- 0.18  $\mu\text{m}$ , six layer metal CMOS process
- 1.8 V core voltage, 1.8/2.5/3.3 V drive capable I/Os
- 36 Kbits of SRAM – seven dual-port 4-Kbit high performance SRAM blocks
- Embedded synchronous/asynchronous FIFO controllers
- One user configurable clock manager (CCM) (110-ball WLCSP and 196-ball TFBGA

packages only) (see **Configurable Clock Manager** on page 17 for an explanation of CCM)

- Up to 120 programmable I/Os available
- 100,000 system gates
- Nonvolatile, instant-on
- IEEE 1149.1 boundary scan testing compliant

### Programmable I/O

- Bank programmable drive strength
- Bank programmable slew rate control
- Independent I/O banks capable of supporting multiple I/O standards in one device
- Native support for DDRIOs (196-ball package only)
- Bank programmable I/O standards: LVTTTL, LVCMOS, and LVCMOS18
- Can be used for level shifter and I/O voltage translator

### Very Low Power (VLP) Mode

- The QuickLogic<sup>®</sup> ArcticLink Solution Platform has a special VLP pin which can enable a low power sleep mode that significantly reduces the overall power consumption of the device by placing the device in standby.
- Enter/exit VLP mode from/to normal operation in less than 250  $\mu\text{s}$  (typical)

### Security Links

There are several security links to disable JTAG access to the device. Programming these optional links completely disables access to the device from the outside world and provides an extra level of design security not possible in SRAM-based FPGAs.

### JTAG

QuickLogic ArcticLink Solution Platform supports IEEE 1149.1 boundary scan or post-manufacturing testability. External access to this feature can be completely disabled.

## Solution Platform Combining USB, SD/SDIO/MMC/CE-ATA, and Programmable Fabric

Table 1: ArcticLink Solution Platform

Features		QL1A100
Max Programmable Fabric Gates		100,000
Logic Cells		640
Max I/O		120
RAM Modules		7
FIFO Controllers		7
RAM bits <sup>a</sup>		36,864
CCM (110-ball WLCSP and 196-ball TFBGA packages only)		1
Packages	WLCSP (10 x 11 array)	110
	TFBGA (8 mm x 8 mm)	121
	TFBGA (12 mm x 12 mm)	196
Hi-Speed USB 2.0 OTG Controller with DMA, ULPI Interface and On-Chip PHY		1
SD/SDIO/MMC/CE-ATA Controller		1
Scratchpad SRAM Bytes		8 K

a. There are eight RAM blocks, the last two are concatenated.

Table 2: QL1A100 Maximum Usable I/Os

Device	VCCIO Banks				Total Maximum Usable I/Os
	Bank A	Bank B	Bank C	Bank D	
110 WLCSP (10 x 11 array)	15	21	12	15	63
121 TFBGA (8 mm x 8 mm)	10	20	12	18	60
196 TFBGA (12 mm x 12 mm)	30	34	12	44	120

## Process Data

The QuickLogic ArcticLink Solution Platform is fabricated on a 0.18  $\mu\text{m}$ , six layer metal CMOS process. The core voltage is 1.8 V. The I/O voltage input tolerance and output drive can be set as 1.8 V, 2.5 V, and 3.3 V.

## Application Specific Standard Product (ASSP)

### Hi-Speed USB 2.0 OTG Controller

The on-chip Hi-Speed USB 2.0 OTG controller is a Dual-Role Device (DRD) that supports host and device functions.

The Hi-Speed USB 2.0 OTG Controller main features include:

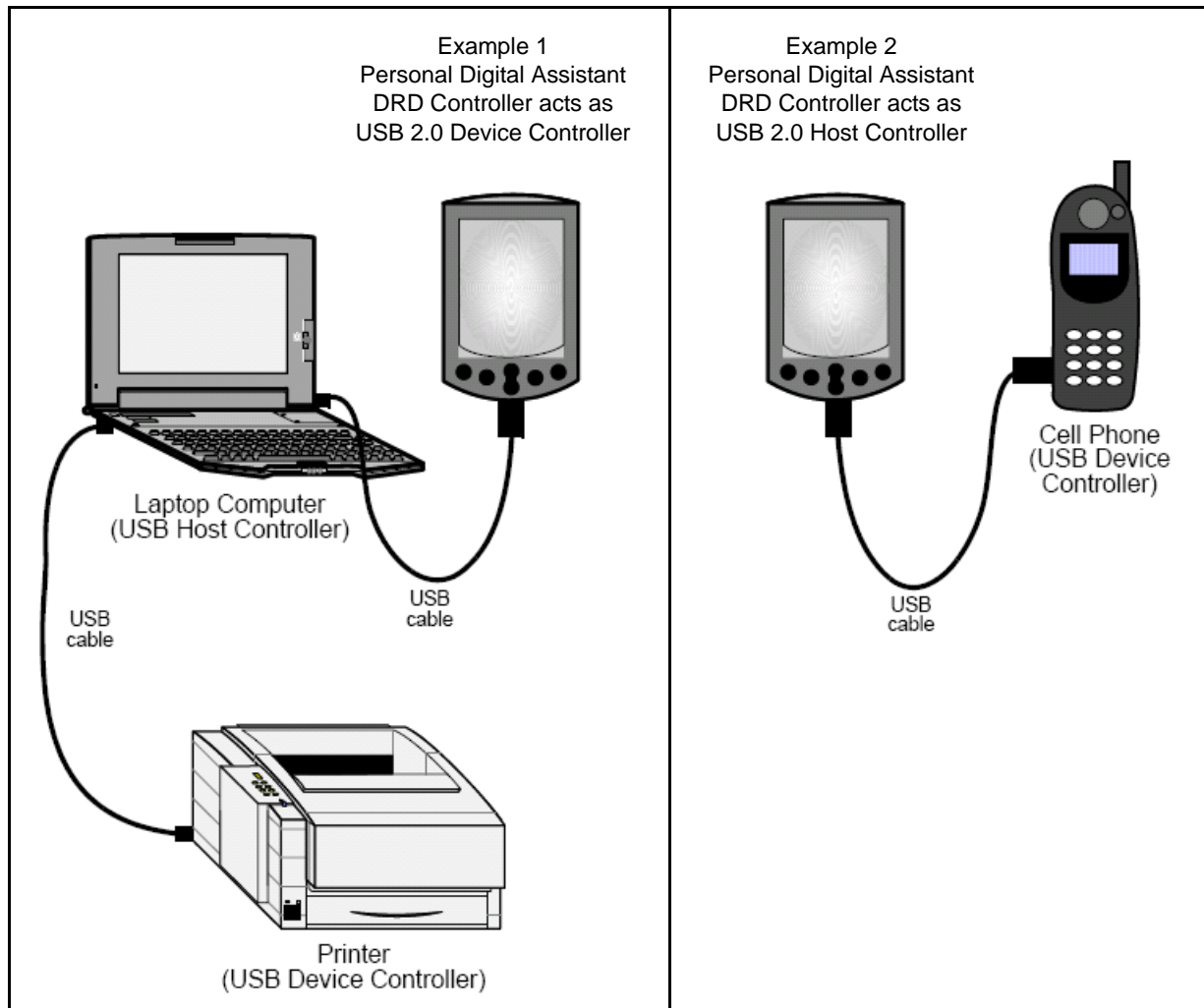
- Fully compliant with *Universal Serial Bus Specification, Revision 2.0*.
- Fully compliant with the *On-The-Go Supplement to the USB 2.0 Specification, Revision 1.0a*
- Integrated USB 2.0 OTG port capable of high-speed (HS, 480 Mbps), full-speed (FS, 12 Mbps), and low-speed (LS, 1.5 Mbps) transfers
- Integrated PHY with dedicated Internal Phase-Locked Loop (PLL) with external 12 MHz input for low EMI
- Supports both Point-to-Point and Multi-Point (root hub) applications
- Optional ULPI HS/Full-Speed USB 1.1 Shared-Pin Interface via ASSP/programmable fabric interface
- Optional I<sup>2</sup>C™ compatible serial bus for OTG control in Full-Speed USB 1.1 mode available via ASSP/programmable fabric interface
- Double-buffering scheme for improved throughput and data transfer capabilities
- Supports OTG Host Negotiation Protocol (HNP) and Session Request Protocol (SRP)
- Supports suspend and remote wake-up
- Supports external charge pump source for applications requiring higher current requirements of VBUS
- Configurable power management features
- Integrated 5.2 KB FIFO
- Supports packet-based, dynamic FIFO memory allocation, for flexible, efficient use of RAM
- Total of sixteen endpoints comprising of:
  - One fixed bidirectional control endpoint
  - One software programmable IN or OUT endpoint
  - Seven IN endpoints
  - Seven OUT endpoints

The DRD controller is optimized for the following applications and systems:

- Portable electronic devices
- Point-to-point applications (no hub, direct connection to HS, FS, or LS device)
- Multi-point applications (as an embedded USB host) to devices (hub and split support)

**Figure 1** shows typical scenarios for a Personal Digital Assistant (PDA) application. In Example 1 the laptop computer contains a USB host for the PDA and printer peripherals. In Example 2 the DRD controller in the PDA acts as the USB host for the cell phone peripheral.

Figure 1: Typical DRD Controller Applications



## USB DMA Controller

The USB DMA Controller in the USB 2.0 Controller can transfer data to and from the Fabric or the dual-port scratchpad 8 KB SRAM.

The USB 2.0 OTG Controller is software selectable to be in Slave mode or DMA mode through the use of the DMAEn bit of the GAHBCFG register. In Slave mode, data transfers to/from the USB Tx/Rx FIFOs is handled by the software driver running on the attached CPU. In DMA mode, data transfers between the USB Tx/Rx FIFOs and the 8 KB SRAM (or FPGA memory controller) is handled by the internal USB DMA Controller.

The internal USB DMA Controller translates internal DMA requests/cycles into Fast Peripheral/SRAM Interface bridge Master requests/cycles. The DMA address, transfer count, and packet count registers reside in the USB Slave Registers block. The selected channel's address is provided as input into the USB DMA Controller. The software driver sets up the transfer and the USB interrupts the processor only on transfer completion or an error condition.

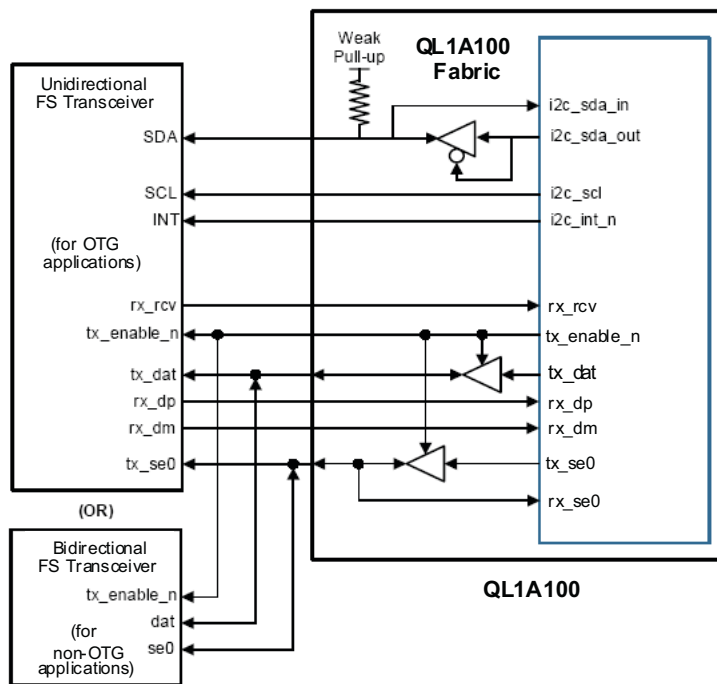
## 2-Wire Serial and ULPI to Fabric Interface

### I<sup>2</sup>C Compatible Serial Bus

I<sup>2</sup>C (Inter-Integrated Circuit) is a simple bidirectional 2-wire serial bus which enables devices to communicate directly with each other.

The I<sup>2</sup>C compatible serial bus can be used for OTG control of a Full-Speed USB 1.1 OTG Transceiver. **Figure 2** shows unidirectional and bidirectional Full-Speed USB 1.1 OTG Transceiver and optional I<sup>2</sup>C compatible serial connections. See **Table 3** for ULPI pin sharing modes.

Figure 2: USB 1.1 6-Pin Unidirectional with 2-Wire Serial for OTG and 3-Pin Bidirectional Non-OTG Full-Speed Serial Transceiver Dedicated Interface – I<sup>2</sup>C Compatible Serial Bus



The I<sup>2</sup>C compatible serial bus interface can also be used for the support of Mini USB Analog CarKit Interface CEA-936 in OTG and non-OTG configurations and is not intended for use with other devices. Refer to the targeted ULPI CarKit PHY documentation for more information regarding the use of I<sup>2</sup>C compatible serial bus interface with ULPI CarKit PHYs.

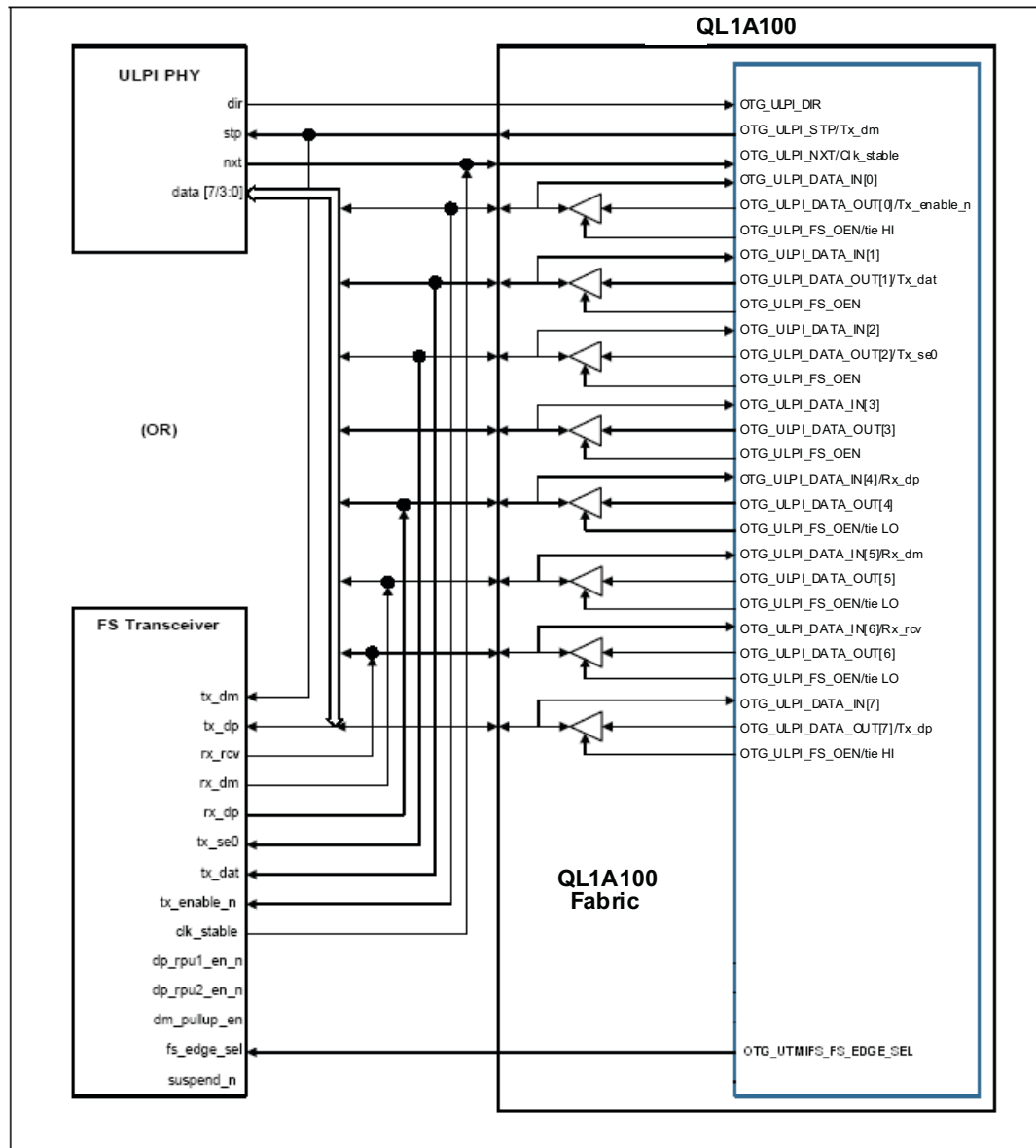
### UTMI+ Low Pin Interface (ULPI)

ULPI defines an interface between USB link controllers and the PHYs or transceivers that drive the actual bus. ULPI is designed to reduce the pin count of HS USB PHYs thus minimizing the cost and footprint of external PHY chips and reducing the pin count to the USB link controller. The available ULPI interface on the

ArcticLink Solution Platform is intended for connecting an external ULPI CarKit PHY or implementing PHY-less chip-to-chip communication. Use the integrated HS PHY on the ArcticLink Solution Platform for systems that do not require ULPI CarKit or PHY-less chip-to-chip communication support.

**Figure 3** shows the QL1A100 device connected to a ULPI PHY or Full-Speed USB 1.1 OTG Serial Transceiver.

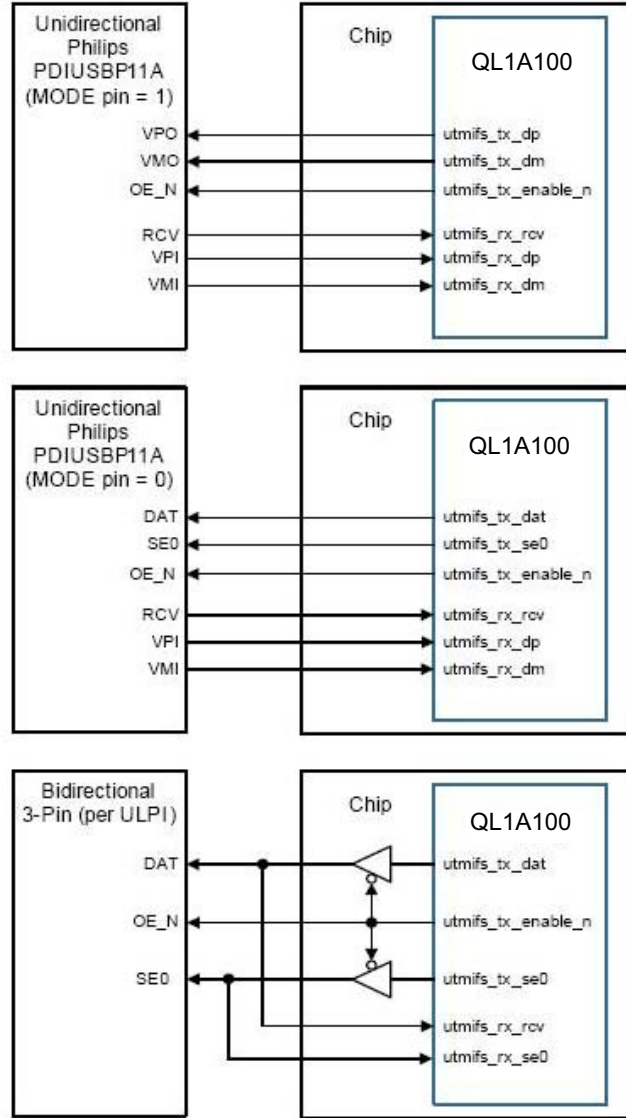
Figure 3: ULPI HS PHY/USB 1.1 Serial Transceiver Shared-Pin Interface



**NOTE:** Not all FsLs serial pins are required for all FS Transceivers or FS Hubs, it is shown only for reference and connectivity purposes. The ULPI and FS clocks pins are shared (not shown), external clock switching may be required. OTG and I<sup>2</sup>C compatible serial pins are not shared (not shown).

Figure 4 shows sample FS/LS serial connections for a Philips PDIUSBP11A USB Transceiver and 3-pin configuration as part of the ULPI (optional) FsLs Serial support.

Figure 4: Philips PDIUSBP11A and ULPI 3-Pin Transceiver Connections



ULPI Vendor Control access is provided in the ArcticLink Solution Platform is described in Chapter 7 of the *ArcticLink Solution Platform User Manual*. Software can program the PHY Vendor Control register which is translated as a register read/write command in ULPI for ULPI PHY register access.

## ULPI Modes of Operation

The ArcticLink Solution Platform supports ULPI interface (8-bit SDR, 6-pin FsLs Serial, 3-pin FsLs Serial and Carkit) as shown in **Table 3**.

Table 3: OTG ULPI Signal Modes

ULPI Synchronous HS Mode (8-bit SDR)	FS Serial Mode		Carkit Mode
	6-Pin	3-Pin	
ULPI_DATA[0]	Tx_enable	Tx_enable	Txd
ULPI_DATA[1]	Tx_dat	dat	Rxd
ULPI_DATA[2]	Tx_se0	se0	Reserved
ULPI_DATA[3]	Interrupt	Interrupt	Interrupt
ULPI_DATA[4]	Rx_dp	Unused	Unused
ULPI_DATA[5]	Rx_dm	Unused	Unused
ULPI_DATA[6]	Rx_rcv	Unused	Unused
ULPI_DATA[7]	Tx_dp	Unused	Unused
ULPI_CLK (60 MHz)	Clk (48 MHz)	Clk (48 MHz)	Unused
ULPI_DIR	Dir	Dir	Dir
ULPI_NXT	Nxt	Nxt	Nxt
ULPI_STP	Stp/Tx_dm	Stp	Stp
OTG_ULPI_FS_OEN	OTG_ULPI_FS_OEN	OTG_ULPI_FS_OEN	OTG_ULPI_FS_OEN
Unused	OTG_UTMIFS_RX_SE0	OTG_UTMIFS_RX_SE0	Unused

The ArcticLink Solution Platform supports the optional FsLs Serial mode as per the ULPI specification for ULPI PHYs with FsLs support or standalone FS transceivers both using a shared pin ULPI interface as shown in **Figure 3** on page 6.

**NOTE:** The ArcticLink Solution Platform does not support FsLs Serial modes of ULPI PHYs which require FsLs Serial modes to operate on frequencies other than 48 MHz. The ArcticLink Solution Platform also requires PHYs to internally switch the ULPI Clock output to 60 MHz and 48 MHz for ULPI and FsLs modes respectively.

Programming FsLs Serial Mode for standalone FS transceivers and integrated ULPI PHYs:

- The mode is selected by setting the GUSBCFG.ULPIFsLs, GUSBCFG.PHYSel, and GUSBCFG.ULPI\_UTMI\_Sel registers, and must be set before any USB event (see the *ArcticLink Solution Platform User Manual* for details)
- In ULPI FsLs Host mode, the application must program HCFG.FSLSPclksel to “01” so the internal clock is running at 48 MHz
- In ULPI FsLs Device mode, the application must program DCFG.DevSpd to “11” to denote the maximum speed the ArcticLink Solution Platform can support in this mode
- To select the 6-pin FsLs Serial mode, the application must program the GUSBCFG.FSIntf to “0”
- To select the 3-pin FsLs Serial mode, the application must program the GUSBCFG.FSIntf to “1”

## ULPI Interface Initialization

After the ULPI is reset and the PHY is initialized, depending on how the registers are set, ULPI or 6-pin FsLs serial or 3-pin FsLs serial modes are enabled.

For FsLs Serial modes of ULPI PHYs, “Interface Control” register is set.

During 6-pin full-speed/low-speed Serial mode, the ulpi data bus is mapped to signal definitions as shown in **Table 3** under the “Serial Mode 6-pin” column.

During 3-pin full-speed/low-speed Serial mode, the ulpi data bus is mapped to signal definitions as shown in **Table 3** under the “Serial Mode 3-pin” column.

**NOTE:** The following signals are provided and not pin shared but may be required for some FS transceiver applications:

- OTG\_utmifs\_rx\_se0: UTMI FS Serial SE0 assertion received
- OTG\_utmifs\_fs\_edge\_sel: UTMI FS selects low/full-speed slew rate

**NOTE:** OTG\_ULPI\_CLK is pin shared with ULPI and FsLs Serial mode for 60 MHz and 48 MHz interface clocks respectively.

For FsLs Serial modes of ULPI PHYs, to exit Serial mode, the ArcticLink Solution Platform receives an interrupt from the PHY, and the PHY registers are updated.

## Carkit Support in Fabric

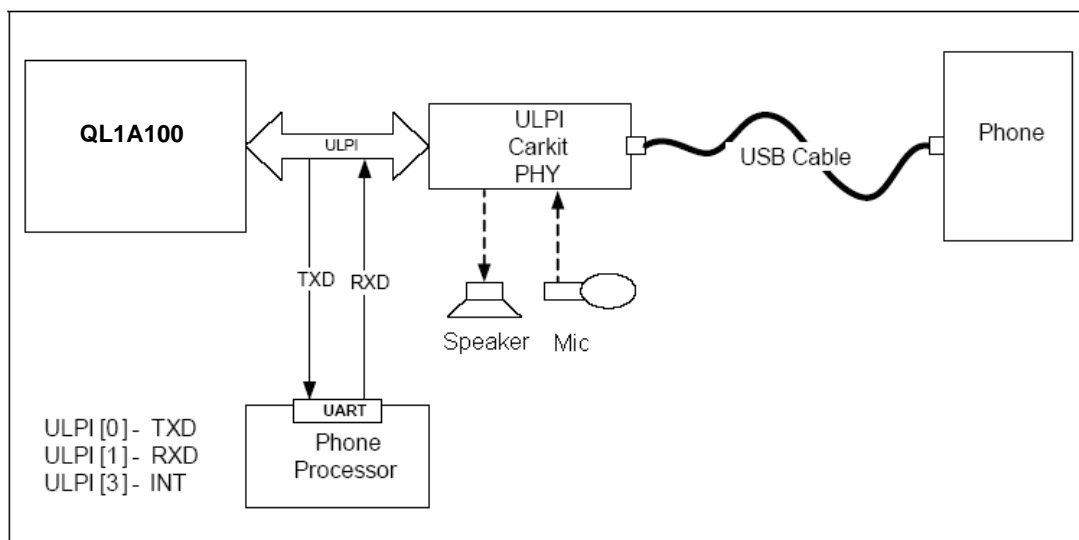
Typically, USB-ULPI Carkit PHYs support three main modes: HS USB, UART and Audio.

The ArcticLink Solution Platform Carkit support fulfills the USB responsibility of multiplexing the ULPI data lines between UART and USB-ULPI modes, and receiving Carkit interrupts from the PHY.

For a more complete Carkit implementation using the ArcticLink Solution Platform, a Carkit or Phone requires additional elements such as Carkit logic or processor blocks for configuration and control, UARTs, and separate I/Os for Speaker and Mic.

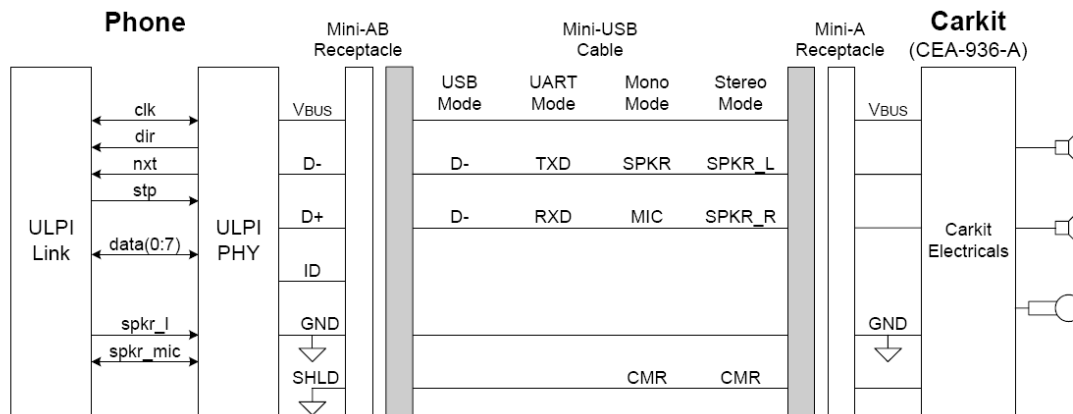
**Figure 5** shows the ArcticLink Solution Platform in an in-dash Carkit.

Figure 5: ArcticLink Solution Platform in an In-Dash Carkit Application Block Diagram



The **Figure 6** shows the basic architecture of the ULPI Carkit interface, and the allowed signaling modes.

Figure 6: ULPI Carkit Interface Architecture



The Carkit application for the ArcticLink Solution Platform can be a cell phone or Carkit. For Carkit applications, the ULPI PHY resistively pulls down the ID. The ULPI PHY on a cell phone can monitor the resistive pull-down to detect a Carkit connection.

For external ULPI Carkit PHY applications, in USB mode it should operate as a standard HS USB-ULPI capable interface. The Speaker (SPK) and Microphone (MIC) are analog circuits.

The ULPI and UART are digital circuits that share the ULPI data bus as shown in **Figure 6** and as mentioned in **Table 3**, column Carkit Mode. ULPI or UART modes can be selected via the software application. The selection is accomplished by setting the Carkit Mode bit in the Interface Control register and setting the TxdEn and RxdEn bits in the Carkit Control register of the ULPI PHY. Software can access ULPI PHY internal registers using register read/writes to the ArcticLink Solution Platform's vendor control access.

When the application selects ULPI or UART interfaces the Carkit interrupts are received by the ArcticLink Solution Platform through RXCMD, bit[7] or ulpi\_data[3] respectively.

## Full-Speed USB 1.1 Hub Support in Fabric

An optional Full-Speed USB 1.1 Hub can be implemented within the ArcticLink Solution Platform Fabric in lieu of the optional single Full-Speed USB 1.1 port. The optional hub connects to the single Full-Speed USB 1.1 serial upstream port and in turn provides multiple downstream ports that can be routed to various GPIOs. Note that an external 48 MHz source clock is required as input to the ArcticLink Solution Platform for both the single and multi port Full-Speed USB 1.1 serial implementations.

## USB Charge Pump (External)

A charge pump is necessary for USB Host or USB OTG A-device mode implementations to supply a 5 V source to attached devices.

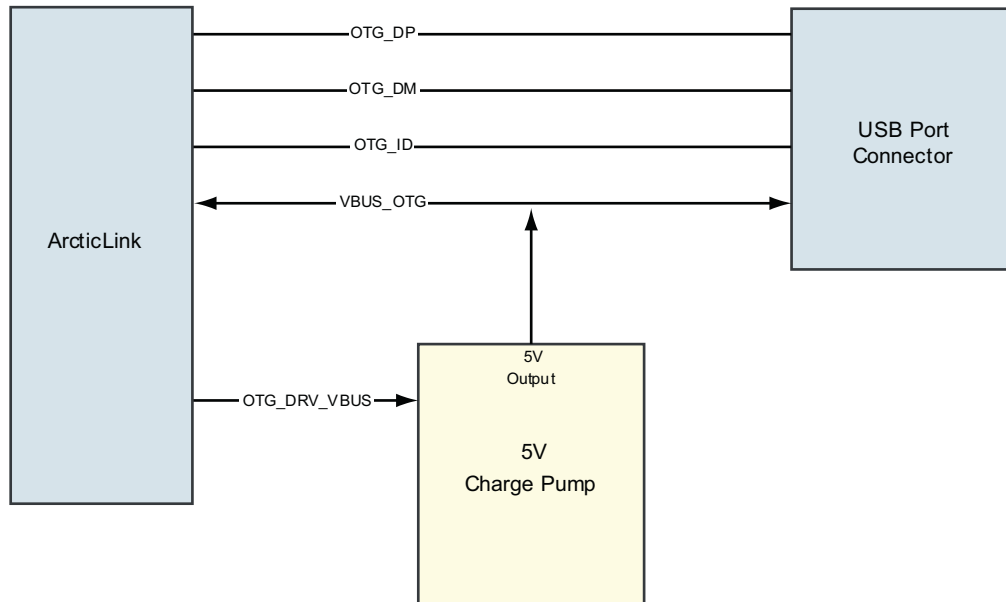
A large selection of charge pumps are available and should be selected by the designer depending on system requirements such as:

- +4.8 V to +5.25V OTG-compatible output on VBUS.
- 8 mA (minimum for OTG applications), 100 mA (minimum for low-powered Host applications), 500 mA (recommended) output current, depending on the type of devices to be powered by the charge pump.

Consult the selected charge pump data sheet for details on its connectivity.

**Figure 7** illustrates a typical external charge pump implementation connected to the ArcticLink Solution Platform and a USB connector.

Figure 7: USB Charge Pump Connectivity Block Diagram



## SD/SDIO/MMC/CE-ATA Host Controller

The SD/SDIO/MMC/CE-ATA Host Controller is compliant with *SD Host Controller Standard Specification, Version 2.0* and supports MMC Specification, Version 4.1.

The SD/SDIO/MMC/CE-ATA Host Controller main features include:

- Supports MMC 4.1
- Supports clock rate up to 52 MHz
- Supports SD and SDIO
- Supports I/O commands 52 and 53
- Supports 1-bit, 4-bit and 8-bit data modes
- Supports SDIO device interrupt in 1-bit, 4-bit, and 8-bit modes
- Supports block size up to 512 bytes
- Dynamic Buffer Management to increase data throughput
- Available DREQ signal for Marvell® PXA processor to improve processor DMA performance

The CE-ATA mode SD/SDIO/MMC/CE-ATA Host Controller is compliant with *CE-ATA Digital Protocol, Revision 1.1RC* and based on the *SD Host Controller Standard Specification, Version 2.0*.

The CE-ATA mode main features include:

- Supports clock rate up to 52 MHz
- Supports CE-ATA commands 39, 60, and 61
- Supports CE-ATA Command Completion Interrupt from device to host
- Supports CE-ATA Command Completion Signal Disable protocol generation
- Supports 1-bit, 4-bit and 8-bit data modes
- Supports 512-byte block sizes
- Dynamic Buffer Management to increase data throughput
- Available DREQ signal for Marvell PXA processor to improve processor DMA performance

## 8 KB On-Chip Scratchpad Memory

A scratchpad memory is provided on-chip for temporary storage as well as to facilitate data flow between the USB controller and external host processor. The scratchpad is dual-ported with one port connected to the internal bus closely coupled with the Hi-Speed USB 2.0 OTG Controller, while the other port is connected to the fabric master SRAM interface and source clock. This enables the internal bus logic to run at a much higher clock frequency independent of the FPGA design frequency.

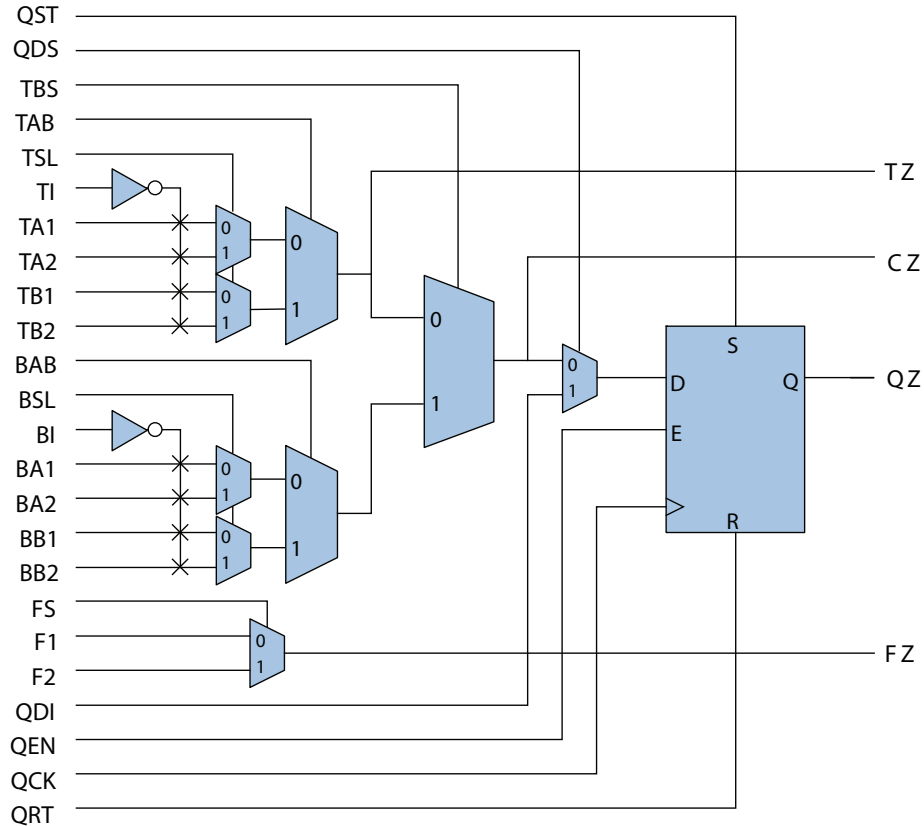
## Fast Peripheral/SRAM Interface Bridge for FPGA Memory Controller

To improve performance, external bus mastering can be achieved through the on-chip Fast Peripheral/SRAM Interface bridge for systems where bus mastering is an option. This bridge provides a way for the internal DMA engine in the Hi-Speed USB 2.0 OTG Controller to directly access external memory through a memory controller implemented in the FPGA. This bridge provides a clock domain crossing to allow the internal bus clock to run independently of the FPGA memory controller clock.

## Programmable Fabric Architectural Overview

The QuickLogic ArcticLink Solution Platform logic cell structure presented in **Figure 8** is a single register, multiplexer-based logic cell. It is designed for wide fan-in and multiple, simultaneous output functions. The cell fits a wide range of functions with up to 24 simultaneous inputs (including register control lines), and four outputs (three combinatorial and one registered). The high logic capacity and fan-in of the logic cell accommodates many user functions with a single level of logic delay.

Figure 8: Logic Cell

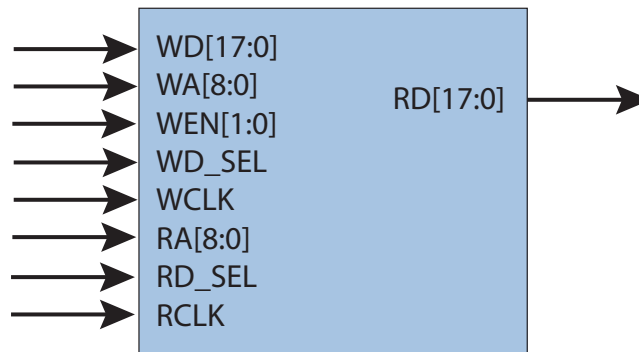


## RAM Modules

The ArcticLink Solution Platform has 4-Kbit (4,608 bits) RAM blocks which are used primarily as buffers and FIFOs to significantly improve system performance. The RAM features include:

- Independently configurable read and write data bus widths
- Independent read and write clocks
- Horizontal and vertical concatenation
- Write byte enables
- Selectable pipelined or non-pipelined read data
- Ability to generate true dual-port RAMs through concatenation with completely independent read/write ports and clock domains

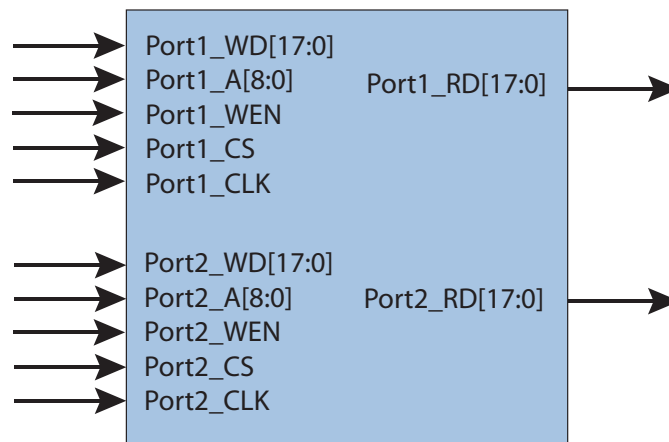
Figure 9: 4-Kbit Dual-Port RAM Block



## True Dual-Port RAM

The ArcticLink Solution Platform dual-port RAM modules can also be concatenated to generate true dual-port RAMs. The true dual-port RAM module's Port1 and Port2 have completely independent read and write ports, and separate read and write clocks. This allows Port1 and Port2 to have different data widths and clock domains. **Figure 10** shows an example of a 512x18 true dual-port RAM.

Figure 10: 512x18 True Dual-Port RAM Block



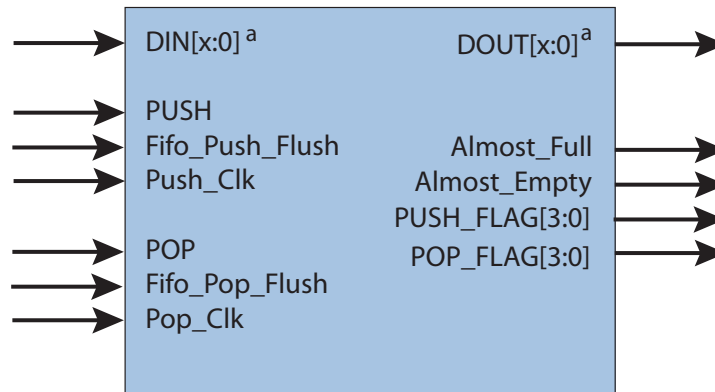
## Embedded FIFO Controllers

Every RAM block can be implemented as a synchronous or asynchronous FIFO. There are built-in FIFO controllers that allow for varying depths and widths without requiring programmable fabric resources.

The ArcticLink Solution Platform FIFO controller features include:

- x9, x18 and x36 data bus widths
- Independent PUSH and POP clocks
- Independent programmable data width on PUSH and POP sides
- Configurable synchronous or asynchronous FIFO operation
- 4-bit PUSH and POP level indicators to provide FIFO status outputs for each port
- Pipelined read data to improve timing

Figure 11: FIFO Module



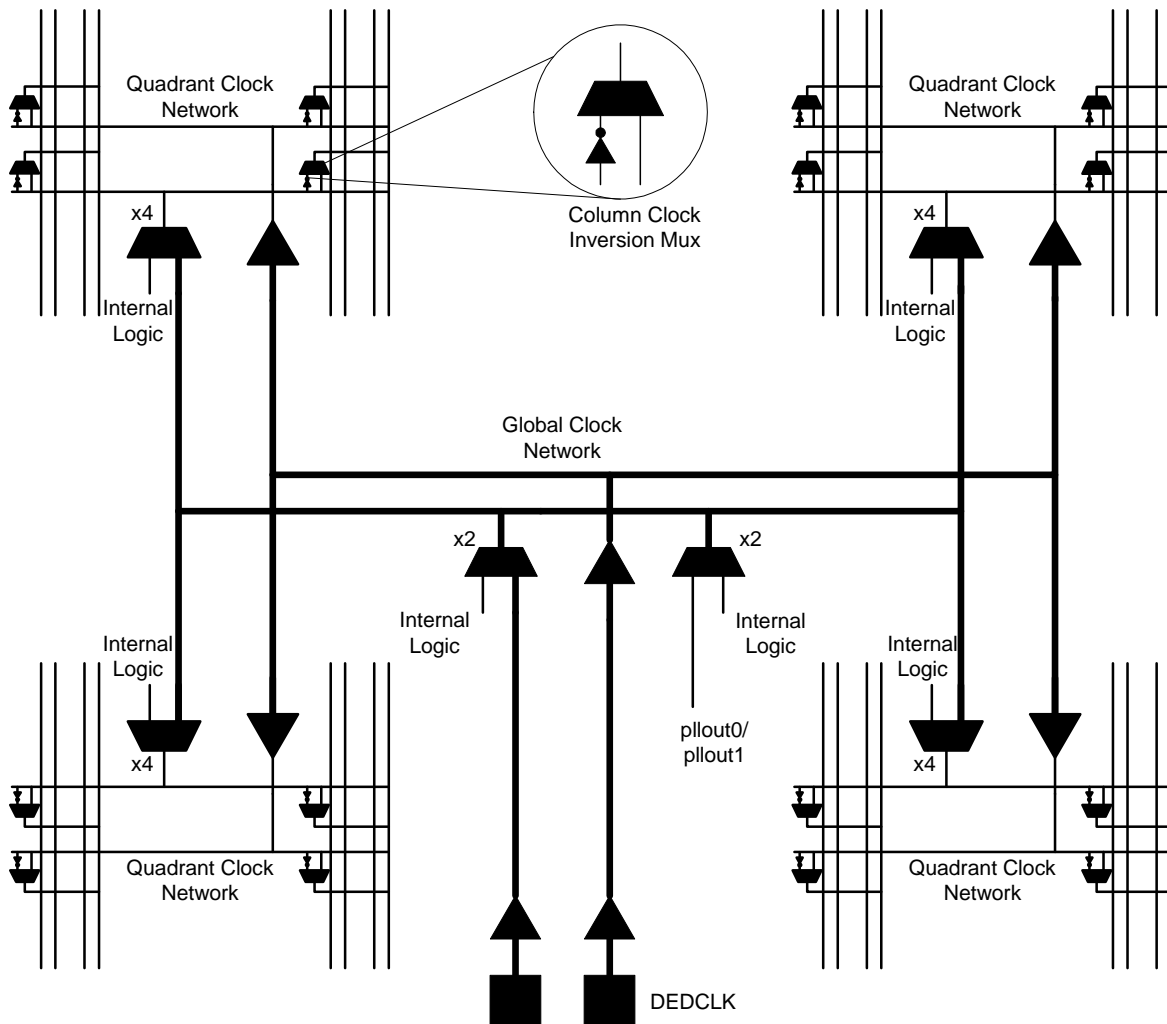
a.  $x = \{1,2,3,\dots,35\}$ .

## Distributed Clock Networks

The ArcticLink Solution Platform clock network architecture consists of a 2-level H-tree network as shown in **Figure 12**. The first level spans from the clock pad, via the global clock network multiplexers (located in the middle of the chip) and ends at the center of each quadrant. The second level spans from the center of the quadrant, via the column clock buffer and ends at every logic cell in that quadrant.

There are five global clock networks per chip and five quad clock networks per quadrant, thus providing up to 20 total quad clock networks per chip. All global clock networks can drive the quadrant clock networks, which in turn drive RAM clock inputs, the reset, and enable of I/O registers, as well as any input port of the logic cell. The column clock buffers in the quadrant clock networks also have the ability to invert the signals as well.

Figure 12: Global Clock Architecture



The ArcticLink Solution Platform has three clock pads, but five global clock networks. Of the five global clock networks, one is a dedicated network that directly feeds the quadrant quad clock network – this global network is referred to as the dedicated fast clock. Of the remaining four global clock networks, two can be driven either by a clock pad or an internally generated signal. The fourth and fifth global clock networks do not have the option to be driven by a clock pad. They can only be driven by an internally generated signal or by the CCM outputs – pllout0 or pllout1.

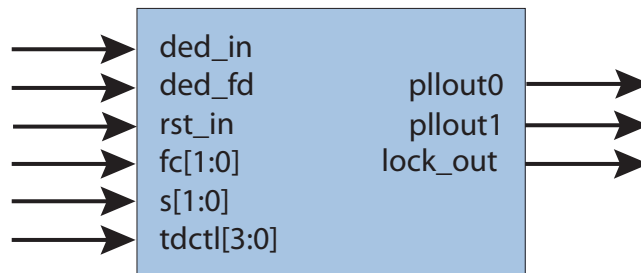
It is important to note that the select lines for the global clock and quad-net muxes are static signals and cannot be changed dynamically during device operation. The selects are automatically configured by the software depending on designer's input.

## Configurable Clock Manager

The QuickLogic ArcticLink 110-ball WLCSP and 196-ball TFBGA devices have one CCM. The CCM features include:

- Input frequency range from 25 MHz to 200 MHz
- Output frequency range from 25 MHz to 200 MHz
- Output jitter is less than 200 ps peak-to-peak
- Two outputs: pullout0 (with 0° phase shift), and pullout1 (with an option of 0°, 90°, 180°, or 270° phase shift plus a programmable delay).
- Programmable delay allows delays up to 2.5 ns at 250 ps intervals
- Output frequency lock time in less than 10  $\mu$ s

Figure 13: Configurable Clock Manager



The reset signal can be routed from a clock pad or generated using internal logic. The lock\_out signal can be routed to internal logic and/or an output pad. CCM clock outputs can drive the global clock networks, as well as any general purpose I/O pin. Once the CCM has synchronized the output clock to the incoming clock, the lock\_out signal will be asserted to indicate that the output clock is valid. Lock detection requires at least 10  $\mu$ s after reset to assert lock\_out. The ArcticLink Solution Platform CCM has three modes of operation, based on the input frequency and desired output frequency. **Table 4** indicates the features of each mode.

Table 4: CCM PLL Mode Frequencies

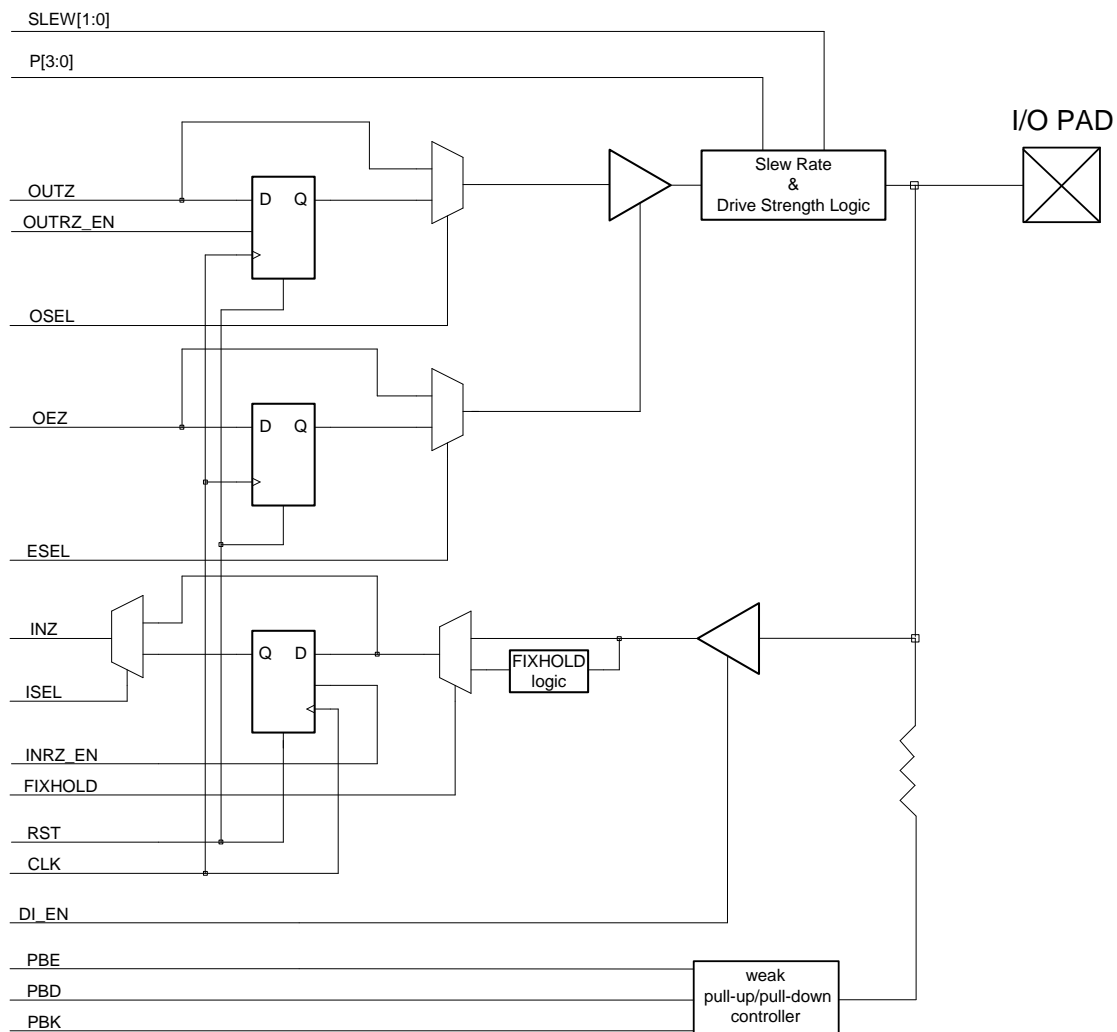
Output Frequency	Input Frequency Range	Output Frequency Range	PLL Mode
x1	25 MHz to 200 MHz	25 MHz to 200 MHz	PLL_MULT1
x2	15 MHz to 100 MHz	30 MHz to 200 MHz	PLL_MULT2
x4	10 MHz to 50 MHz	40 MHz to 200 MHz	PLL_MULT4

## General Purpose Input Output (GPIO) Cell Structure

The GPIO features include:

- Direct or registered input with input path select
- Direct or registered output with output path select
- Direct or registered output enable with OE path select
- Input buffer enable to reduce power
- Programmable weak keeper, programmable pull-up/pull-down control
- Programmable drive strength
- Configurable slew rate
- Support for JTAG boundary scan

Figure 14: GPIO Cell



With bidirectional I/O pins and global clock input pins, the ArcticLink Solution Platform maximizes I/O performance, functionality, and flexibility. All input and I/O pins are 1.8 V, 2.5 V, and 3.3 V tolerant and comply with the specific I/O standard selected. For single-ended I/O standards, the corresponding VCCIO bank input specifies the input tolerance and the output drive voltage. Drive strength and slew rate are configured for an entire bank. Weak keeper, pull-up, and pull-down functions can be configured for individual I/O. The default configuration for QuickLogic QuickWorks® software has the drive strength set to 4 and the slew rate set to wow.

## DDRIO Cell Structure

The QuickLogic ArcticLink 196-ball device supports DDRIOs, which allows clocking data on both the positive and negative clock edges. All ArcticLink devices have one I/O bank (Bank D) that can be configured in either a GPIO bank or a DDRIO mode. When bank D is configured to DDRIO mode, it is further divided into DDRIO sets. Each set contains 12 I/Os, which include 8 DQs, 1 DQM, 1 DQS, 1 DQCK\_N and 1 DQCK\_P (for the differential clocks, refer to [Table 5](#)).

Figure 15: DDRIO Block Diagram

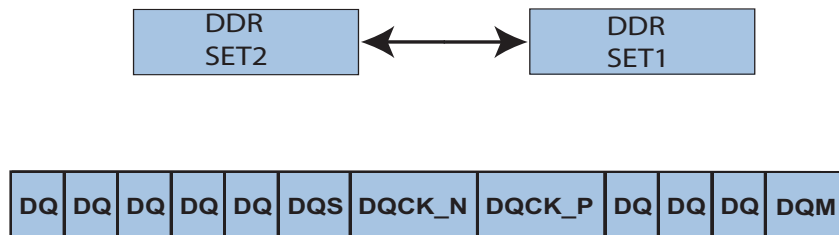


Table 5: Available DDR Sets

Device	Package	Number of DDR Sets
QL1A100	PT196	2
	PM121	0
	CSP110	0

## DDRIO in GPIO Mode

DDR in GPIO mode features include programmable I/O standards via the VCCIO input pins (1.8V LVCMOS, 2.5V LVCMOS, and 3.3V LVTTTL).

**NOTE:** The DDR-capable I/Os in bank D on the QL1A100 device in the 196-ball package (i.e., the I/Os with labels other than GPIO(D)) do not support PCI. For PCI support in the 196-ball package, use only single-function (non-DDR) pins labeled as GPIO(A), GPIO(B), GPIO(C), and GPIO(D). Furthermore, for the QL1A100 device in the 121-ball package, I/Os in bank D labeled as GPIO(D) on pins A8, B6, B7, B8, C7 and C8 also do not support PCI. When using the 121-ball package, any other GPIO(D:A) pins can be used for PCI except the 6 pins specifically identified above.

## Very Low Power (VLP) Mode

The QuickLogic ArcticLink Solution Platform has a unique feature, referred to as VLP mode, which reduces power consumption by placing the device in standby. Specifically, VLP mode can bring the programmable fabric standby current down to less than 10  $\mu\text{A}$  at room temperature when no incoming signals are toggled. VLP mode is controlled by the VLP pin. The VLP pin is active low, so VLP mode is activated by pulling the VLP pin to ground. Conversely, the VLP pin must be pulled to 3.3 V for normal operation.

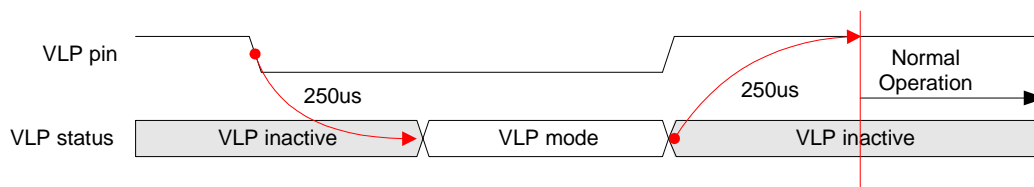
When the ArcticLink Solution Platform goes into VLP mode, the following occurs:

- All register values in the programmable fabric and GPIO are preserved
- All RAM cell data is retained
- The outputs from all GPIO to the internal logic are tied to a weak '1'
- GPIO outputs drive the previous values
- GPIO output enables retain the previous values
- Clock pad inputs are gated
- The CCM is held in the reset state

The entire operation from normal mode to VLP mode requires 250  $\mu\text{s}$  (300  $\mu\text{s}$  maximum). As mentioned in the VLP behavioral description above, the output of the GPIO to the internal logic is a weak '1'. Therefore, to preserve data retention GPIO should not be used for a set, reset, or clock signal.

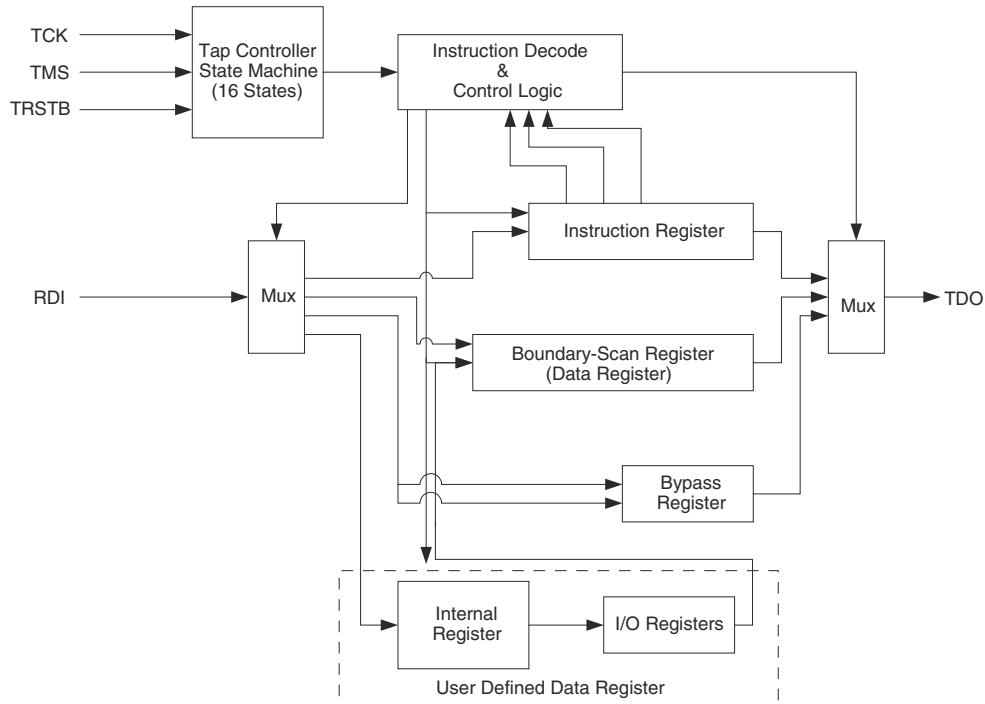
As the Solution Platform exits out of VLP mode, the data from the registers, RAM, and GPIO will be used to recover the functionality of the device. Furthermore, since the CCM is in a reset state during VLP mode, it will have to re-acquire the correct output signals before asserting lock\_out. The time required to go from VLP mode to normal operation is 250  $\mu\text{s}$  (300  $\mu\text{s}$  maximum). **Figure 16** displays the delays associated with entering and exiting VLP mode.

Figure 16: Typical VLP Mode Timing



## Joint Test Access Group (JTAG) Information

Figure 17: JTAG Block Diagram



QuickLogic's ArcticLink solution platform complies with IEEE standard 1149.1, the Standard Test Access Port and Boundary Scan Architecture (see the Note following the Sample/Preload Instruction description). The JTAG boundary scan test methodology allows complete observation and control of the boundary pins of a JTAG-compatible device through JTAG software. A Test Access Port (TAP) controller works in concert with the Instruction Register (IR), which allow users to run three required tests along with several user-defined tests. JTAG tests allow users to reduce system debug time, reuse test platforms and tools, and reuse subsystem tests for comprehensive verification of higher level system elements.

The 1149.1 standard requires the following three tests:

- **Extest Instruction.** The Extest Instruction performs a printed circuit board (PCB) interconnect test. This test places a device into an external boundary test mode, selecting the boundary scan register to be connected between the TAP Test Data In (TDI) and Test Data Out (TDO) pins. Boundary scan cells are preloaded with test patterns (through the Sample/Preload Instruction), and input boundary cells capture the input data for analysis.
- **Sample/Preload Instruction.** The Sample/Preload Instruction allows a device to remain in its functional mode, while selecting the boundary scan register to be connected between the TDI and TDO pins. For this test, the boundary scan register can be accessed through a data scan operation, allowing users to sample the functional data entering and leaving the device.

**NOTE:** The ULPI and CE-ATA interface pins are multi-function pins and shared with the Fabric GPIO cells. If these pins are selected for use as ULPI or CE-ATA I/Os, the Sample/Preload Instruction cannot be used with the ArcticLink solution platform.

- **Bypass Instruction.** The Bypass Instruction allows data to skip a device boundary scan entirely, so the data passes through the bypass register. The Bypass instruction allows users to test a device without passing through other devices. The bypass register is connected between the TDI and TDO pins, allowing serial data to be transferred through a device without affecting the operation of the device.

## JTAG BSDL Support

- Boundary Scan Description Language (BSDL)
- Machine-readable data for test equipment to generate testing vectors and software
- BSDL files available for all device/package combinations from QuickLogic
- Extensive industry support available and ATVG (Automatic Test Vector Generation)

## Electrical Specifications

### DC Characteristics

The DC Specifications are provided in **Table 6** through **Table 10**.

Table 6: Absolute Maximum Ratings

Parameter	Value	Parameter	Value
VCC, VCCP_OTG, and CCM_VCC Voltage	-0.5 V to 2.2 V	Latch-up Immunity	±100 mA
VCCIO, VCCA_OTG, and VCCIO_ASSP Voltage	-0.5 V to 4.0 V	ESD Pad Protection	2 kV
VREF Voltage	-0.5 V to 2.0 V	ESD Pad Protection (USB D+, D-, ID, VBUS_OTG)	8 kV
Input Voltage VBUS_OTG, OTG_DP, and OTG_DM	-0.5 V to 5.0 V	Leaded Package Storage Temperature	-65° C to + 150° C
Input Voltage All other I/Os	-0.5 V to 4.0 V	Laminate Package (BGA) Storage Temperature	-55° C to + 125° C

Table 7: Recommended Operating Range

Symbol	Parameter	Industrial		Commercial		Unit
		Min.	Max.	Min.	Max.	
VCC, VCCP_OTG and CCM_VCC	Supply voltage	1.71	1.89	1.71	1.89	V
VCCIO and VCCIO_ASSP	I/O input tolerance voltage	1.71	3.60	1.71	3.60	V
TJ	Junction temperature	-40	100	0	85	°C
VCCA_OTG	USB OTG PHY I/O input tolerance voltage	3.0	3.6	3.0	3.6	V

Table 8: Recommended Power Supply Ripple Noise

Symbol	Parameter	Conditions	Min.	Max.	Unit
VCC	Digital Supply Voltage	ALL	-50	+50	mV
VCCP_OTG and VCCA_OTG	Analog Supply Voltage for USB OTG core	<4 MHz	-10	+10	mV
		>4 MHz	-50	+50	mV
		<160 MHz	-50	+50	mV
CCMVCC	Analog Supply Voltage for the Fabric	<4 MHz	-10	+10	mV
		>4 MHz	-30	+30	mV
		<160 MHz	-30	+30	mV

Table 9: DC Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$I_I$	I or I/O Input Leakage Current	$V_I = V_{CCIO}$ or GND	-	-	1	$\mu A$
$I_{OZ}$	3-State Output Leakage Current	$V_I = V_{CCIO}$ or GND	-	-	1	$\mu A$
$C_I$	I/O Input Capacitance	$V_{CCIO} = 3.6 V$	-	-	10	pF
$C_{CLOCK}$	Clock Input Capacitance	$V_{CCIO} = 3.6 V$	-	-	10	pF
$I_{REF}$	Quiescent Current on INREF	-	-	-	5	$\mu A$
$I_{PD}$	Current on programmable pull-down	$V_{CCIO} = 3.6 V$	-200	-	-50	$\mu A$
		$V_{CCIO} = 2.75 V$	-150	-	-25	$\mu A$
		$V_{CCIO} = 1.89 V$	-100	-	-10	$\mu A$
$I_{PU}$	Current on programmable pull-up	$V_{CCIO} = 3.6 V$	50	-	200	$\mu A$
		$V_{CCIO} = 2.75 V$	25	-	150	$\mu A$
		$V_{CCIO} = 1.89 V$	10	-	100	$\mu A$
$I_{VLP}$	Quiescent Current on VLP pin	$VLP=3.3$	-	1	10	$\mu A$
$I_{CCM}$	Quiescent Current on CCMVCC	$VCC=1.89 V$	-	1	10	$\mu A$
$I_{VCC}$	Quiescent Current	$VLP=GND$	-	5	40	$\mu A$
		$VLP=3.3V$	-	40	100	$\mu A$
$I_{VCCIO}$	Quiescent Current on VCCIO	$V_{CCIO} = 3.6 V$	-	2	10	$\mu A$
		$V_{CCIO} = 2.75 V$	-	2	10	$\mu A$
		$V_{CCIO} = 1.89 V$	-	2	10	$\mu A$

Table 10: DC Input and Output Levels<sup>a</sup>

Symbol	INREF		$V_{IL}$		$V_{IH}$		$V_{OL}$	$V_{OH}$	$I_{OL}$	$I_{OH}$
	$V_{MIN}$	$V_{MAX}$	$V_{MIN}$	$V_{MAX}$	$V_{MIN}$	$V_{MAX}$	$V_{MAX}$	$V_{MIN}$	mA	mA
LVTTL	n/a	n/a	-0.3	0.8	2.2	$V_{CCIO} + 0.3$	0.4	2.4	2.0	-2.0
LVC MOS2	n/a	n/a	-0.3	0.7	1.7	$V_{CCIO} + 0.3$	0.7	1.7	2.0	-2.0
LVC MOS18	n/a	n/a	-0.3	0.63	1.2	$V_{CCIO} + 0.3$	0.7	1.7	2.0	-2.0
GTL+	0.88	1.12	-0.3	$INREF - 0.2$	$INREF + 0.2$	$V_{CCIO} + 0.3$	0.6	n/a	40	n/a
PCI	n/a	n/a	-0.3	$0.3 \times V_{CCIO}$	$0.6 \times V_{CCIO}$	$V_{CCIO} + 0.5$	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	1.5	-0.5
SSTL2	1.15	1.35	-0.3	$INREF - 0.18$	$INREF + 0.18$	$V_{CCIO} + 0.3$	0.74	1.76	7.6	-7.6
SSTL3	1.3	1.7	-0.3	$INREF - 0.2$	$INREF + 0.2$	$V_{CCIO} + 0.3$	1.10	1.90	8	-8

a. The data provided in **Table 10** represents the JEDEC and PCI specification. The QuickLogic Solution Platform either meet or exceed these requirements.

Figure 18 and Figure 19 illustrate quiescent current for QL1A100 with VLP = 0 V and 3.3 V.

Figure 18: Quiescent Current for QL1A100 with VLP = 0 V

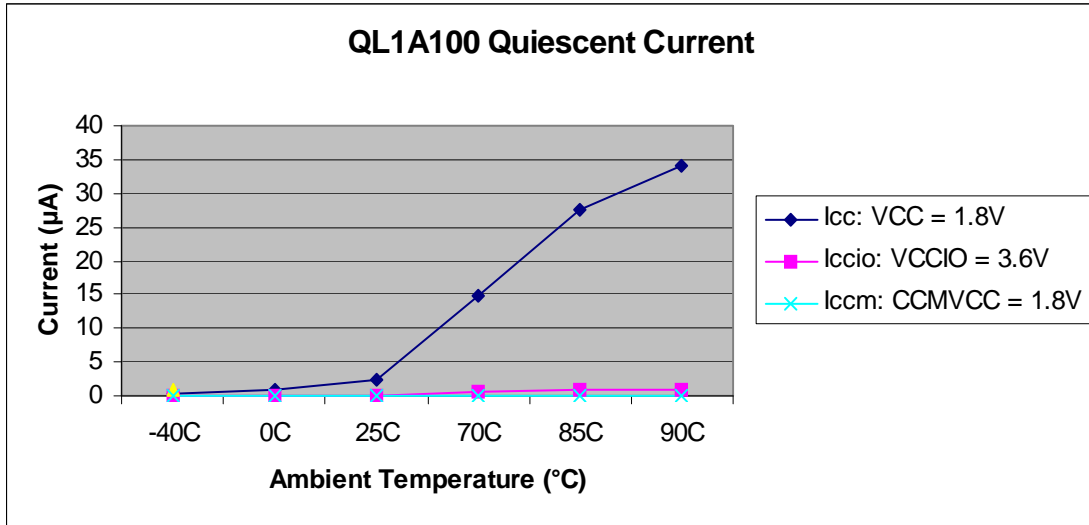
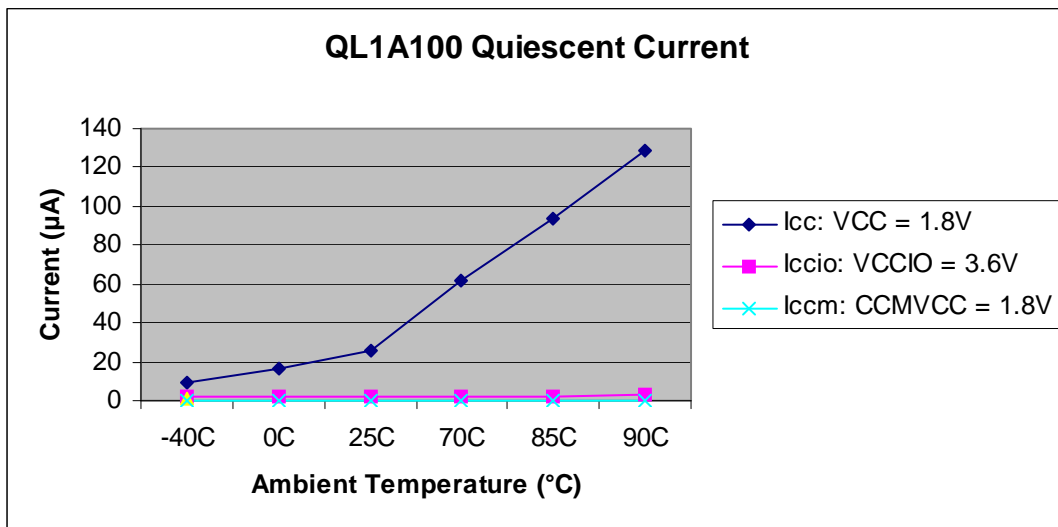


Figure 19: Quiescent Current for QL1A100 with VLP = 3.3 V



## AC Characteristics

See the *PolarPro Family Data Sheet* at [http://www.quicklogic.com/images/polarpro\\_DS.pdf](http://www.quicklogic.com/images/polarpro_DS.pdf) for AC specifications for programmable fabric. As an exception, see **Table 11** for programmable fabric clock tree timing specific to the ArcticLink Solution Platform. The following AC timing numbers are for worst case Commercial (T = 85°C Junction, V = 1.71V), and worst case Industrial (T = 100°C Junction, V = 1.71V) conditions.

## Programmable Fabric Clock Tree Timing

Table 11 shows the clock tree delays in the programmable fabric.

Table 11: Tree Clock Delay

Clock Segment	Parameter	Commercial		Industrial	
		Min.	Max.	Min.	Max.
$t_{PGCK}$	Delay from global clock pad input to quadrant network	1.54 ns	1.86 ns	1.56 ns	1.88 ns
$t_{PDCK}$	Delay from dedicated clock pad input to quadrant network	1.4 ns	1.66 ns	1.42 ns	1.68 ns
$t_{BGCK}$	Global clock tree delay (quad net to flip-flop)	20 ps	200 ps	30 ps	220 ps
$t_{GSKEW}$	Global delay clock skew	30 ps	190 ps	40 ps	200 ps
$t_{DSKEW}$	Dedicated clock skew	30 ps	190 ps	40 ps	200 ps

Table 12 and Table 13 show the USB OTG and Fabric PLL timing requirements.

Table 12: USB OTG PLL Timing Requirements

Symbol	Parameter	Min.	Max.	Unit
$t_{PERIOD\_OTG\_CLK}$	12 MHz OTG_CLK period range	83.291	83.375	ns
$t_{JITTER\_OTG\_CLK}$	12 MHz OTG_CLK jitter tolerance	-500	+500	ppm

Table 13: Fabric PLL Timing Requirements

Symbol	Parameter	Min.	Max.	Unit
$t_{JITTER\_FB\_CLK}$	100 MHz FB_CLK jitter tolerance	-	150	ps

## Fabric/ASSP Interface Timing

**Table 14** describes the timing for the ASSP input signals and **Table 15** describes the timing for the ASSP output signals for the ArcticLink Solution Platform. The timing assumes typical process, voltage, and temperature conditions (i.e., VCC = 1.8 V and temperature = 25°C). In addition, the GPIO VCCIO voltage is assumed to be 3.30 V.

Table 14: ASSP Input Signals (Fabric to ASSP)

Pin Name	Reference Clock	Width	Setup Time, Tsu (ns)	Hold Time Th (ns)
<b>Peripheral Bus SRAM Interface</b>				
FB_cs [2:0]	FB_clk	3	2.81	0.96
FB_addr [19:2]	FB_clk	18	2.70	1.46
FB_wdata [31:0]	FB_clk	32	0.71	1.43
FB_be [3:0]	FB_clk	4	1.18	1.23
FB_we	FB_clk	1	2.20	0.75
FB_re	FB_clk	1	2.30	0.74
<b>Fast Peripheral Bus / SRAM Interface (Master)</b>				
FPB_rdata [31:0]	FB_clk	32	0	1.64
FPB_drdy	FB_clk	1	1.92	0.96
<b>OTG ULPI Interface</b>				
OTG_ULPI_DATA_IN[7:0]	OTG_ULPI_CLK	8	0.29	1.15
OTG_ULPI_DIR	OTG_ULPI_CLK	1	2.05	1.40
OTG_ULPI_NXT	OTG_ULPI_CLK	1	2.20	1.04
OTG_UTMIFS_RX_SE0	OTG_ULPI_CLK	1	0.03	1.20
<b>OTG I<sup>2</sup>C Compatible Serial Bus</b>				
I2C_SDA_IN	I2C_SCL	1	0	1.73
I2C_INT_N	I2C_SCL	1	0	1.81
<b>SDIO 0 (SD/SDIO/MMC/CE-ATA)</b>				
SD0_CD	FB_clk	1	0	0.88
SD0_WP	FB_clk	1	0	1.03
<b>Global Register</b>				
GPIO_IN [7:0]	FB_clk	8	0.21	0.79
FB_INT1	FB_clk	1	1.25	0.34
FB_INT2	FB_clk	1	1.24	0.48
FB_INT3	FB_clk	1	1.26	0
FB_INT4	FB_clk	1	1.26	0.06

Table 15: ASSP Output Signals (ASSP to Fabric)

Pin Name	Reference Clock	Width	Clock-to-Output Tco (ns)
<b>Peripheral Bus / SRAM Interface</b>			
FB_rdata [31:0]	FB_clk	32	4.37
FB_drdy	FB_clk	1	2.25
<b>Fast Peripheral Bus / SRAM Interface (Master)</b>			
FPB_cs	FB_clk	1	2.38
FPB_addr [31:1]	FB_clk	31	2.52
FPB_wdata [31:0]	FB_clk	32	3.82
FPB_be [3:0]	FB_clk	4	2.65
FPB_we	FB_clk	1	3.13
FPB_re	FB_clk	1	3.10
<b>OTG ULPI Interface</b>			
OTG_ULPI_DATA_OUT[7:0]	OTG_ULPI_CLK	8	4.40
OTG_ULPI_STP	OTG_ULPI_CLK	1	4.20
OTG_ULPI_FS_OEN	OTG_ULPI_CLK	1	1.93
OTG_UTMIFS_FS_EDGE_SEL	OTG_ULPI_CLK	1	5.55
<b>OTG I<sup>2</sup>C Compatible Serial Bus</b>			
I2C_SDA_OUT	I2C_SCL	1	3.41
<b>SDIO 0 (SD/SDIO/MMC/CE-ATA)</b>			
SPB_dreq	FB_clk	1	2.77
SD0_Pwr_on (active low)	FB_clk	1	2.72
SD0_LED_on	FB_clk	1	2.34
<b>Global Register</b>			
GPIO_OUT [7:0]	FB_clk	8	2.66
FB_INT_OUT	FB_clk	1	3.50

## Package Thermal Characteristics

The ArcticLink Solution Platform is available for Commercial (0°C to 85°C Junction) and Industrial (-40°C to 100°C Junction) temperature ranges.

Thermal Resistance Equations:

$$\theta_{JC} = (T_J - T_C) / P \text{ (not applicable for QL1A100 –110-pin WLCSP package)}$$

$$\theta_{JA} = (T_J - T_A) / P$$

$$P_{MAX} = (T_{JMAX} - T_{AMAX}) / \theta_{JA}$$

Parameter Description:

$\theta_{JC}$ : Junction-to-case thermal resistance (not applicable for QL1A100 –110-pin WLCSP package)

$\theta_{JA}$ : Junction-to-ambient thermal resistance

$T_J$ : Junction temperature

$T_A$ : Ambient temperature

P: Power dissipated by the device while operating

$P_{MAX}$ : The maximum power dissipation for the device

$T_{JMAX}$ : Maximum junction temperature

$T_{AMAX}$ : Maximum ambient temperature

**NOTE:** Maximum junction temperature ( $T_{JMAX}$ ) is 100°C. To calculate the maximum power dissipation for a device package look up  $\theta_{JA}$  from **Table 16**, pick an appropriate  $T_{AMAX}$  and use:

$$P_{MAX} = (125^\circ\text{C} - T_{AMAX}) / \theta_{JA}$$

Table 16: Package Thermal Characteristics

Package Description				$\theta_{JA}$ (°C/W)			$\theta_{JC}$ (°C/W)
Device	Package Code	Package Type	Pin Count	0 LFM	200 LFM	400 LFM	
QL1A100	CSP	WLCSP (10 x 11 array)	110	31.0	27.0	25	NA
	PM	TFBGA (8 mm x 8 mm)	121	33.0	29.0	28.0	10
	PT	TFBGA (12 mm x 12 mm)	196	32.0	28.0	27	8

## Power Versus Operating Frequency

$$P_{\text{total}} = P_{\text{fb}} + P_{\text{asspcore}} + P_{\text{asspio}}$$

$$P_{\text{total}} = [ 0.252 + f ( 0.00024 N_{\text{gpin}} + 0.05233 N_{\text{gpout}} + 0.00015 N_{\text{ddrin}} + 0.00024 N_{\text{ddrgpin}} + 0.04202 N_{\text{ddrout}} + 0.05083 N_{\text{ddrgpout}} + 0.00091 N_{\text{lc}} + 0.02439 N_{\text{ram}} + 0.04348 N_{\text{fifo}} + 0.02697 N_{\text{ckbf}} + 0.00661 N_{\text{clbf}} + 0.00240 N_{\text{ckld}} + 0.13182 N_{\text{ccm}} ) ] + [ 72.0341 + 0.694 F_{\text{sysclk}} + 0.252 F_{\text{fbclk}} ] + [ 63.6672 + 0.0706 F_{\text{sysclk}} + 0.05 F_{\text{fbclk}} ]$$

Where:

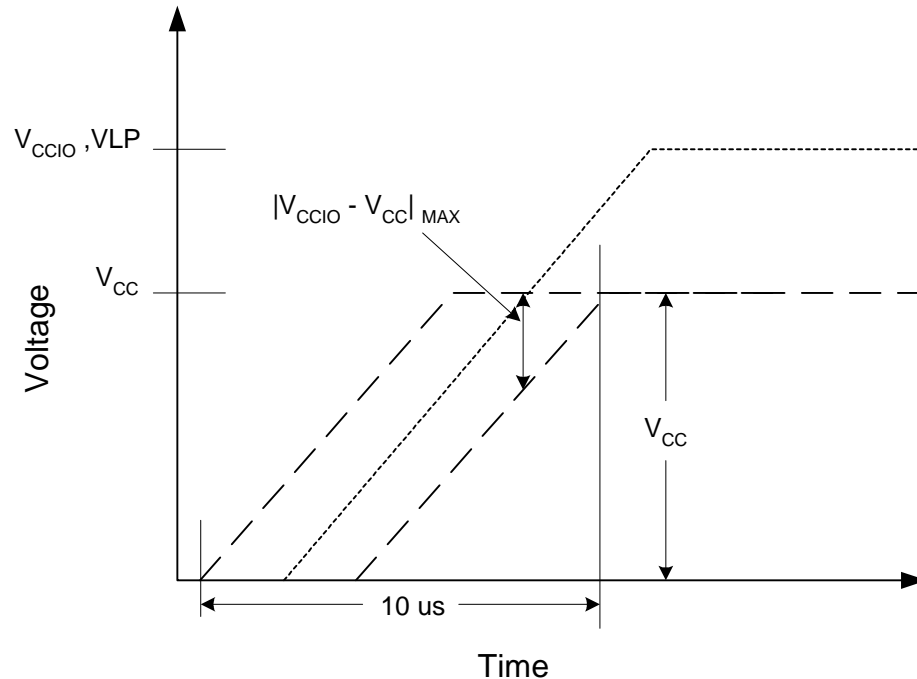
- $N_{\text{gpin}}$  = Number of GPIO Inputs
- $N_{\text{gpout}}$  = Number of GPIO Outputs
- $N_{\text{ddrin}}$  = Number of DDRIO Inputs
- $N_{\text{ddrgpin}}$  = Number of DDRIO use as GPIO Inputs
- $N_{\text{ddrout}}$  = Number of DDRIO Outputs
- $N_{\text{ddrgpout}}$  = Number of DDRIO use as GPIO Outputs
- $N_{\text{lc}}$  = Number of Logic Cells
- $N_{\text{ram}}$  = Number of RAM Blocks
- $N_{\text{fifo}}$  = Number of FIFOs
- $N_{\text{ckbf}}$  = Number of Clock Buffers
- $N_{\text{clbf}}$  = Number of Column Clock Buffers
- $N_{\text{ckld}}$  = Number of Clock Loads connected to the Column Clock Buffers
- $N_{\text{ccm}}$  = Number of CCMs
- $F_{\text{sysclk}}$  = ASSP SYS\_clk frequency
- $F_{\text{fbclk}}$  = ASSP FB\_clk frequency

**NOTE:** I/O timing is based on 3.3V for GPIO and 2.5V for DDRIO with a 5pf load. Core voltage is 1.8V. ASSP power consumption is based on both OTG and SDIO being active, assuming that the OTG PHY is switching 50% of the time, sd\_clk is equal to sys\_clk divided by 2.

For more accurate power consumption estimation, refer to the Power Calculator of the QuickWorks software.

## Power-Up Sequencing

Figure 20: Power-Up Sequencing



**Figure 20** shows an example where all VCCIO = 3.3 V.

When powering up the ArcticLink Solution Platform, VCC, VCCIO rails must take 10 μs or longer to reach the maximum value (refer to **Figure 20**). Ramping VCC and VCCIO faster than 10 μs can cause the device to behave improperly.

It is also important to ensure VCCIO and VLP are within 500 mV of VCC when ramping up the power supplies. In the case where VCCIO or VLP are greater than VCC by more than 500 mV an additional current draw can occur as VCC passes its threshold voltage. In a case where VCC is greater than VCCIO by more than 500 mV the protection diodes between the power supplies become forward biased. If this occurs then there will be an additional current load on the power supply. Having the diodes on can cause a reliability problem, since it can wear out the diodes and subsequently damage the internal transistors.

## Programming Stipulation

For the ArcticLink Solution Platform to correctly program, there must not be any race conditions or internally generated free-running oscillators in the design. This will cause an ICC programming failure during the programming process. QuickLogic cannot guarantee the operation of any device that fails programming. Therefore, race conditions and free-running oscillators must be removed from designs so that ArcticLink devices can correctly pass programming.

## USB Eye Diagrams

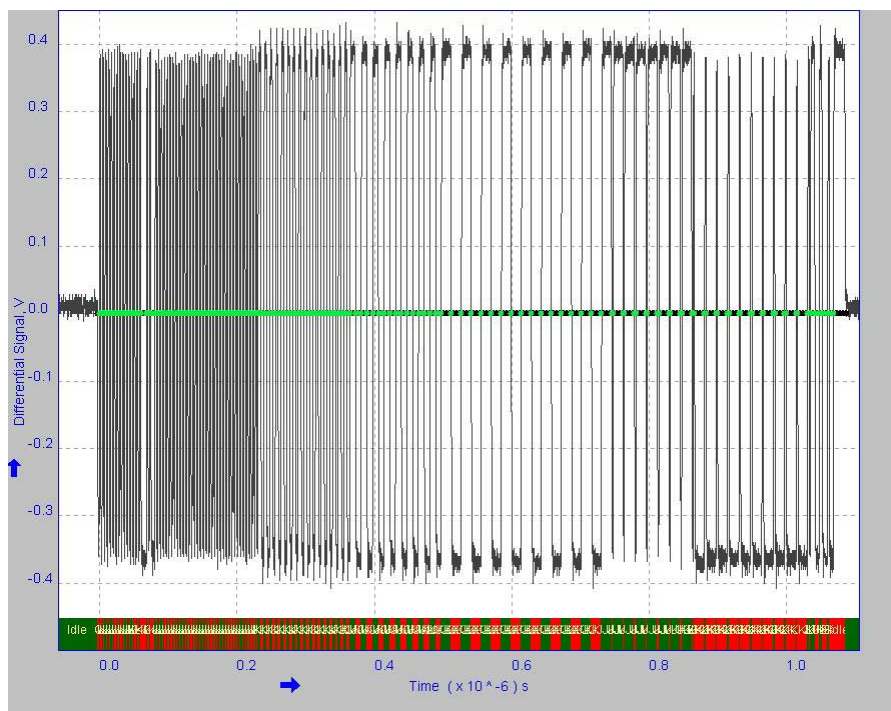
- Chip: ArcticLink 121 package
- Scope: Tektronix TDS7404B Digital Phosphor Oscilloscope
- Scope Testing Software: TDSUSB2 software version 3.0.4 Build 5
- Probe: Tektronix P7350 5Ghz 6.25x Differential Probe
- Test Fixture: Tektronix TDSUSBF USB2.0 Compliance Test Fixture
- PCB: Quicklogic ArcticLink Compliance Test Set -1
- USB-IF Compliance Test Procedures:
  - Host - [http://www.usb.org/developers/docs/Host\\_HS\\_test\\_tektronix41503.pdf](http://www.usb.org/developers/docs/Host_HS_test_tektronix41503.pdf)
  - Device - [http://www.usb.org/developers/docs/Device\\_HS\\_test\\_tektronix41503.pdf](http://www.usb.org/developers/docs/Device_HS_test_tektronix41503.pdf)

## Signal Quality Test Results for ArcticLink 121 Host Mode

For details on test setup, methodology, and performance criteria, consult the signal quality test description at the <http://www.usb.org/developers/compliance/> USB-IF Compliance Program web page.

## Near End High Speed Signal Data and Common Mode Voltage

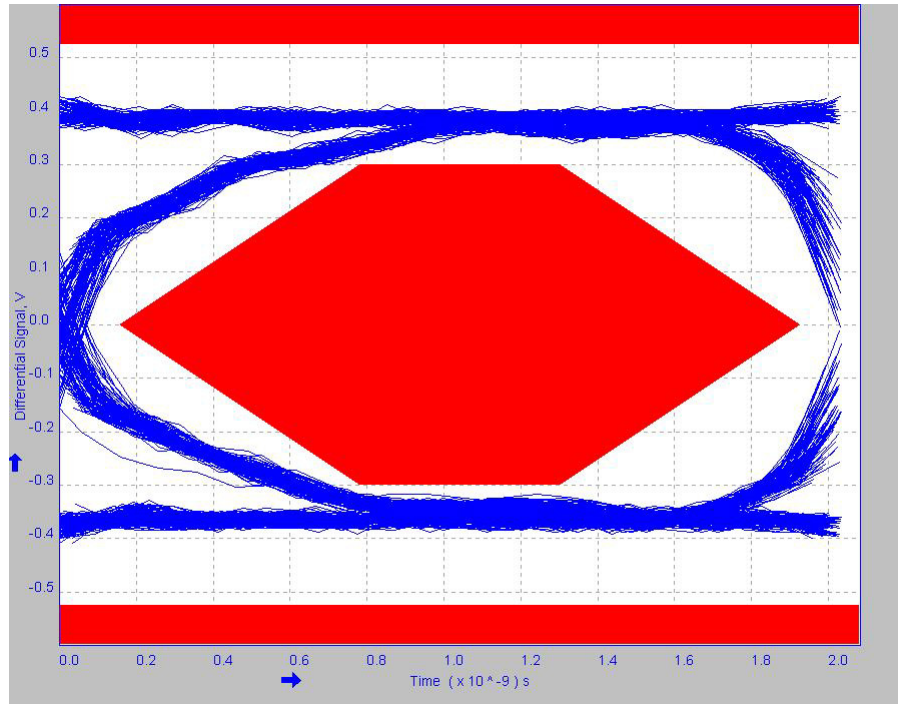
Figure 21: Host Mode Signal Quality Waveform



## Required Tests

- Overall result: pass!
- Signal eye: Eye Diagram Test passes

Figure 22: Host Mode Signal Quality Eye Diagram



- EOP width: 16.65045 ns  
EOP width passes
- EOP width (bits): 7.992826  
EOP width (bits) passes
- Measured Signalling Rate: 480.0367 Mbps  
Signal rate passes

## Additional Information

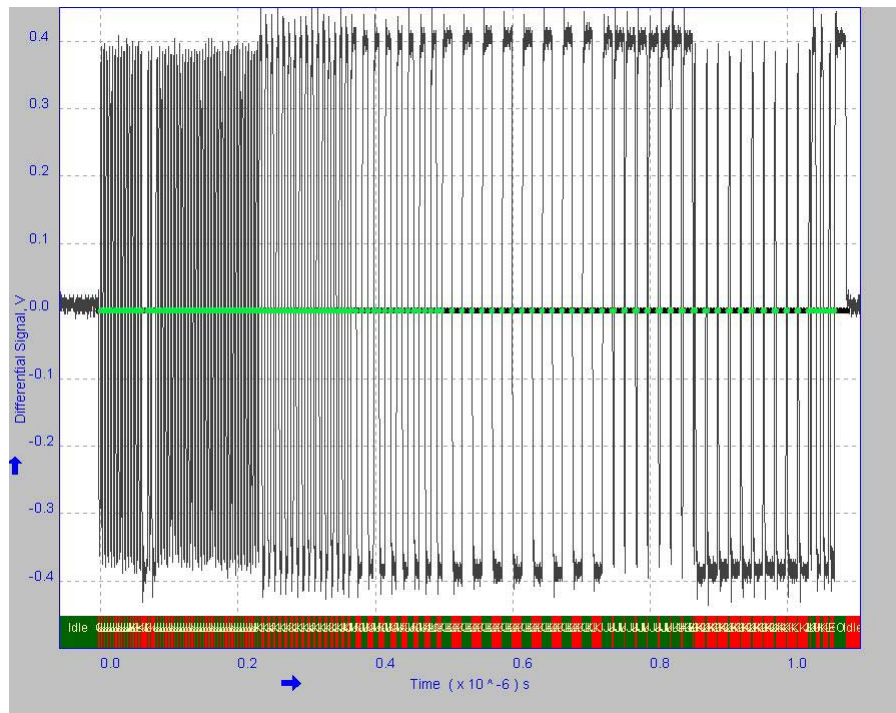
- Consecutive Jitter range: -1.068 us to 639.7 ps RMS Jitter 488.9 ns
- KJ Paired Jitter range: 4.166 ns to 29.16 ns RMS Jitter 12.51 ns
- JK Paired Jitter range: 4.166 ns to 29.16 ns RMS Jitter 12.46 ns

## Signal Quality Test Results for ArcticLink 121 Device Mode

For details on test setup, methodology, and performance criteria, please consult the signal quality test description at the <http://www.usb.org/developers/compliance/> USB-IF Compliance Program web page.

### Near End High Speed Signal Data and Common Mode Voltage

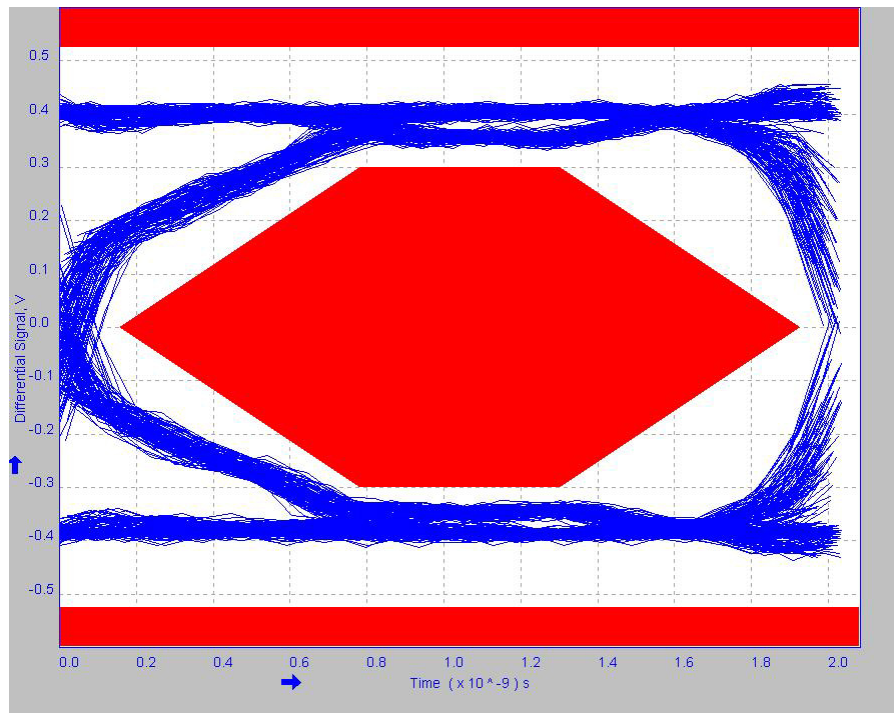
Figure 23: Device Mode Signal Quality Waveform



### Required Tests

- Overall result: pass!
- Signal eye: Eye Diagram Test passes

Figure 24: Device Mode Signal Quality Eye Diagram



- EOP width: 16.55739 ns  
EOP width passes
- EOP width (bits): 7.946519  
EOP width (bits) passes
- Measured Signalling Rate: 479.9380 Mbps  
Signal rate passes

### Additional Information

- Consecutive Jitter range: -1.068 us to 764.1 ps RMS Jitter 488.9 ns
- KJ Paired Jitter range: 4.167 ns to 29.17 ns RMS Jitter 12.51 ns
- JK Paired Jitter range: 4.167 ns to 29.17 ns RMS Jitter 12.46 ns

## Pin Descriptions

**Table 17** shows pins on the ArcticLink Solution Platform that have a single function. See **Table 18** for recommended unused pin terminations.

Table 17: Single-Function Pin Descriptions

Pin	Direction	Function	Description
<b>Dedicated Pin Descriptions</b>			
GPIO(D:A)	I/O	General purpose input/output pin	<p>The I/O pin is a bidirectional pin, configurable to either an input-only, output-only, or bidirectional pin. The letter inside the parenthesis means that the I/O is located in the bank with that letter. If an I/O is not used, the development software provides the option of tying that pin to GND, VCCIO, or Hi-Z.</p> <p>NOTE: The DDR-capable I/Os in bank D on the QL1A100 device in the 196-ball package (i.e., the I/Os with labels other than GPIO(D)) do not support PCI. For PCI support in the 196-ball package, use only single-function (non-DDR) pins labeled as GPIO(A), GPIO(B), GPIO(C), and GPIO(D). Furthermore, for the QL1A100 device in the 121-ball package, I/Os in bank D labeled as GPIO(D) on pins A8, B6, B7, B8, C7 and C8 also do not support PCI. When using the 121-ball package, any other GPIO(D:A) pins can be used for PCI except the 6 pins specifically identified above.</p>
CLK(B:A)	I	Global clock network pin low skew global clock	This pin provides access to a distributed network capable of driving the CLOCK, SET, RESET, all inputs to the Logic Cell, READ and WRITE CLOCKS, Read and Write Enables of the Embedded RAM Blocks, and I/O inputs. The voltage tolerance of this pin is specified by VCCIO(B:A).
DEDCLK(D)	I	Dedicated clock network pin low skew clock	This pin provides access to a distributed network capable of driving the CLOCK, SET, RESET, all inputs to the Logic Cell, READ and WRITE CLOCKS, Read and Write Enables of the Embedded RAM Blocks, and I/O inputs. The voltage tolerance of this pin is specified by VCCIO(D). This network can only be accessed from the DEDCLK(D) input pin.
CCMVCC	I	Power supply pin for CCM	CCM input voltage level. Configurable as 1.8 V only. The CCM is available in the ArcticLink 110-ball WLCSP and 196-ball TFBGA devices only.
CCMGND	I	Ground pin for CCM	Connect to ground. The CCM is available in the ArcticLink 110-ball WLCSP and 196-ball TFBGA devices only.
VLP	I	Very low power mode	Active low. Therefore, when VLP pin is low, the device will go into low power mode. Tie VLP to 3.3 V to disable low power mode.
VCC	I	Power supply pin	Connect to 1.8 V supply.

Table 17: Single-Function Pin Descriptions (Continued)

Pin	Direction	Function	Description
VCCIO(D:A)	I	Input voltage tolerance pin	This pin provides the flexibility to interface the device with either a 3.3 V, 2.5 V, or 1.8 V device. The letter inside the parenthesis means that the VCCIO is located in the bank with that letter. Every I/O pin in the same bank will be tolerant of the same VCCIO input signals and will drive VCCIO level output signals. This pin must be connected to either 3.3 V, 2.5 V, or 1.8 V.
GND	I	Ground pin	Connect to ground.
DQ <sup>a</sup> / GPIO(D)	I/O	Configurable pin can be declared as either a DDRIO DQ or as a general purpose I/O	The D inside the parenthesis means that the I/O is located in Bank D. If an I/O is not used, the development software provides the option of tying that pin to GND, VCCIO, or Hi-Z.
DQS <sup>a</sup> / GPIO(D)	I/O	Configurable pin can be declared as either a DDRIO DQS or as a general purpose I/O	The D inside the parenthesis means that the I/O is located in Bank D. If an I/O is not used, the development software provides the option of tying that pin to GND, VCCIO, or Hi-Z.
DQCK_N <sup>a</sup> / GPIO(D)	I/O	Configurable pin can be declared as either a DDRIO DQ, DDR negative clock, or as a general purpose I/O.	The D inside the parenthesis means that the I/O is located in Bank D. If an I/O is not used, the development software provides the option of tying that pin to GND, VCCIO, or Hi-Z.
DQCK_P <sup>a</sup> / GPIO(D)	I/O	Configurable pin can be declared as either a DDRIO DQ, DDR positive clock, or as a general purpose I/O.	The D inside the parenthesis means that the I/O is located in Bank D. If an I/O is not used, the development software provides the option of tying that pin to GND, VCCIO, or Hi-Z.
VREF(D)	I	Differential reference voltage	VREF(D) is the reference voltage pin for the SSTL1.8 and SSTL2 standards. The D inside the parenthesis means that INREF is located in Bank D. Tie this pin to GND if voltage referenced standards are not used.
VCCIO_ASSP	I	Input voltage tolerance pin	Voltage rail for SYS_RESET_n, OTG_CLK, and OTG_DRV_VBUS (connect to 3.3 V or 1.8 V depending on what the external charge pump can accept for the OTG_DRV_VBUS signal level).
JTAG Pin Descriptions			
TDI/RSI	I	Test data in for JTAG/RAM init. serial data in	Hold HIGH during normal operation. Connect to VCCIO(B) if unused.
TRSTB	I	Reset for JTAG	Active low. Hold LOW during normal operation. Connect to GND if unused. During JTAG, a high voltage is based on VCCIO(B).
TMS	I	Test mode select for JTAG	Hold HIGH during normal operation. Connect to VCCIO(B) if not used for JTAG.
TCK	I	Test clock for JTAG	Hold HIGH or LOW during normal operation. Connect to VCCIO(B) or GND if not used for JTAG.
TDO	O	Test data out for JTAG	Must be left unconnected if not used for JTAG. The output voltage drive is specified by VCCIO(B).

Table 17: Single-Function Pin Descriptions (Continued)

Pin	Direction	Function	Description
<b>USB OTG Pins</b>			
VBUS_OTG	I	Vbus	Pin used by the Hi-Speed USB 2.0 OTG Controller to monitor the Vbus.
OTG_DP	I/O	D+	Positive channel of serial USB cable.
OTG_DM	I/O	D-	Negative channel of serial USB cable.
OTG_ID	I	ID	USB ID pin of mini-AB connector.
VCCA_OTG	I	IO power	Analog 3.3 V supply for OTG PHY.
GND_A_OTG	I	IO ground	Analog ground for OTG PHY.
VCCP_OTG	I	PLL power	1.8 V supply pin for the OTG PHY PLL.
GND_P_OTG	I	PLL ground	Ground pin for the OTG PHY PLL.
OTG_RREF	Analog	Reference resistor	OTG external reference resistor. Tie to GND via a 5.76 K $\pm$ 1% resistor.
OTG_DRV_VBUS	O	Vbus drive enable	This pin is used by the Hi-Speed USB 2.0 OTG Controller to enable the external 5 V power supply (charge pump) to drive the VBUS USB line.
<b>System Pins</b>			
SYS_RESET_n	I	System reset	Used as hardware reset for all ASSP blocks.
OTG_CLK	I	OTG clock	12 MHz reference clock used for OTG PHY. Must be $\pm$ 500 ppm.

a. The number following the DDRIO signal names in the pinout tables indicates the DDRIO set the pin corresponds to.

## Recommended Unused Pin Terminations for the ArcticLink Solution Platform

All unused, general purpose I/O pins can be tied to VCCIO, GND, or Hi-Z (high impedance) internally. By default, QuickLogic QuickWorks software ties unused I/Os to GND.

Terminate the rest of the pins at the board level as recommended in **Table 18**.

Table 18: Recommended Unused Pin Terminations

Signal Name	Recommended Termination
<b>Dedicated Pins</b>	
CLK(B)	Connect to GND or VCCIO(B) if unused.
CLK(A)	Connect to GND or VCCIO(A) if unused.
CCMVCC	Connect to 1.8 V. If a CCM is used, do not attempt disable the CCM by tying the CCMVCC to GND.
DEDCLK(D)	Connect to GND or VCCIO(D) if unused.
VLP	Tie VLP to 3.3 V to disable low power mode.
VREF(D)	If the D I/O bank does not require the use of the VREF signal, connect the pin to GND.
<b>JTAG Pins</b>	
TDI	Connect to VCCIO(B) if not used for JTAG.
TRSTB	Connect to GND if not used for JTAG.
TMS	Connect to VCCIO(B) if not used for JTAG
TCK	Connect to VCCIO(B) or GND if not used for JTAG.
TDO	Must be left unconnected if not used for JTAG.
<b>USB OTG Pins</b>	
VBUS_OTG	If the designer does not intend to use the USB core, tie to GND.
OTG_DP	If the designer does not intend to use the USB core, leave unconnected.
OTG_DM	If the designer does not intend to use the USB core, leave unconnected.
OTG_ID	If the designer does not intend to use the USB core, leave unconnected.
VCCA_OTG	If the designer does not intend to use the USB core, tie this supply input to GND and configure the PHY for suspend mode by properly programming the global registers.
VCCP_OTG	If the designer does not intend to use the USB core, tie this supply input to GND and configure the PHY for suspend mode by properly programming the global registers.
OTG_RREF	If the designer does not intend to use the USB core, leave unconnected.
OTG_DRV_VBUS	If the designer does not intend to use the USB core, leave unconnected.

## Multi-Function Pins

**Table 19** shows I/O pins on the ArcticLink Solution Platform that have more than one function. These pins are normally GPIO pins unless the conditions in **Table 19** are met. See **Packaging Pinout Tables** on page 46 for the specific location of these pins.

Table 19: Multi-Function Pin Descriptions

Pin Name	Direction	Description	Condition
<b>SD/SDIO/MMC/CE-ATA =&gt; 10 pins</b>			
ASSP_SD0_DATA[0]	I/O	SD/SDIO/MMC/CE-ATA data bit 0	AF_SD0_EN = 1
ASSP_SD0_DATA[1]	I/O	SD/SDIO/MMC/CE-ATA data bit 1	
ASSP_SD0_DATA[2]	I/O	SD/SDIO/MMC/CE-ATA data bit 2	
ASSP_SD0_DATA[3]	I/O	SD/SDIO/MMC/CE-ATA data bit 3	
ASSP_SD0_CLK	O	SD/SDIO/MMC/CE-ATA clock out	
ASSP_SD0_CMD	I/O	SD/SDIO/MMC/CE-ATA command bit	
ASSP_SD0_DATA[4]	I/O	SD/SDIO/MMC/CE-ATA data bit 4	AF_SD0_EN = 1 and AF_SD0_8BIT_EN = 1
ASSP_SD0_DATA[5]	I/O	SD/SDIO/MMC/CE-ATA data bit 5	
ASSP_SD0_DATA[6]	I/O	SD/SDIO/MMC/CE-ATA data bit 6	
ASSP_SD0_DATA[7]	I/O	SD/SDIO/MMC/CE-ATA data bit 7	
<b>ULPI =&gt; 12 pins</b>			
ASSP_ULPI_DATA[7]	I/O	ULPI data bit [7]	AF_ULPI_EXT_EN =1
ASSP_ULPI_DATA[6]	I/O	ULPI data bit [6]	
ASSP_ULPI_DATA[5]	I/O	ULPI data bit [5]	
ASSP_ULPI_DATA[4]	I/O	ULPI data bit [4]	
ASSP_ULPI_DATA[3]	I/O	ULPI data bit [3]	
ASSP_ULPI_CLK	I	ULPI clock input	
ASSP_ULPI_DIR	I	ULPI data direction	
ASSP_ULPI_DATA[2]	I/O	ULPI data bit [2]	
ASSP_ULPI_DATA[1]	I/O	ULPI data bit [1]	
ASSP_ULPI_DATA[0]	I/O	ULPI data bit [0]	
ASSP_ULPI_NXT	I	ULPI NXT signal	
ASSP_ULPI_STP	O	ULPI STP signal	

## ASSP/Programmable Fabric Interface Ports

Table 20: ASSP-to-Fabric Port Description

Signal Name	Direction <sup>a</sup>	Width (bits)	Function	Default <sup>b</sup>
<b>ASSP System Clock =&gt; 1 Signal</b>				
SYS_clk	Out	1	ASSP bus clock	1'b0
<b>Peripheral Bus =&gt; 1 Signal</b>				
FB_clk	Out	1	SRAM Interface clock	1'b0
<b>Peripheral Buses SRAM Interface =&gt; 92 Signals</b>				
FB_cs [2:0]	Out	3	Chip select for peripheral bus targets. <u>FB_cs[2:0] Target</u> 000 None selected. 001 8 KByte SRAM. 010 SD/SDIO/MMC/CE-ATA and global registers. 100 USB OTG registers. All others Invalid. Do not select more than one target at a time.	3'b0
FB_addr [19:2]	Out	18	Address (32-bit aligned access only).	18'b0
FB_wdata [31:0]	Out	32	Write data.	18'b0
FB_rdata [31:0]	In	32	Read data.	
FB_be [3:0]	Out	4	Byte enable.	4'b0
FB_drdy	In	1	Data ready.	
FB_we	Out	1	Write enable.	1'b0
FB_re	Out	1	Read enable.	1'b0
<b>Fast Peripheral Bus / SRAM Interface (Master) =&gt; 103 Signals</b>				
FPB_cs	In	1	Chip select	
FPB_addr [31:1]	In	31	Address NOTE: Only 30 bits are driven, bit[1] is grounded inside the core.	
FPB_wdata [31:0]	In	32	Write data	
FPB_rdata [31:0]	Out	32	Read data	32'b0
FPB_be [3:0]	In	4	Byte enable	
FPB_we	In	1	Write enable	
FPB_re	In	1	Read enable	
FPB_drdy	Out	1	Data Ready	1'b0
<b>OTG ULPI Interface =&gt; 23 Signals</b>				
OTG_ULPI_CLK	Out	1	Interface clock.	1'b0
OTG_ULPI_DATA_IN[7:0]	Out	8	ULPI data bus for synchronous (normal) mode. Table 3 lists signal definitions for other modes.	8'b0
OTG_ULPI_DATA_OUT[7:0]	In	8		

Table 20: ASSP-to-Fabric Port Description (Continued)

Signal Name	Direction <sup>a</sup>	Width (bits)	Function	Default <sup>b</sup>
OTG_ULPI_DIR	Out	1	ULPI dir <u>Mode</u> Synchronous (Normal) Serial Carkit <u>Usage</u> Data bus direction Always asserted Always asserted	
OTG_ULPI_NXT	Out	1	ULPI next data <u>Mode</u> Synchronous (Normal) Serial Carkit <u>Usage</u> Accept/request next data Not used Not used	1'b0
OTG_ULPI_STP	In	1	ULPI stop data <u>Mode</u> Synchronous (Normal) Serial Carkit <u>Usage</u> End of transmit packet Exit serial mode Exit carkit mode	
OTG_UTMIFS_RX_SE0	Out	1	UTMI FS serial SE0 assertion received.	1'b0
OTG_UTMIFS_FS_EDGE_SEL	In	1	UTMI FS selects low/full-speed slew rate.	
<b>OTG I<sup>2</sup>C Compatible Serial Bus=&gt; 4 Signals</b>				
I2C_SCL	In	1	Serial clock.	
I2C_SDA_OUT	In	1	Serial output data.	
I2C_SDA_IN	Out	1	Serial input data.	1'b0
I2C_INT_N	Out	1	Interrupt request.	1'b0
<b>SDIO 0 (SD/SDIO/MMC/CE-ATA) =&gt; 5 Signals</b>				
SPB_dreq	In	1	DMA request signal.	
SD0_CD	Out	1	SDIO 0 card detect.	1'b0
SD0_Pwr_on	In	1	Active low. SDIO 0 power control for power saving.	
SD0_LED_on	In	1	SDIO 0 LED control.	
SD0_WP	Out	1	SDIO 0 write protect.	1'b0
<b>Global Register =&gt; 21 Signals</b>				
GPIO_IN [7:0]	Out	8	General purpose I/O (input to ASSP).	8'b0
GPIO_OUT [7:0]	In	8	General purpose I/O (output from ASSP).	
FB_INT1	Out	1	Fabric interrupt #1.	1'b0
FB_INT2	Out	1	Fabric interrupt #2.	1'b0
FB_INT3	Out	1	Fabric interrupt #3.	1'b0
FB_INT4	Out	1	Fabric interrupt #4.	1'b0
FB_INT_OUT	In	1	Fabric interrupt from ASSP.	

Table 20: ASSP-to-Fabric Port Description (Continued)

Signal Name	Direction <sup>a</sup>	Width (bits)	Function	Default <sup>b</sup>
<b>Global Register Configuration Control (Anti-Fuse) - Nonroutable =&gt; 87 Signals</b>				
AF_FB_VL [3:0]	Out	4	Fabric address decode signal. Sets the uppermost 4-bit decode for 8 K SRAM access in internal bus. Internal bus transactions from the USB DMA will be decoded to the SRAM scratchpad when internal bus address[31:28] matches AF_FB_VL[3:0]. Otherwise, internal bus transaction will be decoded as transaction to SRAM Master interface bridge.	4'b0
AF_QL_REV [3:0]	Out	4	QuickLogic revision code.	4'b0
AF_QL_ID [7:0]	Out	8	QuickLogic ID code.	8'b0
AF_USB_CFG	Out	1	USB OTG configuration bit. Configuration bit reflected as the USB feature bit of the global registers. Use this bit to notify the host processor of presence of USB feature.	1'b0
AF_ATA_CFG	Out	1	CE-ATA configuration bit. Configuration bit reflected as the CE-ATA feature bit of the global registers. Use this bit to notify the host processor of presence of CE-ATA feature.	1'b0
AF_SDIO1_CFG	Out	1	SDIO 1 configuration bit.	1'b0
AF_PCI_CFG	Out	1	PCI configuration bit.	1'b0
AF_IDE_CFG	Out	1	IDE controller configuration bit.	1'b0
AF_SRAM_MAP	Out	1	SRAM address map bit.	1'b0
AF_BUS_WIDTH	Out	1	Host CPU bus width. Configuration bit reflected as the processor bus width in the global register. Use this bit to program the host processor bus width: 0 = 16-bit 1 = 32-bit  Value will not affect the ArcticLink Solution Platform internal bus access. Internal access will always be in 32-bit.  NOTE: A 16- to32-bit converter must be programmed in the FPGA for a 16-bit processor bus to work properly.	1'b0

Table 20: ASSP-to-Fabric Port Description (Continued)

Signal Name	Direction <sup>a</sup>	Width (bits)	Function	Default <sup>b</sup>
AF_SDCLK_FREQ	Out	6	<p>Base clock frequency for SD clock.</p> <p>Configuration bits reflected as SD/SDIO base clock frequency in SD/SDIO capability register. This value indicates the base (maximum) clock frequency for the SD clock in MHz. The next higher integer value is used for non-integer clock frequencies.</p> <p>The host driver uses this value to calculate the clock divider value (refer to the SDCLK Frequency Select in the Clock Control register). The resulting clock frequency must not exceed the upper limit of the SD device's clock frequency.</p> <p>The supported clock range is 10 MHz to 63 MHz. If these bits are programmed to 0, the host must find an alternate way to get this information.</p>	6'b0
AF_TIMEOUT_UNIT	Out	1	<p>Time out clock unit.</p> <p>Configuration bit reflected as the base clock frequency unit for data time-out error detection in SD/SDIO capability register.</p> <p>'0' = KHz '1' = MHz</p>	1'b0
AF_TIMEOUT_FREQ	Out	6	<p>Time out clock frequency.</p> <p>Configuration bits reflected as the base clock frequency for data time-out error detection in SD/SDIO capability register.</p>	6'b0
AF_MAX_BLK_LEN	Out	2	<p>Maximum block length.</p> <p>Configuration bits reflected as the maximum block size in SD/SDIO capability register. This provides the maximum block size the host can read or write to the SD/SDIO/MMC/CE-ATA Host Controller buffer without insertion of wait states. The current SD/SDIO/MMC/CE-ATA can only support "00" (512 byte size).</p>	2'b0
AF_VOLT_SUP	Out	3	<p>Voltage support.</p> <p>Configuration bits reflected as the SD/SDIO/MMC/CE-ATA interface supported voltage in SD/SDIO capability register.</p>	3'b0
AF_MAX_CUR_33V	Out	8	<p>Maximum current for 3.3 V.</p> <p>Configuration bits reflected as the maximum current capability for 3.3 V in SD/SDIO capability register. If this information is supplied to the Host System via another method, all Maximum Current Capabilities registers shall be 0.</p>	8'b0

Table 20: ASSP-to-Fabric Port Description (Continued)

Signal Name	Direction <sup>a</sup>	Width (bits)	Function	Default <sup>b</sup>
AF_MAX_CUR_30V	Out	8	Maximum current for 3.0 V. Configuration bits reflected as the maximum current capability for 3.0 V in SD/SDIO capability register. If this information is supplied to the Host System via another method, all Maximum Current Capabilities registers shall be 0.	8'b0
AF_MAX_CUR_18V	Out	8	Maximum current for 1.8v. Configuration bits reflected as the maximum current capability for 1.8 V in SD/SDIO capability register. If this information is supplied to the Host System via another method, all Maximum Current Capabilities registers shall be 0.	8'b0
AF_SPEC_VER	Out	8	SD host controller specification version number.	8'b0
AF_VEND_VER	Out	8	Vendor version number.	8'b0
AF_DMA_SUP	Out	1	SD/SDIO/MMC/CE-ATA DMA support enable.	1'b0
AF_SD0_EN	Out	1	SD/SDIO/MMC/CE-ATA enable. '0' = Disables SD/SDIO/MMC/CE-ATA '1' = Enables SD/SDIO/MMC/CE-ATA NOTE: This automatically makes a set of pre-assigned programmable I/Os into SD/SDIO/MMC/CE-ATA I/Os.	1'b0
AF_SD0_8BIT_EN	Out	1	SD/SDIO/MMC/CE-ATA 8-bit enable. '0' = 4-bit SD/SDIO/MMC/CE-ATA '1' = 8-bit SD/SDIO/MMC/CE-ATA NOTE: This controls which subset of the programmable I/Os will be used as SD/SDIO/MMC/CE-ATA I/Os.	1'b0
AF_ULPI_EXT_EN	Out	1	ULPI external pin enable. '0' = Disables ULPI external pins '1' = Enables ULPI external pins NOTE: ULPI interface is used when an internal register (internal to USB core) is set to enable ULPI. This bit controls which of the two ULPI interfaces is used. When set to '0', the FB ULPI interface is used.	1'b0
AF_SD0_PULL_UP_EN	Out	1	SD/SDIO/MMC/CE-ATA data/cmd Line internal pull-up enable. '0' = Disables on-die pull-up resistor on DATA and CMD lines for SSD/SDIO/MMC/CE-ATA. '1' = Enables on-die pull-up resistor on DATA and CMD lines for SD/SDIO/MMC/CE-ATA.	1'b0

a. Direction is with respect to Fabric:

Out = FB -> ASSP (fpga\_out)

In = ASSP -> FB (fpga\_in)

b. Default column provides tie-off value for signals when the particular block that uses the signals are not enabled.

## Packaging Pinout Tables

### QL1A100 - 110 WLCSP (10 x 11 array) Pinout Table

Table 21: QL1A100 - 110 WLCSP (10 x 11 array) Pinout Table

Ball	Function	Ball	Function	Ball	Function	Ball	Function
A1	VCC	C7	GPIO(D)/ ASSP_ULPI_DATA[6]	F2	GPIO(A)	H8	GPIO(B)
A2	GPIO(D)	C8	VCC	F3	GPIO(A)	H9	GPIO(B)
A3	GPIO(D)	C9	GPIO(C)/ ASSP_SD0_DATA[7]	F4	VCCIO(A)	H10	OTG_DRV_VBUS
A4	GPIO(D)/ ASSP_ULPI_STP	C10	GNDP_OTG	F5	GND	H11	OTG_CLK
A5	DEDCLK(D)	C11	OTG_DP	F6	GND	J1	GPIO(B)
A6	GPIO(D)/ ASSP_ULPI_DATA[0]	D1	GPIO(A)	F7	GND	J2	GPIO(B)
A7	GPIO(D)/ASSP_ULPI_ CLK	D2	GPIO(A)	F8	VCCIO(C)	J3	GPIO(B)
A8	GPIO(D)/ ASSP_ULPI_DATA[7]	D3	GPIO(A)	F9	GPIO(C)/ ASSP_SD0_DATA[3]	J4	VCC
A9	VCCA_OTG	D4	VCCIO(D)	F10	GPIO(C)/ ASSP_SD0_DATA[2]	J5	GPIO(B)
A10	OTG_ID	D5	GND	F11	GPIO(C)	J6	GPIO(B)
A11	VBUS_OTG	D6	VCC	G1	GPIO(A)	J7	GPIO(B)
B1	VCCIO(B)	D7	GND	G2	GPIO(A)	J8	GPIO(B)
B2	CCMVCC	D8	GND	G3	GPIO(A)	J9	GPIO(B)
B3	GPIO(D)	D9	GPIO(C)/ ASSP_SD0_DATA[4]	G4	GND	J10	VCCIO(B)
B4	GPIO(D)/ ASSP_ULPI_NXT	D10	GPIO(C)/ ASSP_SDO_DATA[6]	G5	GND	J11	SYS_RESET_N
B5	GPIO(D)/ ASSP_ULPI_DATA[2]	D11	VCCP_OTG	G6	VCC	K1	GPIO(B)
B6	GPIO(D)/ ASSP_ULPI_DATA[3]	E1	CLK(A)/CCMIN	G7	GND	K2	GPIO(B)
B7	GPIO(D)/ ASSP_ULPI_DATA[5]	E2	GPIO(A)	G8	VCC	K3	GPIO(B)
B8	GND	E3	GPIO(A)	G9	GPIO(C)/ ASSP_SD0_DATA[0]	K4	CLK(B)
B9	OTG_RREF	E4	VCC	G10	GPIO(C)/ ASSP_SD0_DATA[1]	K5	GPIO(B)
B10	GND_A_OTG	E5	GND	G11	GPIO(C)	K6	GPIO(B)
B11	OTG_DM	E6	GND	H1	VLP	K7	GPIO(B)
C1	GPIO(A)	E7	GND	H2	GPIO(A)	K8	GPIO(B)
C2	GPIO(A)	E8	VCC	H3	GPIO(B)	K9	VCC
C3	GPIO(A)	E9	GPIO(C)/ ASSP_SD0_CLK	H4	GPIO(B)	K10	GND
C4	GPIO(D)/ ASSP_ULPI_DATA[1]	E10	GPIO(C)/ ASSP_SDO_CMD	H5	GPIO(B)	K11	VCCIO_ASSP
C5	GPIO(D)/ ASSP_ULPI_DIR	E11	GPIO(C)/ ASSP_SD0_DATA[5]	H6	VCCIO(B)		
C6	GPIO(D)/ ASSP_ULPI_DATA[4]	F1	GPIO(A)	H7	GPIO(B)		

## QL1A100 - 121 TFBGA (8 mm x 8 mm) Pinout Table

Table 22: QL1A100 - 121 TFBGA (8 mm x 8 mm) Pinout Table

Ball	Function	Ball	Function	Ball	Function	Ball	Function
A1	OTG_DM	C10	GPIO(A)	F8	VCC	J6	GPIO(B)
A2	VCCA_OTG	C11	GND	F9	GPIO(A)	J7	GPIO(B)
A3	GPIO(D)/ ASSP_ULPI_DATA[7]	D1	VBUS_OTG	F10	GPIO(A)	J8	GPIO(B)
A4	GPIO(D)/ ASSP_ULPI_CLK	D2	VCCP_OTG	F11	GPIO(A)	J9	VCC
A5	GPIO(D)/ ASSP_ULPI_DATA[1]	D3	GNDP_OTG	G1	GPIO(C)/ ASSP_SD0_CLK	J10	VCCIO(B)
A6	GPIO(D)/ ASSP_ULPI_STP	D4	VCC	G2	GPIO(C)/ ASSP_SD0_DATA[2]	J11	GPIO(B)
A7	DEDCLK(D)	D5	GPIO(D)/ ASSP_ULPI_DIR	G3	GPIO(C)/ ASSP_SD0_CMD	K1	SYS_RESET_n
A8	GPIO(D)	D6	VCC	G4	VCCIO(C)	K2	VCCIO_ASSP <sup>a</sup>
A9	TMS	D7	VCCIO(D)	G5	GND	K3	VCC
A10	GPIO(A)	D8	GND	G6	GND	K4	TDO
A11	VCC	D9	VCCIO(A)	G7	GND	K5	GPIO(B)
B1	OTG_DP	D10	GPIO(A)	G8	GND	K6	GPIO(B)
B2	OTG_ID	D11	GPIO(A)	G9	VCC	K7	GPIO(B)
B3	GPIO(D)/ ASSP_ULPI_DATA[4]	E1	TCK	G10	VLP	K8	TDI
B4	GPIO(D)/ ASSP_ULPI_DATA[5]	E2	GPIO(C)/ ASSP_SD0_DATA[6]	G11	TRSTB	K9	GPIO(B)
B5	GPIO(D)/ ASSP_ULPI_DATA[0]	E3	GPIO(C)/ ASSP_SD0_DATA[7]	H1	GPIO(C)/ ASSP_SD0_DATA[1]	K10	GPIO(B)
B6	GPIO(D)	E4	VCCIO(D)	H2	GPIO(C)/ ASSP_SD0_DATA[0]	K11	GPIO(B)
B7	GPIO(D)	E5	GND	H3	GPIO(C)/ ASSP_SD0_DATA[3]	L1	OTG_DRV_VBUS
B8	GPIO(D)	E6	GND	H4	VCC	L2	GND
B9	GPIO(A)	E7	GND	H5	GPIO(B)	L3	GND
B10	GND	E8	GND	H6	VCCIO(B)	L4	GND
B11	VCCIO(B)	E9	GPIO(A)	H7	VCC	L5	GPIO(B)
C1	GND_A_OTG	E10	GPIO(A)	H8	VCC	L6	GPIO(B)
C2	OTG_RREF	E11	CLK(A)	H9	GND	L7	GPIO(B)
C3	GPIO(D)/ ASSP_ULPI_DATA[6]	F1	GPIO(C)/ ASSP_SD0_DATA[5]	H10	GPIO(B)	L8	CLK(B)
C4	GPIO(D)/ ASSP_ULPI_DATA[3]	F2	GPIO(C)	H11	GPIO(B)	L9	GPIO(B)
C5	GPIO(D)/ ASSP_ULPI_DATA[2]	F3	GPIO(C)/ ASSP_SD0_DATA[4]	J1	OTG_CLK	L10	GPIO(B)
C6	GPIO(D)/ ASSP_ULPI_NXT	F4	GND	J2	GPIO(C)	L11	GPIO(B)
C7	GPIO(D)	F5	GND	J3	VCC		
C8	GPIO(D)	F6	GND	J4	VCCIO(B)		
C9	VCC	F7	GND	J5	GPIO(B)		

a. Voltage rail for SYS\_RESET\_n, OTG\_CLK, and OTG\_DRV\_VBUS (connect to 3.3 V or 1.8 V depending on what the external charge pump can accept for the OTG\_DRV\_VBUS signal level).

## QL1A100 - 196 TFBGA (12 mm x 12 mm) Pinout Table

Table 23: QL1A100 – 196 TFBGA (12 mm x 12 mm) Pinout Table

Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function
A1	GPIO(D)/ ASSP_ULPI_DATA[0]	C13	VCCIO(B)	F11	GPIO(A)	J9	GND	M7	GPIO(B)
A2	DQ1/GPIO(D)	C14	CCMVCC	F12	GPIO(A)	J10	VCC	M8	GPIO(B)
A3	DEDCLK(D)	D1	OTG_DM	F13	GPIO(A)	J11	VCC	M9	GPIO(B)
A4	DQS1/GPIO(D)	D2	OTG_ID	F14	GPIO(A)	J12	TRSTB	M10	GPIO(B)
A5	DQCK_P1/GPIO(D)	D3	GND	G1	GPIO(C)/ ASSP_SDO_DATA[5]	J13	GPIO(A)	M11	GPIO(A)
A6	DQCK_N1/GPIO(D)	D4	GPIO(D)/ ASSP_ULPI_DATA[5]	G2	GPIO(C)/ ASSP_SDO_DATA[6]	J14	GPIO(A)	M12	GPIO(A)
A7	DQ1/GPIO(D)	D5	GPIO(D)/ ASSP_ULPI_DATA[2]	G3	VCCP_OTG	K1	GPIO(C)/ ASSP_SDO_DATA[2]	M13	GPIO(A)
A8	DQ2/GPIO(D)	D6	DQ1/GPIO(D)	G4	VCCIO(C)	K2	GPIO(C)/ ASSP_SDO_DATA[1]	M14	GPIO(A)
A9	DQ2/GPIO(D)	D7	DQ1/GPIO(D)	G5	GND	K3	OTG_DRV_VBUS	N1	SYS_RESET_n
A10	DQS2/GPIO(D)	D8	TMS	G6	GND	K4	VCC	N2	GPIO(B)
A11	DQCK_P2/GPIO(D)	D9	DQ2/GPIO(D)	G7	GND	K5	VCCIO(B)	N3	GPIO(B)
A12	DQCK_N2/GPIO(D)	D10	DQ2/GPIO(D)	G8	GND	K6	VCCIO(B)	N4	TDO
A13	GPIO(D)	D11	GPIO(D)	G9	GND	K7	VCCIO(B)	N5	GPIO(B)
A14	GPIO(D)	D12	GND	G10	VCCIO(A)	K8	VCC	N6	GPIO(B)
B1	GPIO(D)/ ASSP_ULPI_CLK	D13	GPIO(A)	G11	VCCIO(A)	K9	VCCIO(B)	N7	GPIO(B)
B2	GPIO(D)/ ASSP_ULPI_DATA[6]	D14	CCMGND	G12	GPIO(A)	K10	GPIO(A)	N8	GPIO(B)
B3	GPIO(D)/ ASSP_ULPI_DATA[4]	E1	OTG_DP	G13	GPIO(A)	K11	VCC	N9	GPIO(B)
B4	GPIO(D)/ ASSP_ULPI_DATA[1]	E2	OTG_RREF	G14	GPIO(A)	K12	GPIO(A)	N10	GPIO(B)
B5	GPIO(D)/ ASSP_ULPI_STP	E3	VBUS_OTG	H1	GPIO(C)/ ASSP_SDO_CLK	K13	GPIO(A)	N11	GPIO(B)
B6	DQ1/GPIO(D)	E4	VCC	H2	GPIO(C)/ ASSP_SDO_CMD	K14	GPIO(A)	N12	VLP
B7	DQ1/GPIO(D)	E5	VCCIO(D)	H3	GPIO(C)/H ASSP_SDO_DATA[4]	L1	GPIO(C)/ ASSP_SDO_DATA[0]	N13	GND
B8	DQ1/GPIO(D)	E6	VCCIO(D)	H4	VCC	L2	GND	N14	GPIO(A)
B9	DQ2/GPIO(D)	E7	VCCIO(D)	H5	GND	L3	GPIO(B)	P1	GPIO(B)
B10	DQ2/GPIO(D)	E8	VCC	H6	GND	L4	GPIO(B)	P2	GPIO(B)
B11	DQ2/GPIO(D)	E9	VCCIO(D)	H7	GND	L5	GND	P3	GPIO(B)
B12	GPIO(D)	E10	VCCIO(D)	H8	GND	L6	GPIO(B)	P4	GPIO(B)
B13	GPIO(D)	E11	VCC	H9	GND	L7	TDI	P5	GPIO(B)
B14	GPIO(D)	E12	GPIO(A)	H10	VCCIO(A)	L8	GPIO(B)	P6	CLK(B)
C1	VCCA_OTG	E13	GPIO(A)	H11	VCCIO(A)	L9	GPIO(B)	P7	GPIO(B)
C2	GPIO(D)/ ASSP_ULPI_DATA[3]	E14	GPIO(A)	H12	GPIO(A)	L10	GPIO(B)	P8	GPIO(B)
C3	GPIO(D)/ ASSP_ULPI_DATA[7]	F1	GND_A_OTG	H13	GPIO(A)	L11	GPIO(A)	P9	GPIO(B)
C4	GPIO(D)/ ASSP_ULPI_DIR	F2	TCK	H14	CLK(A)/PLLIN	L12	GPIO(A)	P10	GPIO(B)
C5	GPIO(D)/ ASSP_ULPI_NXT	F3	GNDP_OTG	J1	GPIO(C)	L13	GPIO(A)	P11	GPIO(B)
C6	DQ1/GPIO(D)	F4	GPIO(C)/ ASSP_SDO_DATA[7]	J2	GPIO(C)/ ASSP_SDO_DATA[3]	L14	GPIO(A)	P12	GPIO(B)
C7	VREF(D)	F5	VCC	J3	GPIO(C)	M1	OTG_CLK	P13	GPIO(A)
C8	DQ1/GPIO(D)	F6	GND	J4	VCCIO_ASSP <sup>a</sup>	M2	GPIO(B)	P14	GPIO(A)
C9	DQ2/GPIO(D)	F7	GND	J5	VCC	M3	VCCIO(B)		
C10	DQ2/GPIO(D)	F8	GND	J6	GND	M4	GPIO(B)		
C11	GPIO(D)	F9	GND	J7	GND	M5	GPIO(B)		
C12	GPIO(D)	F10	VCC	J8	GND	M6	GPIO(B)		

a. Voltage rail for SYS\_RESET\_n, OTG\_CLK, and OTG\_DRV\_VBUS (connect to 3.3 V or 1.8 V depending on what the external charge pump can accept for the OTG\_DRV\_VBUS signal level).

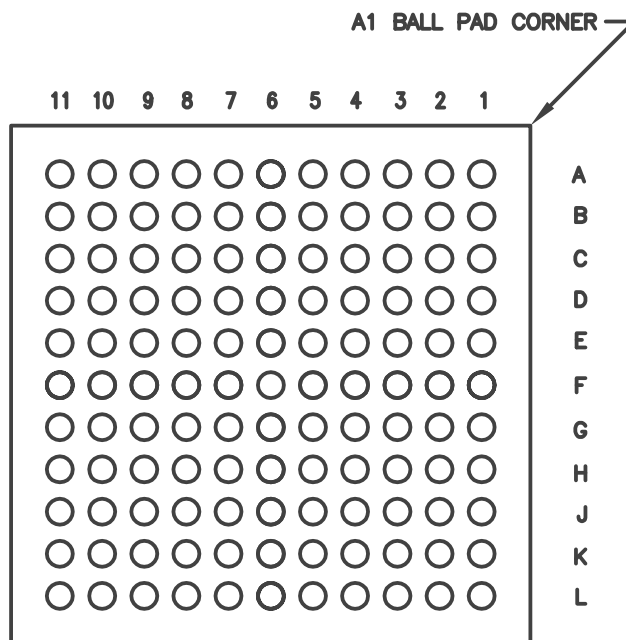
## Packaging Pinout Diagrams

### QL1A100 - 121 TFBGA Pinout Diagram

Top



Bottom

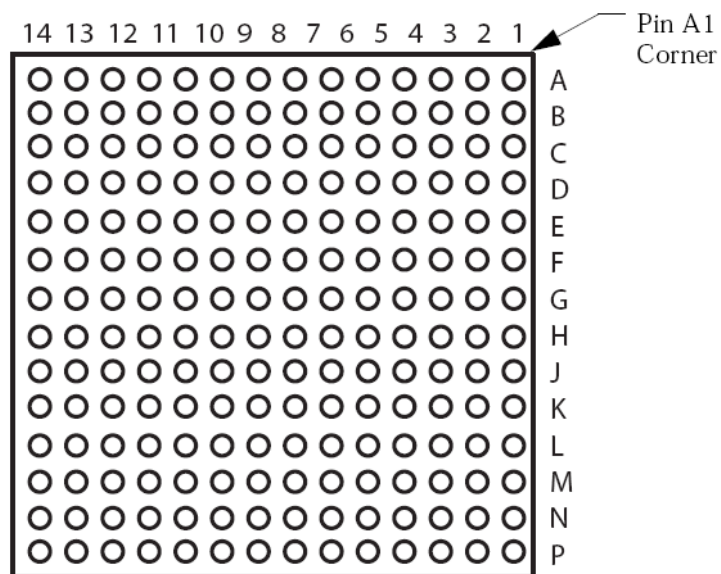


## QL1A100 - 196 TFBGA (12 mm x 12 mm) Pinout Diagram

Top



Bottom









## Packaging Information

The ArcticLink Solution Platform packaging information is shown in **Table 24**.

Table 24: Packaging Options

Device Information	QL1A100		
	Ball	Pb	Pb-Free
Package Definitions <sup>a</sup>	110 WLCSP (10 x 11 array) Pitch - 0.40 mm	-	X
	121 TFBGA (8 mm x 8 mm) Pitch - 0.65 mm	-	X
	196 TFBGA (12 mm x 12 mm) Pitch - 0.80 mm	-	X

a. TFBGA = Thin Profile Fine Pitch Ball Grid Array  
WLCSP = Wafer Level Chip Scale Package

## Ordering Information

ArcticLink Solution Platform Customer Specific Standard Products (CSSPs) have assigned part numbers, contact your local sales representative for your specific CSSP number.

## Contact Information

Phone: (408) 990-4000 (US)  
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Support: [www.quicklogic.com/support](http://www.quicklogic.com/support)

Internet: [www.quicklogic.com](http://www.quicklogic.com)

## Revision History

Revision	Date	Originator and Comments
A	June 2006	Judd Heape and Kathleen Murchek
B	December 2006	Stanley Hung, Judd Heape and Kathleen Murchek
C	March 2007	Judd Heape and Kathleen Murchek
D	July 2007	Judd Heape and Kathleen Murchek
E	December 2007	Kathleen Murchek Changed title from ArcticLink Solution Platform Data Sheet to ArcticLink Device Data Sheet. Added conditional text and made minor changes.
F	July 2008	Kathleen Murchek Updated Disclaimer, Contact and Ordering information. Added Theta-JC column to Package Thermal Characteristics table.
G	July 2008	Jason Lew and Kathleen Murchek Added 110 WLCSP pinout package information.
H	September 2008	Jason Lew and Kathleen Murchek Updated QL1A100 - 110 WLCSP (10 x 11 array) Pinout Table
I	October 2008	Jason Lew and Kathleen Murchek Added "The CCM is available in the ArcticLink 110-ball WLCSP and 196-ball TFBGA devices only." to the pin descriptions for CCMVCC and CCMGND.
J	April 2009	Jason Lew and Kathleen Murchek
K	January 2010	Tim Saxe and Kathleen Murchek Added notation that SD0_Pwr_on signal is active low.
L	May 2010	Kathleen Bylsma Updated contact information.

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