

ArcticLink[®] Solution Platform Data Sheet



Programmable Solution Platform Including Hi-Speed Universal Serial Bus (USB) 2.0 On-The-Go (OTG) and SD/SDIO/MMC/CE-ATA

Platform Highlights

Hi-Speed USB 2.0 OTG Controller

- Single port OTG with embedded high-speed PHY
- Optional 12-signal ULPI interface
- Full-speed CEA-936-A mini-USB analog carkit interface
- Dedicated DMA controller
- High-speed up to 480 Mbits/sec.

SD/SDIO/MMC/CE-ATA Host Controller

- SD/SDIO 1-bit or 4-bit up to 52 MHz with Secure Digital High Capacity (SDHC) support
- CE-ATA 1-bit, 4-bit or 8-bit up to 52 MHz
- MMC 1-bit, 4-bit or 8-bit up to 52 MHz
- High-speed and flexible to support multiple storage options and SDIO peripherals

Flexible Programmable Fabric

- 20 customizable building blocks (CBBs) (see [Programmable Fabric Architectural Overview](#) on page 16 for a detailed explanation of CBBs)
- 1.8 V core voltage, 1.8/2.5/3.3 V drive capable I/Os
- 36 Kbits of SRAM – seven dual-port 4-Kbit high performance SRAM blocks
- Embedded synchronous/asynchronous FIFO controllers
- One user configurable clock manager (CCM) (110-ball WLCSP and 196-ball TFBGA packages only) (see [Configurable Clock Manager](#) on page 17 for an explanation of CCM)
- Up to 120 programmable I/Os available
- Ideal platform to implement additional proven system building blocks, custom functions, glue logic and processor interface

Programmable I/O

- Bank programmable drive strength
- Bank programmable slew rate control
- Independent I/O banks capable of supporting multiple I/O standards in one device
- Native support for DDRIOs (196-ball package only)
- Bank programmable I/O standards: LVTTTL, LVCMOS, and LVCMOS18
- Can be used for level shifter and I/O voltage translator

Very Low Power (VLP) Mode

- The QuickLogic[®] ArcticLink Solution Platform has a special VLP pin which can enable a low power sleep mode that significantly reduces the overall power consumption of the device by placing the device in standby.
- Enter/exit VLP mode from/to normal operation in less than 250 μ s (typical)

JTAG

QuickLogic ArcticLink Solution Platform supports IEEE 1149.1 boundary scan or post-manufacturing testability. External access to this feature can be completely disabled.

Solution Highlights

- Integrated, single-chip solution for multiple peripheral host controllers and interfaces to reduce both system BOM cost and board space.
- Flexible platform with configurable Hi-Speed (HS) USB 2.0 On-The-Go (OTG), high speed SDIO, multi-format storage interfaces and programmable fabric for additional proven system blocks and custom functions.
- Fast time-to-market with QuickLogic's complete low power connectivity solutions.

Solution Platform Combining USB, SD/SDIO/MMC/CE-ATA, and Programmable Fabric

The ArcticLink Solution Platform combines a Hi-Speed USB 2.0 OTG controller with built-in PHY, an SD/SDIO/MMC/CE-ATA host controller and 20 Customizable Building Blocks (CBBs) of programmable fabric for additional proven system blocks, custom functions and glue logic. QuickLogic provides a portfolio of proven system blocks such as PCI, IDE, NAND controller, high-speed SPI and Bluetooth2.X UART.

Because Hi-Speed USB 2.0 OTG and SD/SDIO/MMC/CE-ATA host controllers are being used in almost every handheld device in the mobile market today, they are implemented in the hard logic to yield the optimal area, performance, cost and power consumption. QuickLogic's lowest power programmable fabric, based on QuickLogic's patented ViaLink technology, provides ultimate flexibility, allowing customers to quickly make changes to their system and differentiate their products from their competitors.

Table 1 summarizes the ArcticLink Solution Platform features.

Table 1: ArcticLink Solution Platform

Features		QL1A100
Customizable Building Blocks (CBBs)		20
Max I/O		120
RAM Modules		7
FIFO Controllers		7
RAM bits ^a		36,864
CCM (110-ball WLCSP and 196-ball TFBGA packages only)		1
Packages	WLCSP (10 x 11 array)	110
	TFBGA (8 mm x 8 mm)	121
	TFBGA (12 mm x 12 mm)	196
Hi-Speed USB 2.0 OTG Controller with DMA, ULPI Interface and On-Chip PHY		1
SD/SDIO/MMC/CE-ATA Controller		1
Scratchpad SRAM Bytes		8 K

a. There are eight RAM blocks, two of which are concatenated.

Table 2 shows the maximum usable I/Os available in each VCCIO bank.

Table 2: QL1A100 Maximum Usable I/Os

Device	VCCIO Banks				Total Maximum Usable I/Os
	Bank A	Bank B	Bank C	Bank D	
110 WLCSP (10 x 11 array)	15	21	12	15	63
121 TFBGA (8 mm x 8 mm)	10	20	12	18	60
196 TFBGA (12 mm x 12 mm)	30	34	12	44	120

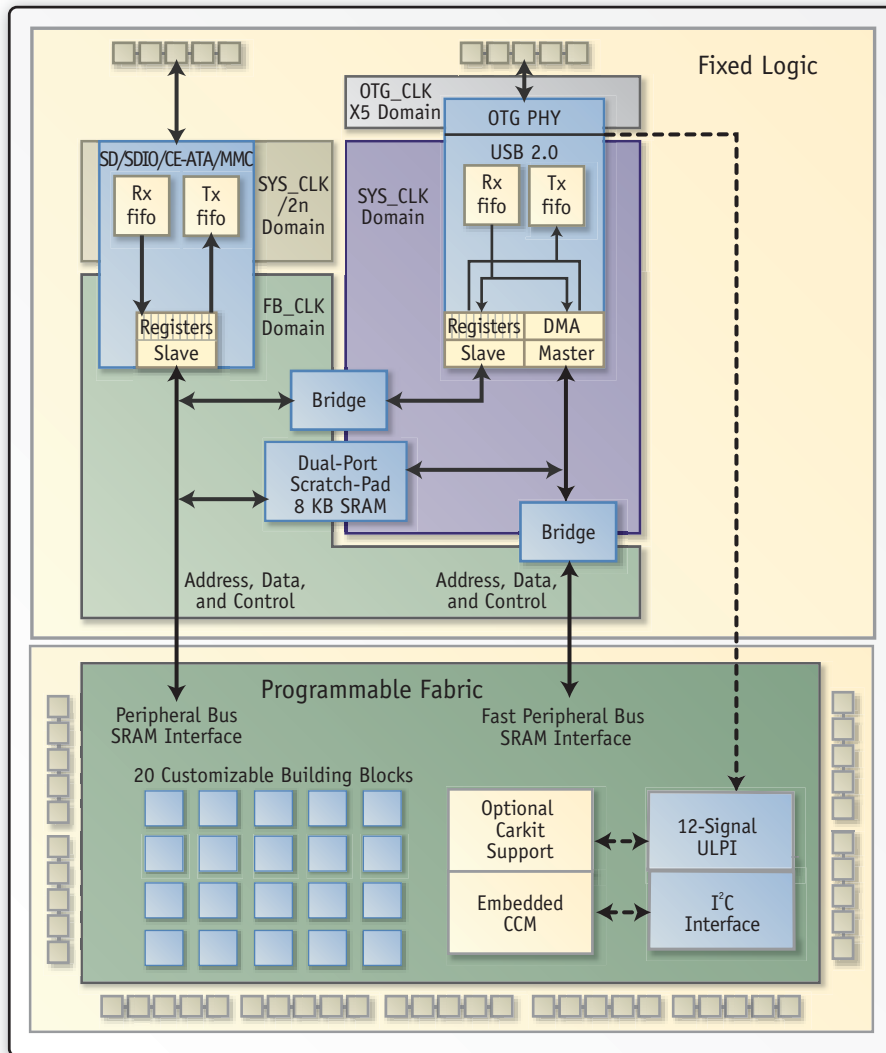
Table 3 summarizes the type and size of the proven system blocks provided by QuickLogic.

Table 3: Proven System Blocks Provided by QuickLogic

Proven System Blocks for Each Technology Segment	
Storage	Intelligence
• IDE/P-ATA Host Controller	• Direct Memory Access (DMA)
• CE-ATA Host Controller	• Smart Data Transfer (SDT)
• NAND Flash Controller	• Data Aggregator (DA)
• Secure Digital (SD) Card Host Controller	Security and Custom Options
• Compact Flash (CF) Host Controller	• Content Protection for Recordable Media (CPRM)
• Multimedia Card (MMC) Controller	• Serial ID
• Memory Stick (MS) Controller	Network
• Managed NAND Controller with Boot Capability	• SDIO Client
• Optical Drive Controller (ATAPI)	• High-Speed SDIO Controller
Video and Imaging	• MiniPCI for Ethernet, Wi-Fi/WiMAX Controller
• X/Y Swap	• SPI Controller
• High-Definition LCD Controller	• Bluetooth 2.x + EDR High-Speed UART

Figure 1 is a block diagram of the ArcticLink Solution Platform.

Figure 1: ArcticLink Solution Platform Block Diagram

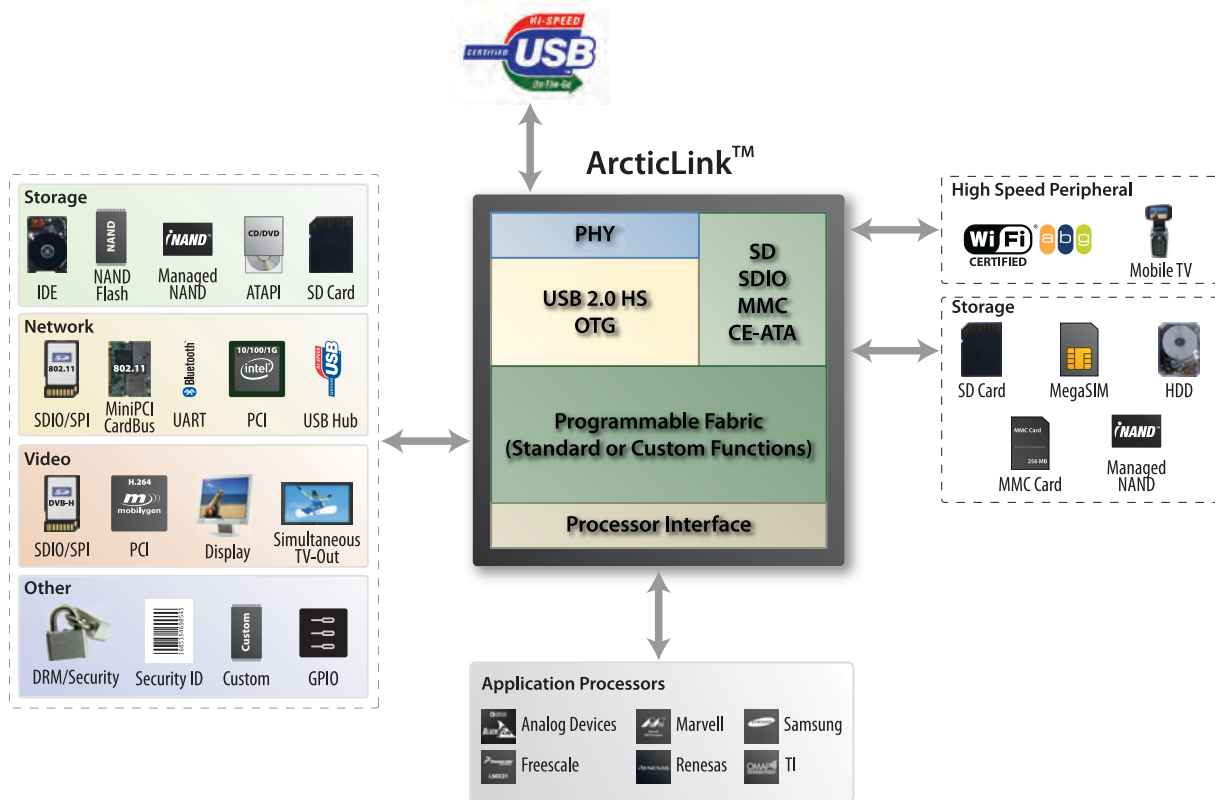


Applications Overview

As shown in **Figure 2**, the ArcticLink Solution Platform consists of three main modules: HS USB 2.0 OTG with PHY, SDIO/SD/MMC/CE-ATA, and programmable fabric. This highly integrated, yet flexible architecture makes it the ideal platform to implement processor companion solutions for smartphones, portable media players (PMP), portable navigation devices (PND), controllers, ePOS terminals, wireless data cards and ExpressCards.

The ArcticLink Solution Platform can be used to replace up to five discrete components, reducing BOM cost and saving board space. It gives developers the ability to harness a wide variety of interfaces with ultra-low power consumption. QuickLogic also provides proven system blocks, software drivers, documentation, reference schematics and support to help accelerate time-to-market.

Figure 2: ArcticLink Connectivity Solutions



Full System Design Support

QuickLogic provides a full range of services and libraries to address a development team's needs such as hardware design support, software drivers, and packaging.

On the hardware development front, QuickLogic supports customers in two ways. First, its Customer Solutions Architects (CSAs) help development teams determine the best way to utilize a CSSP platform in their design. Working closely with the development team's designers, the CSAs help create detailed specifications for the functionality and performance of a customized CSSP.

Once the specifications are complete, QuickLogic's System Solution Team (SST) steps in to implement the design. The SST handles the details of configuring the personality of hard-logic blocks, implementing additional standard functions in the programmable fabric, and implementing the customer's unique functions in the fabric. Support from the SST carries through the design phase into test and system integration. SST members work along side customer development team members at the customer site to ensure that the customized CSSP functions as intended.

To aid a development team's software development effort, QuickLogic supports its CSSPs and library logic blocks with a full range of device drivers. Drawing on its experience with Windows® CE, Windows Mobile®, and Linux® operating systems, QuickLogic has created drivers for each OS for every block. The drivers are optimized for the CSSP implementation and are fully supported during the customer's hardware/software integration phase.

Fixed Logic Building Blocks

Hi-Speed USB 2.0 OTG Controller

The on-chip Hi-Speed USB 2.0 OTG controller is a Dual-Role Device (DRD) that supports host and device functions.

The Hi-Speed USB 2.0 OTG Controller main features include:

- Fully compliant with *Universal Serial Bus Specification, Revision 2.0*.
- Fully compliant with the *On-The-Go Supplement to the USB 2.0 Specification, Revision 1.0a*
- Integrated USB 2.0 OTG port capable of high-speed (HS, 480 Mbps), full-speed (FS, 12 Mbps), and low-speed (LS, 1.5 Mbps) transfers
- Integrated PHY with dedicated Internal Phase-Locked Loop (PLL) with external 12 MHz input for low EMI
- Supports both Point-to-Point and Multi-Point (root hub) applications
- Optional ULPI HS/Full-Speed USB 1.1 Shared-Pin Interface via fixed logic/programmable fabric interface
- Optional I²C™ compatible serial bus for OTG control in Full-Speed USB 1.1 mode available via fixed logic/programmable fabric interface
- Double-buffering scheme for improved throughput and data transfer capabilities
- Supports OTG Host Negotiation Protocol (HNP) and Session Request Protocol (SRP)
- Supports suspend and remote wake-up
- Supports external charge pump source for applications requiring higher current requirements of VBUS

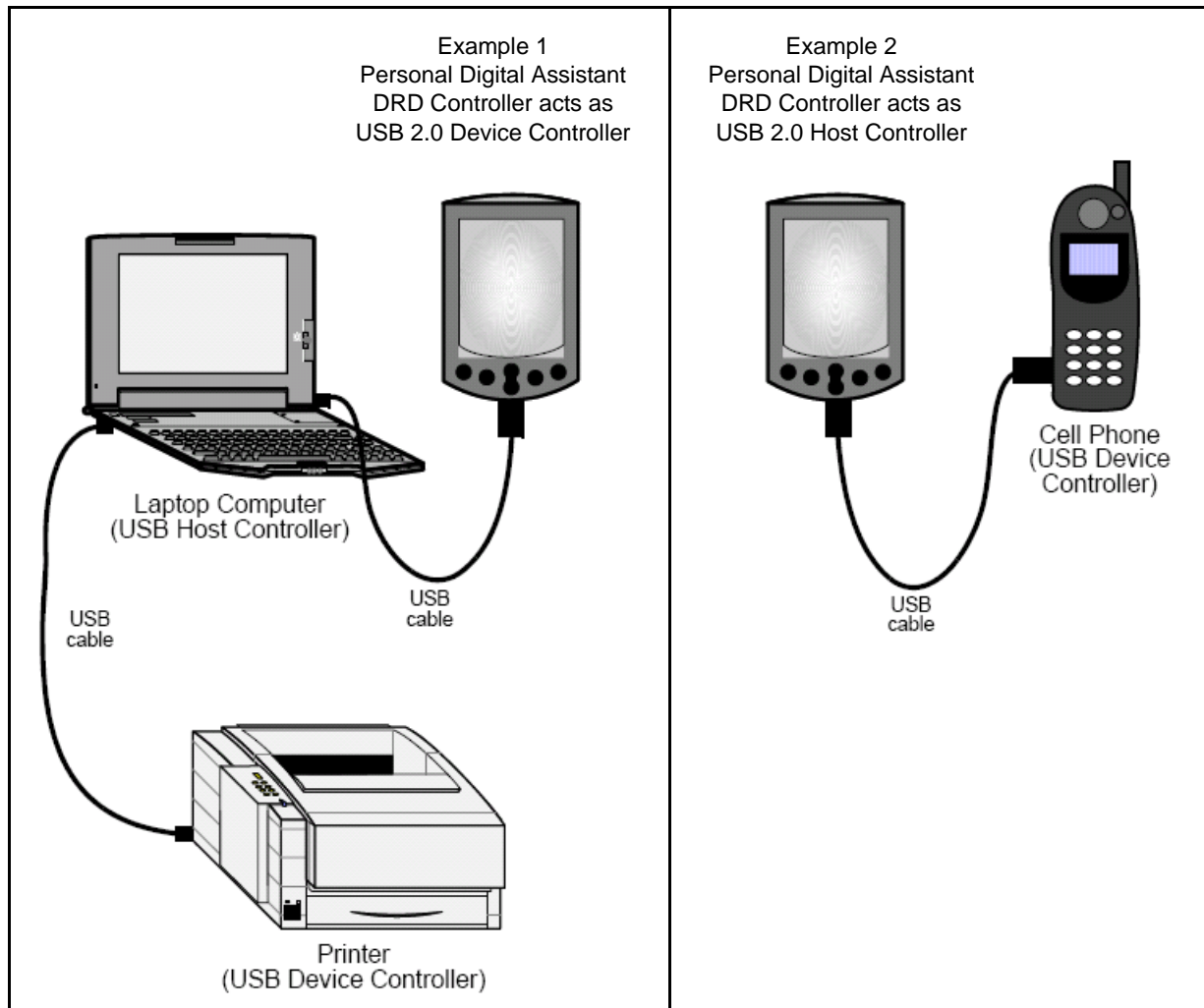
- Configurable power management features
- Integrated 5.2 KB FIFO
- Supports packet-based, dynamic FIFO memory allocation, for flexible, efficient use of RAM
- Total of sixteen endpoints comprising of:
 - One fixed bidirectional control endpoint
 - One software programmable IN or OUT endpoint
 - Seven IN endpoints
 - Seven OUT endpoints

The DRD controller is optimized for the following applications and systems:

- Portable electronic devices
- Point-to-point applications (no hub, direct connection to HS, FS, or LS device)
- Multi-point applications (as an embedded USB host) to devices (hub and split support)

Figure 3 shows typical scenarios for a Personal Digital Assistant (PDA) application. In Example 1 the laptop computer contains a USB host for the PDA and printer peripherals. In Example 2 the DRD controller in the PDA acts as the USB host for the cell phone peripheral.

Figure 3: Typical DRD Controller Applications



USB DMA Controller

The USB DMA Controller in the USB 2.0 Controller (see [Figure 1](#) on page 4) can transfer data to and from the Fabric or the dual-port scratchpad 8 KB SRAM.

The USB 2.0 OTG Controller is software selectable to be in Slave mode or DMA mode through the use of the DMAEn bit of the GAHBCFG register. In Slave mode, data transfers to/from the USB Tx/Rx FIFOs is handled by the software driver running on the attached CPU. In DMA mode, data transfers between the USB Tx/Rx FIFOs and the 8 KB SRAM (or programmable fabric memory controller) is handled by the internal USB DMA Controller.

The internal USB DMA Controller translates internal DMA requests/cycles into Fast Peripheral/SRAM Interface bridge Master requests/cycles. The DMA address, transfer count, and packet count registers reside in the USB Slave Registers block. The selected channel's address is provided as input into the USB DMA Controller. The software driver sets up the transfer and the USB interrupts the processor only on transfer completion or an error condition.

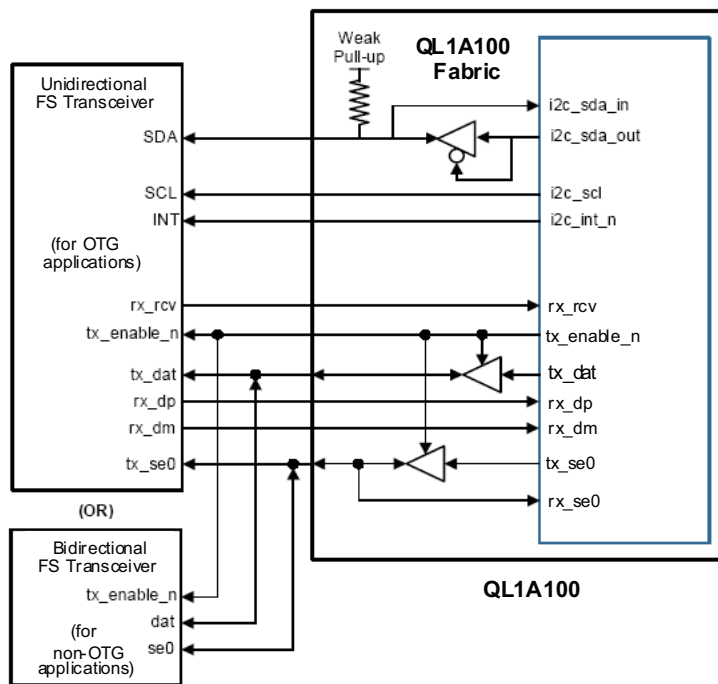
2-Wire Serial and ULPI to Fabric Interface

I²C Compatible Serial Bus

I²C (Inter-Integrated Circuit) is a simple bidirectional 2-wire serial bus which enables devices to communicate directly with each other.

The I²C compatible serial bus can be used for OTG control of a Full-Speed USB 1.1 OTG Transceiver. **Figure 4** shows unidirectional and bidirectional Full-Speed USB 1.1 OTG Transceiver and optional I²C compatible serial connections. See **Table 4** for ULPI pin sharing modes.

Figure 4: USB 1.1 6-Pin Unidirectional with 2-Wire Serial for OTG and 3-Pin Bidirectional Non-OTG Full-Speed Serial Transceiver Dedicated Interface – I²C Compatible Serial Bus



The I²C compatible serial bus interface can also be used for the support of Mini USB Analog CarKit Interface CEA-936 in OTG and non-OTG configurations and is not intended for use with other devices. Refer to the targeted ULPI CarKit PHY documentation for more information regarding the use of I²C compatible serial bus interface with ULPI CarKit PHYs.

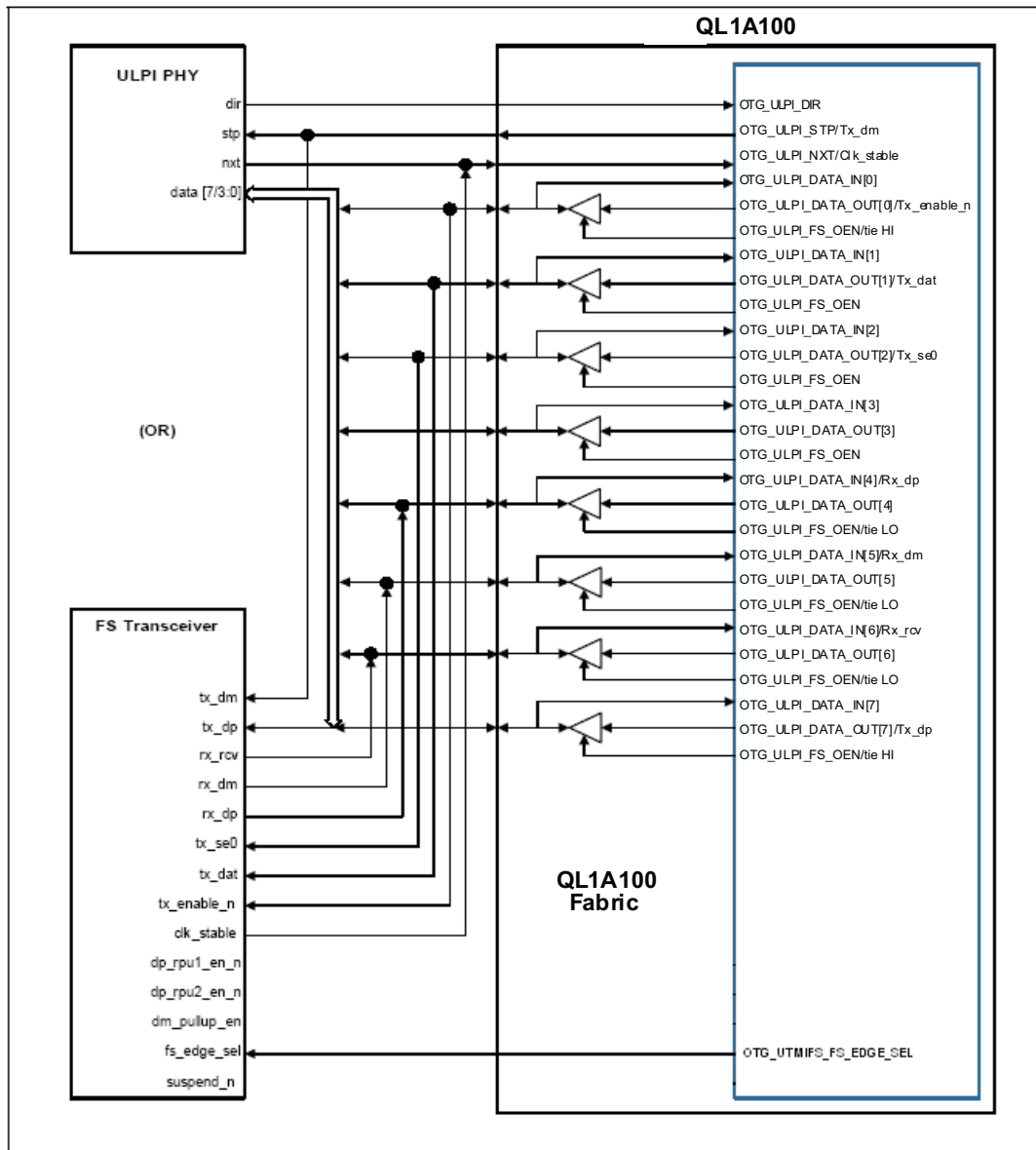
UTMI+ Low Pin Interface (ULPI)

ULPI defines an interface between USB link controllers and the PHYs or transceivers that drive the actual bus. ULPI is designed to reduce the pin count of HS USB PHYs thus minimizing the cost and footprint of external PHY chips and reducing the pin count to the USB link controller. The available ULPI interface on the

ArcticLink Solution Platform is intended for connecting an external ULPI CarKit PHY or implementing PHY-less chip-to-chip communication. Use the integrated HS PHY on the ArcticLink Solution Platform for systems that do not require ULPI CarKit or PHY-less chip-to-chip communication support.

Figure 5 shows the QL1A100 device connected to a ULPI PHY or Full-Speed USB 1.1 OTG Serial Transceiver.

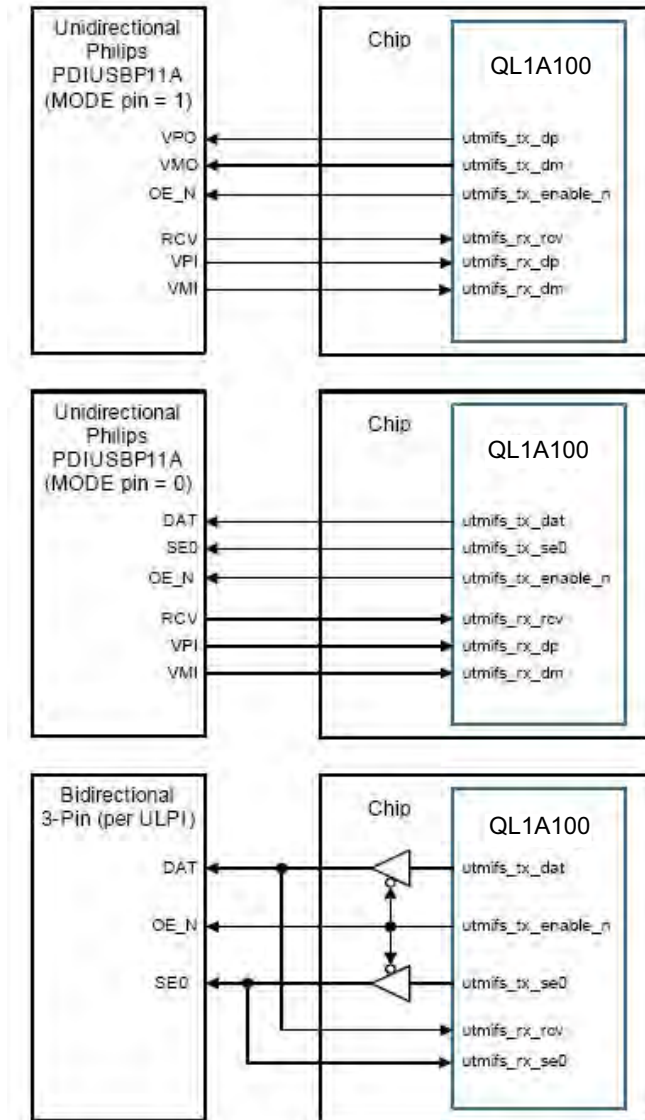
Figure 5: ULPI HS PHY/USB 1.1 Serial Transceiver Shared-Pin Interface



NOTE: Not all FsLs serial pins are required for all FS Transceivers or FS Hubs, it is shown only for reference and connectivity purposes. The ULPI and FS clocks pins are shared (not shown), external clock switching may be required. OTG and I²C compatible serial pins are not shared (not shown).

Figure 6 shows sample FS/LS serial connections for a Philips PDIUSBP11A USB Transceiver and 3-pin configuration as part of the ULPI (optional) FsLs Serial support.

Figure 6: Philips PDIUSBP11A and ULPI 3-Pin Transceiver Connections



ULPI Vendor Control access is provided in the ArcticLink Solution Platform is described in Chapter 7 of the *ArcticLink Solution Platform User Manual*. Software can program the PHY Vendor Control register which is translated as a register read/write command in ULPI for ULPI PHY register access.

ULPI Modes of Operation

The ArcticLink Solution Platform supports ULPI interface (8-bit SDR, 6-pin FsLs Serial, 3-pin FsLs Serial and Carkit) as shown in **Table 4**.

Table 4: OTG ULPI Signal Modes

ULPI Synchronous HS Mode (8-bit SDR)	FS Serial Mode		Carkit Mode
	6-Pin	3-Pin	
ULPI_DATA[0]	Tx_enable	Tx_enable	Txd
ULPI_DATA[1]	Tx_dat	dat	Rxd
ULPI_DATA[2]	Tx_se0	se0	Reserved
ULPI_DATA[3]	Interrupt	Interrupt	Interrupt
ULPI_DATA[4]	Rx_dp	Unused	Unused
ULPI_DATA[5]	Rx_dm	Unused	Unused
ULPI_DATA[6]	Rx_rcv	Unused	Unused
ULPI_DATA[7]	Tx_dp	Unused	Unused
ULPI_CLK (60 MHz)	Clk (48 MHz)	Clk (48 MHz)	Unused
ULPI_DIR	Dir	Dir	Dir
ULPI_NXT	Nxt	Nxt	Nxt
ULPI_STP	Stp/Tx_dm	Stp	Stp
OTG_ULPI_FS_OEN	OTG_ULPI_FS_OEN	OTG_ULPI_FS_OEN	OTG_ULPI_FS_OEN
Unused	OTG_UTMIFS_RX_SE0	OTG_UTMIFS_RX_SE0	Unused

The ArcticLink Solution Platform supports the optional FsLs Serial mode as per the ULPI specification for ULPI PHYs with FsLs support or standalone FS transceivers both using a shared pin ULPI interface as shown in **Figure 5** on page 10.

NOTE: The ArcticLink Solution Platform does not support FsLs Serial modes of ULPI PHYs which require FsLs Serial modes to operate on frequencies other than 48 MHz. The ArcticLink Solution Platform also requires PHYs to internally switch the ULPI Clock output to 60 MHz and 48 MHz for ULPI and FsLs modes respectively.

Programming FsLs Serial Mode for standalone FS transceivers and integrated ULPI PHYs:

- The mode is selected by setting the GUSBCFG.ULPIFsLs, GUSBCFG.PHYSel, and GUSBCFG.ULPI_UTMI_Sel registers, and must be set before any USB event (see the *ArcticLink Solution Platform User Manual* for details)
- In ULPI FsLs Host mode, the application must program HCFG.FSLSPclksel to “01” so the internal clock is running at 48 MHz
- In ULPI FsLs Device mode, the application must program DCFG.DevSpd to “11” to denote the maximum speed the ArcticLink Solution Platform can support in this mode
- To select the 6-pin FsLs Serial mode, the application must program the GUSBCFG.FSIntf to “0”
- To select the 3-pin FsLs Serial mode, the application must program the GUSBCFG.FSIntf to “1”

ULPI Interface Initialization

After the ULPI is reset and the PHY is initialized, depending on how the registers are set, ULPI or 6-pin FsLs serial or 3-pin FsLs serial modes are enabled.

For FsLs Serial modes of ULPI PHYs, “Interface Control” register is set.

During 6-pin full-speed/low-speed Serial mode, the ulpi data bus is mapped to signal definitions as shown in **Table 4** under the “Serial Mode 6-pin” column.

During 3-pin full-speed/low-speed Serial mode, the ulpi data bus is mapped to signal definitions as shown in **Table 4** under the “Serial Mode 3-pin” column.

NOTE: The following signals are provided and not pin shared but may be required for some FS transceiver applications:

- OTG_utmifs_rx_se0: UTMI FS Serial SE0 assertion received
- OTG_utmifs_fs_edge_sel: UTMI FS selects low/full-speed slew rate

NOTE: OTG_ULPI_CLK is pin shared with ULPI and FsLs Serial mode for 60 MHz and 48 MHz interface clocks respectively.

For FsLs Serial modes of ULPI PHYs, to exit Serial mode, the ArcticLink Solution Platform receives an interrupt from the PHY, and the PHY registers are updated.

Carkit Support in Fabric

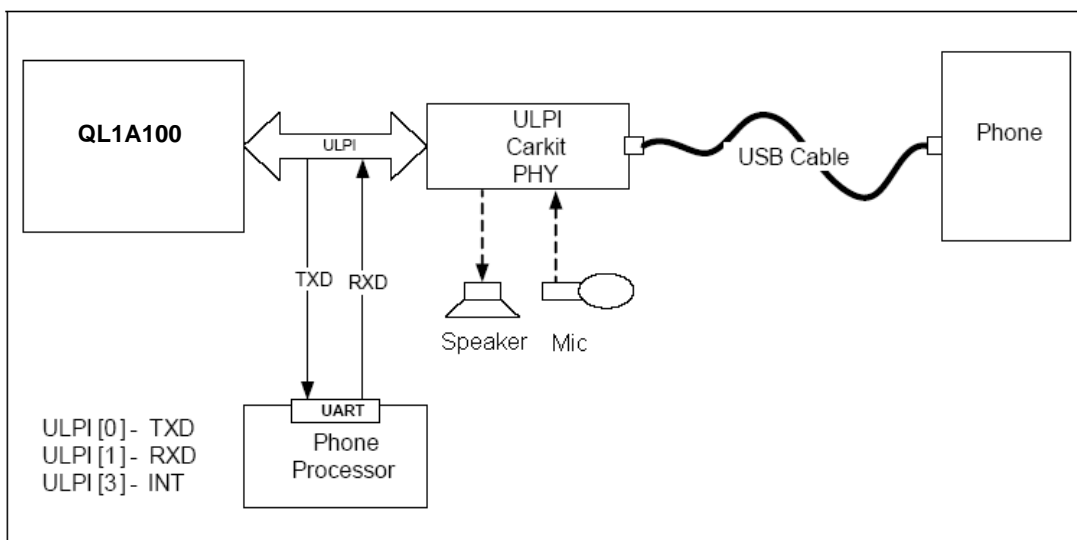
Typically, USB-ULPI Carkit PHYs support three main modes: HS USB, UART and Audio.

The ArcticLink Solution Platform Carkit support fulfills the USB responsibility of multiplexing the ULPI data lines between UART and USB-ULPI modes, and receiving Carkit interrupts from the PHY.

For a more complete Carkit implementation using the ArcticLink Solution Platform, a Carkit or Phone requires additional elements such as Carkit logic or processor blocks for configuration and control, UARTs, and separate I/Os for Speaker and Mic.

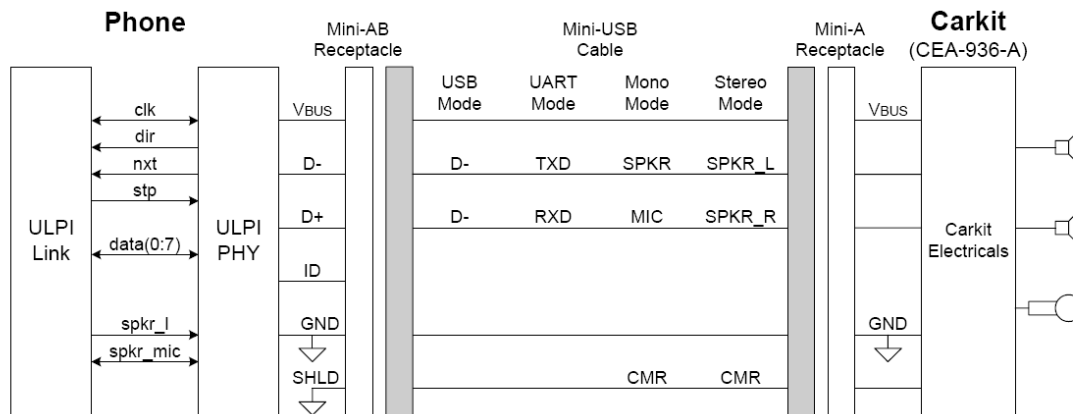
Figure 7 shows the ArcticLink Solution Platform in an in-dash Carkit.

Figure 7: ArcticLink Solution Platform in an In-Dash Carkit Application Block Diagram



The **Figure 8** shows the basic architecture of the ULPI Carkit interface, and the allowed signaling modes.

Figure 8: ULPI Carkit Interface Architecture



The Carkit application for the ArcticLink Solution Platform can be a cell phone or Carkit. For Carkit applications, the ULPI PHY resistively pulls down the ID. The ULPI PHY on a cell phone can monitor the resistive pull-down to detect a Carkit connection.

For external ULPI Carkit PHY applications, in USB mode it should operate as a standard HS USB-ULPI capable interface. The Speaker (SPK) and Microphone (MIC) are analog circuits.

The ULPI and UART are digital circuits that share the ULPI data bus as shown in **Figure 8** and as mentioned in **Table 4**, column Carkit Mode. ULPI or UART modes can be selected via the software application. The selection is accomplished by setting the Carkit Mode bit in the Interface Control register and setting the TxdEn and RxdEn bits in the Carkit Control register of the ULPI PHY. Software can access ULPI PHY internal registers using register read/writes to the ArcticLink Solution Platform's vendor control access.

When the application selects ULPI or UART interfaces the Carkit interrupts are received by the ArcticLink Solution Platform through RXCMD, bit[7] or ulpi_data[3] respectively.

Full-Speed USB 1.1 Hub Support in Fabric

An optional Full-Speed USB 1.1 Hub can be implemented within the ArcticLink Solution Platform Fabric in lieu of the optional single Full-Speed USB 1.1 port. The optional hub connects to the single Full-Speed USB 1.1 serial upstream port and in turn provides multiple downstream ports that can be routed to various GPIOs. Note that an external 48 MHz source clock is required as input to the ArcticLink Solution Platform for both the single and multi port Full-Speed USB 1.1 serial implementations.

USB Charge Pump (External)

A charge pump is necessary for USB Host or USB OTG A-device mode implementations to supply a 5 V source to attached devices.

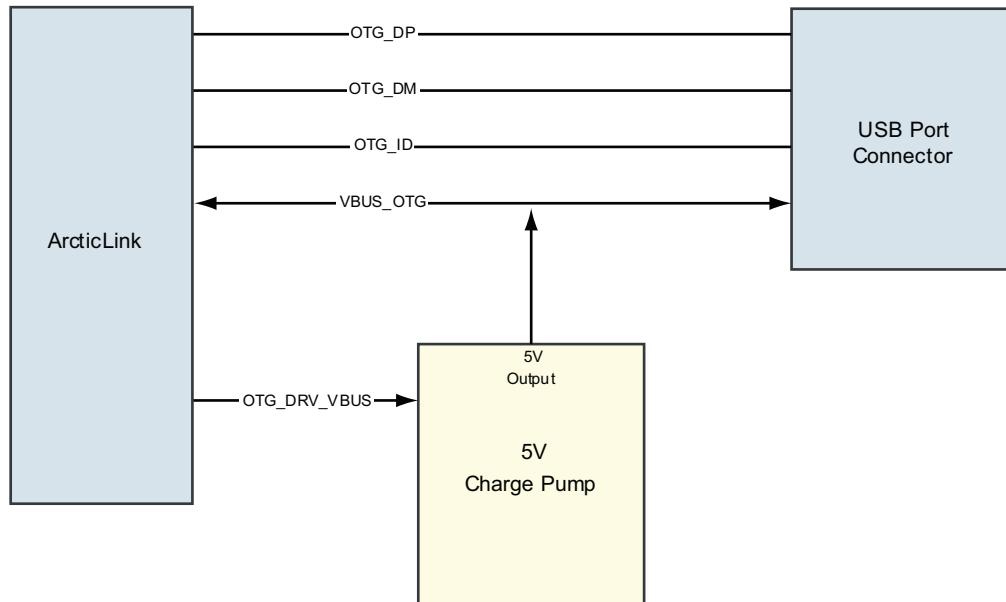
A large selection of charge pumps are available and should be selected by the designer depending on system requirements such as:

- +4.8 V to +5.25V OTG-compatible output on VBUS.
- 8 mA (minimum for OTG applications), 100 mA (minimum for low-powered Host applications), 500 mA (recommended) output current, depending on the type of devices to be powered by the charge pump.

Consult the selected charge pump data sheet for details on its connectivity.

Figure 9 illustrates a typical external charge pump implementation connected to the ArcticLink Solution Platform and a USB connector.

Figure 9: USB Charge Pump Connectivity Block Diagram



SD/SDIO/MMC/CE-ATA Host Controller

The SD/SDIO/MMC/CE-ATA Host Controller is compliant with *SD Host Controller Standard Specification, Version 2.0* and supports MMC Specification, Version 4.1.

The SD/SDIO/MMC/CE-ATA Host Controller main features include:

- Supports MMC 4.1
- Supports clock rate up to 52 MHz
- Supports SD and SDIO
- Supports I/O commands 52 and 53
- Supports 1-bit, 4-bit and 8-bit data modes
- Supports SDIO device interrupt in 1-bit, 4-bit, and 8-bit modes
- Supports block size up to 512 bytes
- Dynamic Buffer Management to increase data throughput
- Available DREQ signal for Marvell® PXA processor to improve processor DMA performance

The CE-ATA mode SD/SDIO/MMC/CE-ATA Host Controller is compliant with *CE-ATA Digital Protocol, Revision 1.1RC* and based on the *SD Host Controller Standard Specification, Version 2.0*.

The CE-ATA mode main features include:

- Supports clock rate up to 52 MHz
- Supports CE-ATA commands 39, 60, and 61
- Supports CE-ATA Command Completion Interrupt from device to host
- Supports CE-ATA Command Completion Signal Disable protocol generation
- Supports 1-bit, 4-bit and 8-bit data modes
- Supports 512-byte block sizes
- Dynamic Buffer Management to increase data throughput
- Available DREQ signal for Marvell PXA processor to improve processor DMA performance

8 KB On-Chip Scratchpad Memory

A scratchpad memory is provided on-chip for temporary storage as well as to facilitate data flow between the USB controller and external host processor. The scratchpad is dual-ported with one port connected to the internal bus closely coupled with the Hi-Speed USB 2.0 OTG Controller, while the other port is connected to the fabric master SRAM interface and source clock. This enables the internal bus logic to run at a much higher clock frequency independent of the programmable fabric design frequency.

Fast Peripheral/SRAM Interface Bridge for Programmable Fabric Memory Controller

To improve performance, external bus mastering can be achieved through the on-chip Fast Peripheral/SRAM Interface bridge for systems where bus mastering is an option. This bridge provides a way for the internal DMA engine in the Hi-Speed USB 2.0 OTG Controller to directly access external memory through a memory controller implemented in the programmable fabric. This bridge provides a clock domain crossing to allow the internal bus clock to run independently of the programmable fabric memory controller clock.

Programmable Fabric Architectural Overview

The QuickLogic ArcticLink Solution Platform features a high performance and low power programmable fabric to implement additional proven system blocks. The programmable fabric consists of 20 customizable building blocks (CBB) to implement combinations of different interfaces required by the customer design specifications, which results in a much higher integration, more flexibility and lower system BOM costs. A CBB is a unit of measurement that represents the on-chip logic that can be used to implement a variety of proven system blocks (such as SDIO, PCI, IDE, CE-ATA and NAND Flash controller), custom logic, or other system level functions (see **Table 3** on page 3 for a list of proven system blocks).

RAM Modules

The ArcticLink Solution Platform has 4-Kbit (4,608 bits) RAM blocks which are used primarily as buffers and FIFOs to significantly improve system performance. The RAM features include:

- Independently configurable read and write data bus widths
- Independent read and write clocks

- Horizontal and vertical concatenation
- Write byte enables
- Selectable pipelined or non-pipelined read data
- Ability to generate true dual-port RAMs through concatenation with completely independent read/write ports and clock domains

Embedded FIFO Controllers

Every RAM block can be implemented as a synchronous or asynchronous FIFO. There are built-in FIFO controllers that allow for varying depths and widths without requiring programmable fabric resources.

The ArcticLink Solution Platform FIFO controller features include:

- x9, x18 and x36 data bus widths
- Independent PUSH and POP clocks
- Independent programmable data width on PUSH and POP sides
- Configurable synchronous or asynchronous FIFO operation
- 4-bit PUSH and POP level indicators to provide FIFO status outputs for each port
- Pipelined read data to improve timing

Configurable Clock Manager

The CCM includes a Phase Locked Loop (PLL) component, a frequency multiplier, and phase modifier. The PLL is a closed loop frequency control system that detects the phase difference between the input and output signals and aligns them. The frequency multiplier adds the ability to multiply the input frequency by a configurable factor of two or four. Additionally, the phase modifier supports the ability to shift the output frequency phase and offset by a given time delay.

The QuickLogic ArcticLink 110-ball WLCSP and 196-ball TFBGA devices have one CCM. The CCM features include:

- Input frequency range from 25 MHz to 200 MHz
- Output frequency range from 25 MHz to 200 MHz
- Output jitter is less than 200 ps peak-to-peak
- Two outputs: pullout0 (with 0° phase shift), and pullout1 (with an option of 0°, 90°, 180°, or 270° phase shift plus a programmable delay).
- Programmable delay allows delays up to 2.5 ns at 250 ps intervals
- Output frequency lock time in less than 10 μs

The reset signal can be routed from a clock pad or generated using internal logic. The lock_out signal can be routed to internal logic and/or an output pad. CCM clock outputs can drive the global clock networks, as well as any general purpose I/O pin. Once the CCM has synchronized the output clock to the incoming clock, the

lock_out signal will be asserted to indicate that the output clock is valid. Lock detection requires at least 10 μ s after reset to assert lock_out. The ArcticLink Solution Platform CCM has three modes of operation, based on the input frequency and desired output frequency. **Table 5** indicates the features of each mode.

Table 5: CCM PLL Mode Frequencies

Output Frequency	Input Frequency Range	Output Frequency Range	PLL Mode
x1	25 MHz to 200 MHz	25 MHz to 200 MHz	PLL_MULT1
x2	15 MHz to 100 MHz	30 MHz to 200 MHz	PLL_MULT2
x4	10 MHz to 50 MHz	40 MHz to 200 MHz	PLL_MULT4

Very Low Power (VLP) Mode

The QuickLogic ArcticLink Solution Platform has a unique feature, referred to as VLP mode, which reduces power consumption by placing the device in standby. Specifically, VLP mode can bring the programmable fabric standby current down to less than 10 μ A at room temperature when no incoming signals are toggled. VLP mode is controlled by the VLP pin. The VLP pin is active low, so VLP mode is activated by pulling the VLP pin to ground. Conversely, the VLP pin must be pulled to 3.3 V for normal operation.

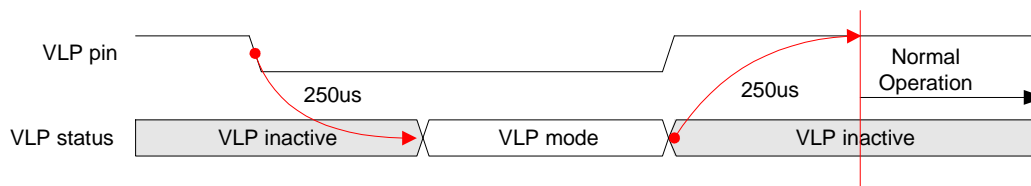
When the ArcticLink Solution Platform goes into VLP mode, the following occurs:

- All register values in the programmable fabric and GPIO are preserved
- All RAM cell data is retained
- The outputs from all GPIO to the internal logic are tied to a weak '1'
- GPIO outputs drive the previous values
- GPIO output enables retain the previous values
- Clock pad inputs are gated
- The CCM is held in the reset state

The entire operation from normal mode to VLP mode requires 250 μ s (300 μ s maximum). As mentioned in the VLP behavioral description above, the output of the GPIO to the internal logic is a weak '1'. Therefore, to preserve data retention GPIO should not be used for a set, reset, or clock signal.

As the Solution Platform exits out of VLP mode, the data from the registers, RAM, and GPIO will be used to recover the functionality of the device. Furthermore, since the CCM is in a reset state during VLP mode, it will have to re-acquire the correct output signals before asserting lock_out. The time required to go from VLP mode to normal operation is 250 μ s (300 μ s maximum). **Figure 10** displays the delays associated with entering and exiting VLP mode.

Figure 10: Typical VLP Mode Timing



Electrical Specifications

DC Characteristics

The DC Specifications are provided in **Table 6** through **Table 10**.

Table 6: Absolute Maximum Ratings

Parameter	Value	Parameter	Value
VCC, VCCP_OTG, and CCM_VCC Voltage	-0.5 V to 2.2 V	Latch-up Immunity	±100 mA
VCCIO, VCCA_OTG, and VCCIO_ASSP Voltage	-0.5 V to 4.0 V	ESD Pad Protection	2 kV
VREF Voltage	-0.5 V to 2.0 V	ESD Pad Protection (USB D+, D-, ID, VBUS_OTG)	8 kV
Input Voltage VBUS_OTG, OTG_DP, and OTG_DM	-0.5 V to 5.0 V	Leaded Package Storage Temperature	-65° C to + 150° C
Input Voltage All other I/Os	-0.5 V to 4.0 V	Laminate Package (BGA) Storage Temperature	-55° C to + 125° C

Table 7: Recommended Operating Range

Symbol	Parameter	Industrial		Commercial		Unit
		Min.	Max.	Min.	Max.	
VCC, VCCP_OTG and CCM_VCC	Supply voltage	1.71	1.89	1.71	1.89	V
VCCIO and VCCIO_ASSP	I/O input tolerance voltage	1.71	3.60	1.71	3.60	V
TJ	Junction temperature	-40	100	0	85	°C
VCCA_OTG	USB OTG PHY I/O input tolerance voltage	3.0	3.6	3.0	3.6	V

Table 8: Recommended Power Supply Ripple Noise

Symbol	Parameter	Conditions	Min.	Max.	Unit
VCC	Digital Supply Voltage	ALL	-50	+50	mV
VCCP_OTG and VCCA_OTG	Analog Supply Voltage for USB OTG core	<4 MHz	-10	+10	mV
		>4 MHz	-50	+50	mV
		<160 MHz	-50	+50	mV
CCMVCC	Analog Supply Voltage for the Fabric	<4 MHz	-10	+10	mV
		>4 MHz	-30	+30	mV
		<160 MHz	-30	+30	mV

Table 9: DC Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_I	I or I/O Input Leakage Current	$V_I = V_{CCIO}$ or GND	-	-	1	μA
I_{OZ}	3-State Output Leakage Current	$V_I = V_{CCIO}$ or GND	-	-	1	μA
C_I	I/O Input Capacitance	$V_{CCIO} = 3.6 V$	-	-	10	pF
C_{CLOCK}	Clock Input Capacitance	$V_{CCIO} = 3.6 V$	-	-	10	pF
I_{REF}	Quiescent Current on INREF	-	-	-	5	μA
I_{PD}	Current on programmable pull-down	$V_{CCIO} = 3.6 V$	-200	-	-50	μA
		$V_{CCIO} = 2.75 V$	-150	-	-25	μA
		$V_{CCIO} = 1.89 V$	-100	-	-10	μA
I_{PU}	Current on programmable pull-up	$V_{CCIO} = 3.6 V$	50	-	200	μA
		$V_{CCIO} = 2.75 V$	25	-	150	μA
		$V_{CCIO} = 1.89 V$	10	-	100	μA
I_{VLP}	Quiescent Current on VLP pin	$VLP=3.3$	-	1	10	μA
I_{CCM}	Quiescent Current on CCMVCC	$VCC=1.89 V$	-	1	10	μA
I_{VCC}	Quiescent Current	$VLP=GND$	-	5	40	μA
		$VLP=3.3V$	-	40	100	μA
I_{VCCIO}	Quiescent Current on VCCIO	$V_{CCIO} = 3.6 V$	-	2	10	μA
		$V_{CCIO} = 2.75 V$	-	2	10	μA
		$V_{CCIO} = 1.89 V$	-	2	10	μA

Table 10: DC Input and Output Levels^a

Symbol	INREF		V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V_{MIN}	V_{MAX}	V_{MIN}	V_{MAX}	V_{MIN}	V_{MAX}	V_{MAX}	V_{MIN}	mA	mA
LVTTTL	n/a	n/a	-0.3	0.8	2.2	$V_{CCIO} + 0.3$	0.4	2.4	2.0	-2.0
LVC MOS2	n/a	n/a	-0.3	0.7	1.7	$V_{CCIO} + 0.3$	0.7	1.7	2.0	-2.0
LVC MOS18	n/a	n/a	-0.3	0.63	1.2	$V_{CCIO} + 0.3$	0.7	1.7	2.0	-2.0
GTL+	0.88	1.12	-0.3	$INREF - 0.2$	$INREF + 0.2$	$V_{CCIO} + 0.3$	0.6	n/a	40	n/a
PCI	n/a	n/a	-0.3	$0.3 \times V_{CCIO}$	$0.6 \times V_{CCIO}$	$V_{CCIO} + 0.5$	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	1.5	-0.5
SSTL2	1.15	1.35	-0.3	$INREF - 0.18$	$INREF + 0.18$	$V_{CCIO} + 0.3$	0.74	1.76	7.6	-7.6
SSTL3	1.3	1.7	-0.3	$INREF - 0.2$	$INREF + 0.2$	$V_{CCIO} + 0.3$	1.10	1.90	8	-8

a. The data provided in **Table 10** represents the JEDEC and PCI specification. The QuickLogic Solution Platform either meet or exceed these requirements.

Figure 11 and Figure 12 illustrate quiescent current for QL1A100 with VLP = 0 V and 3.3 V.

Figure 11: Quiescent Current for QL1A100 with VLP = 0 V

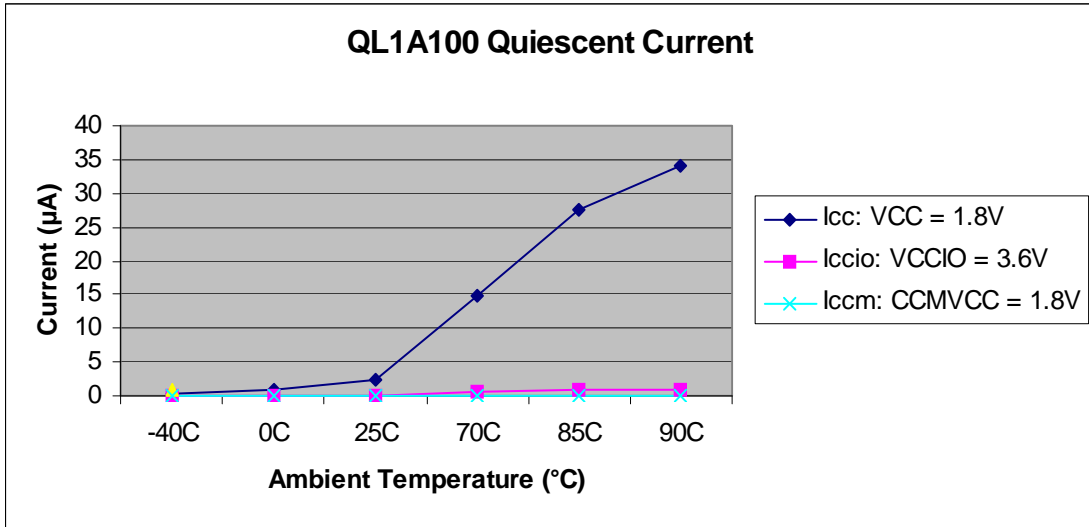
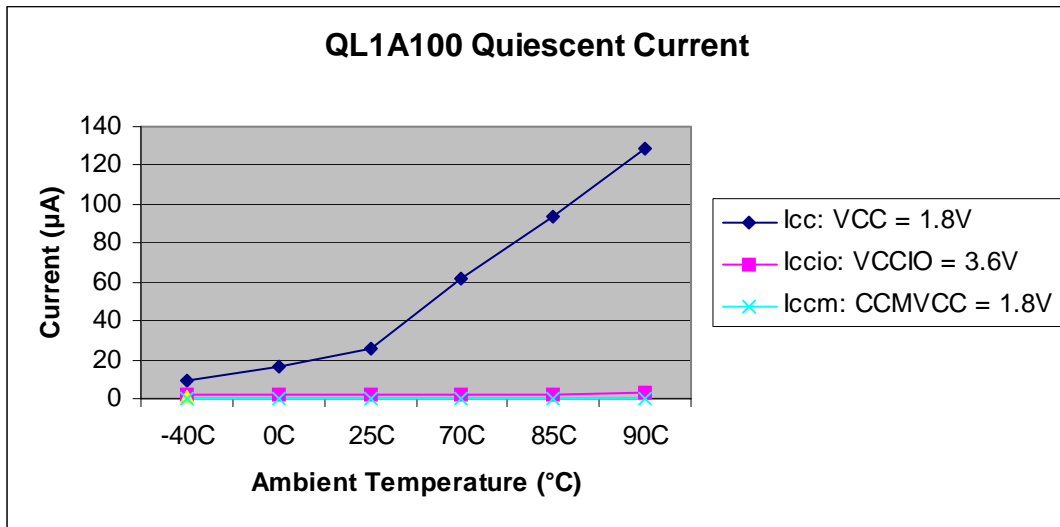


Figure 12: Quiescent Current for QL1A100 with VLP = 3.3 V



AC Characteristics

Hi-Speed USB Timing

Table 11: Hi-Speed USB Timing Characteristics

Symbol	Parameter	Min.	Max.	Unit
$T_{\text{USB_HS_RISE}}$	Hi-Speed USB rise time	0.5		ns
$T_{\text{USB_HS_FALL}}$	Hi-Speed USB fall time	0.5		ns
$T_{\text{USB_FS_RISE}}$	Full-Speed USB rise time	4	20	ns
$T_{\text{USB_FS_FALL}}$	Full-Speed USB fall time	4	20	ns
$T_{\text{USB_LS_RISE}}$	Low-Speed USB rise time	75	300	ns
$T_{\text{USB_LS_FALL}}$	Low-Speed USB fall time	75	300	ns

Programmable Fabric Clock Tree Timing

Table 12 and Table 13 show the USB OTG and Fabric PLL timing requirements.

Table 12: USB OTG PLL Timing Requirements

Symbol	Parameter	Min.	Max.	Unit
$t_{\text{PERIOD_OTG_CLK}}$	12 MHz OTG_CLK period range	83.291	83.375	ns
$t_{\text{JITTER_OTG_CLK}}$	12 MHz OTG_CLK jitter tolerance	-500	+500	ppm

Table 13: Fabric PLL Timing Requirements

Symbol	Parameter	Min.	Max.	Unit
$t_{\text{JITTER_FB_CLK}}$	100 MHz FB_CLK jitter tolerance	-	150	ps

Package Thermal Characteristics

The ArcticLink Solution Platform is available for Commercial (0°C to 85°C Junction) and Industrial (-40°C to 100°C Junction) temperature ranges.

Thermal Resistance Equations:

$$\theta_{JC} = (T_J - T_C) / P \text{ (not applicable for QL1A100 –110-pin WLCSP package)}$$

$$\theta_{JA} = (T_J - T_A) / P$$

$$P_{MAX} = (T_{JMAX} - T_{AMAX}) / \theta_{JA}$$

Parameter Description:

θ_{JC} : Junction-to-case thermal resistance (not applicable for QL1A100 –110-pin WLCSP package)

θ_{JA} : Junction-to-ambient thermal resistance

T_J : Junction temperature

T_A : Ambient temperature

P: Power dissipated by the device while operating

P_{MAX} : The maximum power dissipation for the device

T_{JMAX} : Maximum junction temperature

T_{AMAX} : Maximum ambient temperature

NOTE: Maximum junction temperature (T_{JMAX}) is 100°C. To calculate the maximum power dissipation for a device package look up θ_{JA} from **Table 14**, pick an appropriate T_{AMAX} and use:

$$P_{MAX} = (125^\circ\text{C} - T_{AMAX}) / \theta_{JA}$$

Table 14: Package Thermal Characteristics

Package Description				θ_{JA} (°C/W)			θ_{JC} (°C/W)
Device	Package Code	Package Type	Pin Count	0 LFM	200 LFM	400 LFM	
QL1A100	CSP	WLCSP (10 x 11 array)	110	31.0	27.0	25	NA
	PM	TFBGA (8 mm x 8 mm)	121	33.0	29.0	28.0	10
	PT	TFBGA (12 mm x 12 mm)	196	32.0	28.0	27	8

Power Consumption

USB Power Consumption

Table 15 shows the typical power consumption for a Hi-Speed USB operational with 10 MB file transfer over a 16-bit CPU interface implemented in the programmable fabric. The SDIO clock is turned off.

Table 15: Hi-Speed USB Operational with 10 MB File Transfer

Parameter	Typ. (mA)
Core (1.8 V)	71.01
I/O (3.3 V)	2.02
VDDA (3.3 V) - Analog USB PHY Supply	11.16
VDDP (1.8 V) - USB PHY PLL Supply	3.69
VCCIOASSP (3.3 V)	0.05

Table 16 shows the typical power consumption for a Hi-Speed USB and PHY suspended with the internal and PHY clocks off and Vbus comparator disabled. The 16-bit CPU interface is implemented in the programmable fabric and the SDIO clock is turned off.

Table 16: Hi-Speed USB and PHY Suspended with the Internal and PHY Clocks Off and Vbus Comparator Disabled

Parameter	Typ. (mA)
Core (1.8 V)	13.18
I/O (3.3 V)	0.10
VDDA (3.3 V) - Analog USB PHY Supply	0.15
VDDP (1.8 V) - USB PHY PLL Supply	0.05
VCCIOASSP (3.3 V)	0.05

Table 17 shows the typical power consumption for a Hi-Speed USB and PHY suspended with the internal and PHY clocks off, Vbus comparator disabled, VLP activated and all oscillators shut down (OTG_CLK, ASSP_CLK and FB_CLK). The 16-bit CPU interface is implemented in the programmable fabric and the SDIO clock is turned off.

Table 17: Hi-Speed USB and PHY suspended with the internal and PHY clocks off, Vbus comparator disabled, VLP activated and all oscillators shut down (OTG_CLK, ASSP_CLK and FB_CLK)

Parameter	Typ. (mA)
Core (1.8 V)	0.05
I/O (3.3 V)	0.05
VDDA (3.3 V) - Analog USB PHY Supply	0.15
VDDP (1.8 V) - USB PHY PLL Supply	0.05
VCCIOASSP (3.3 V)	0.05

SD/SDIO/MMC/CE-ATA Power Consumption

Table 18 shows the typical power consumption for an SD memory card file transfer with a 25 MHz clock over a 16-bit CPU interface implemented in the programmable fabric. The USB and PHY are suspended with the internal and PHY clocks off. The Vbus comparator is disabled.

Table 18: SD Memory Card File Transfer with a 25 MHz Clock

Parameter	Typ. (mA)
Core (1.8 V)	20.30
I/O (3.3 V)	3.75
VDDA (3.3 V) - Analog USB PHY Supply	0.15
VDDP (1.8 V) - USB PHY PLL Supply	0.05
VCCIOASSP (3.3 V)	0.05

Programmable Fabric Power Consumption

QuickLogic's ultra low power programmable fabric is ideal for implementing connectivity solutions, custom logic and processor interface. The standby current of the ArcticLink Solution Platform fabric in VLP mode is as low as 4 μ A. The dynamic power consumption varies depending on the operating conditions and what functions are used in the fabric.

Power-Up Sequencing

Figure 13: Power-Up Sequencing

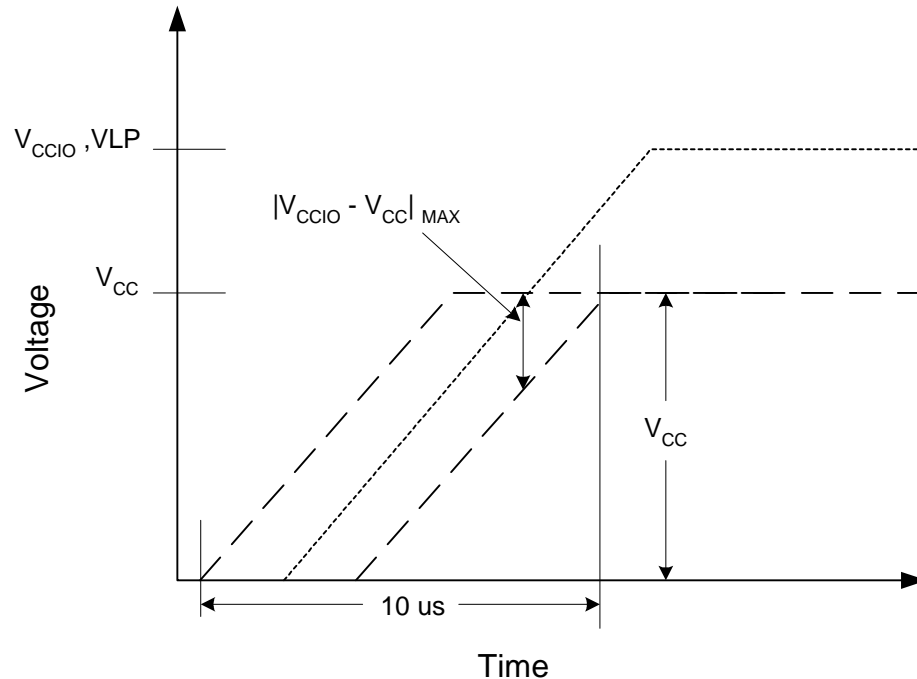


Figure 13 shows an example where all $V_{CCIO} = 3.3$ V.

When powering up the ArcticLink Solution Platform, V_{CC} , V_{CCIO} rails must take 10 μs or longer to reach the maximum value (refer to **Figure 13**). Ramping V_{CC} and V_{CCIO} faster than 10 μs can cause the device to behave improperly.

It is also important to ensure V_{CCIO} and V_{LP} are within 500 mV of V_{CC} when ramping up the power supplies. In the case where V_{CCIO} or V_{LP} are greater than V_{CC} by more than 500 mV an additional current draw can occur as V_{CC} passes its threshold voltage. In a case where V_{CC} is greater than V_{CCIO} by more than 500 mV the protection diodes between the power supplies become forward biased. If this occurs then there will be an additional current load on the power supply. Having the diodes on can cause a reliability problem, since it can wear out the diodes and subsequently damage the internal transistors.

USB Eye Diagrams

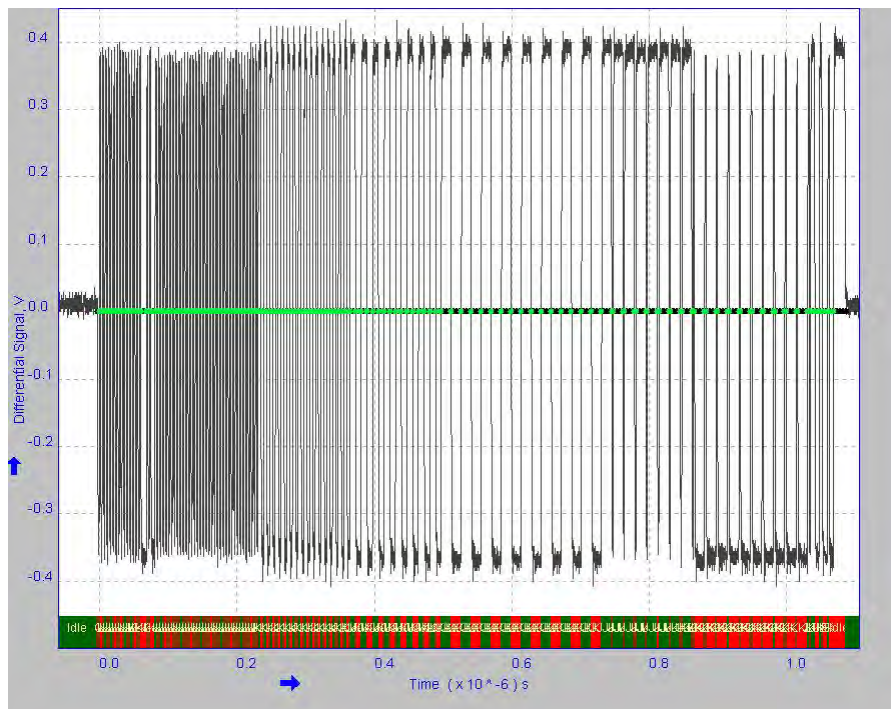
- Chip: ArcticLink 121 package
- Scope: Tektronix TDS7404B Digital Phosphor Oscilloscope
- Scope Testing Software: TDSUSB2 software version 3.0.4 Build 5
- Probe: Tektronix P7350 5Ghz 6.25x Differential Probe
- Test Fixture: Tektronix TDSUSBF USB2.0 Compliance Test Fixture
- PCB: Quicklogic ArcticLink Compliance Test Set -1
- USB-IF Compliance Test Procedures:
 - Host - http://www.usb.org/developers/docs/Host_HS_test_tektronix41503.pdf
 - Device - http://www.usb.org/developers/docs/Device_HS_test_tektronix41503.pdf

Signal Quality Test Results for ArcticLink 121 Host Mode

For details on test setup, methodology, and performance criteria, consult the signal quality test description at the <http://www.usb.org/developers/compliance/> USB-IF Compliance Program web page.

Near End High Speed Signal Data and Common Mode Voltage

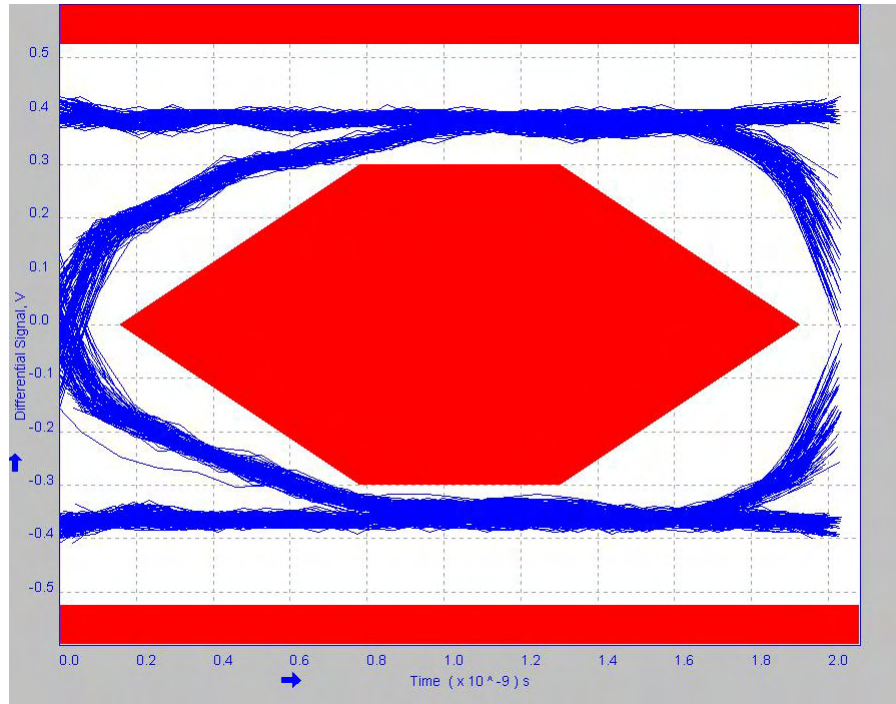
Figure 14: Host Mode Signal Quality Waveform



Required Tests

- Overall result: pass!
- Signal eye: Eye Diagram Test passes

Figure 15: Host Mode Signal Quality Eye Diagram



- EOP width: 16.65045 ns
EOP width passes
- EOP width (bits): 7.992826
EOP width (bits) passes
- Measured Signalling Rate: 480.0367 Mbps
Signal rate passes

Additional Information

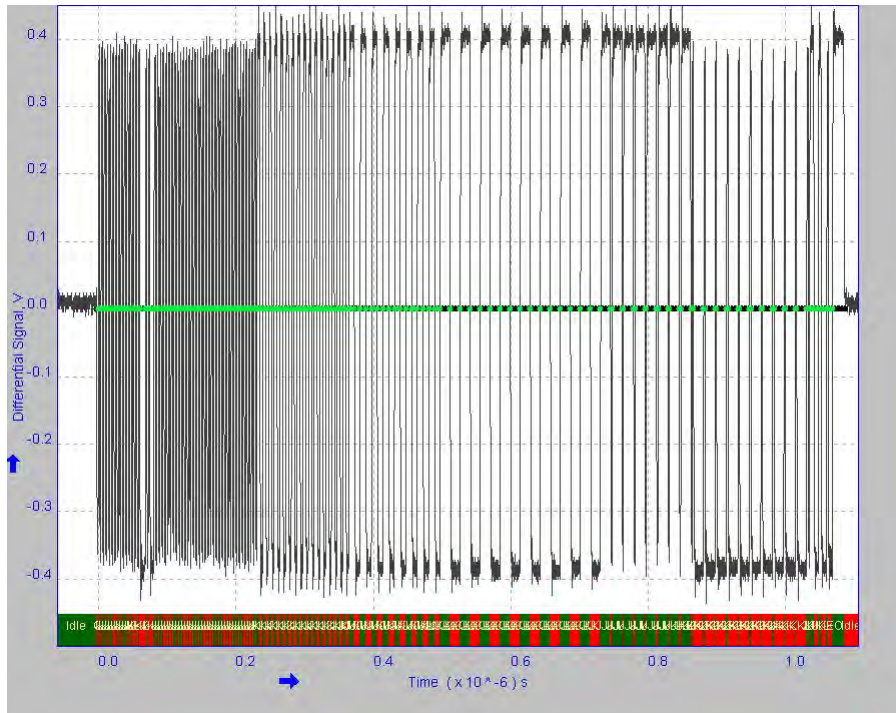
- Consecutive Jitter range: -1.068 us to 639.7 ps RMS Jitter 488.9 ns
- KJ Paired Jitter range: 4.166 ns to 29.16 ns RMS Jitter 12.51 ns
- JK Paired Jitter range: 4.166 ns to 29.16 ns RMS Jitter 12.46 ns

Signal Quality Test Results for ArcticLink 121 Device Mode

For details on test setup, methodology, and performance criteria, please consult the signal quality test description at the <http://www.usb.org/developers/compliance/> USB-IF Compliance Program web page.

Near End High Speed Signal Data and Common Mode Voltage

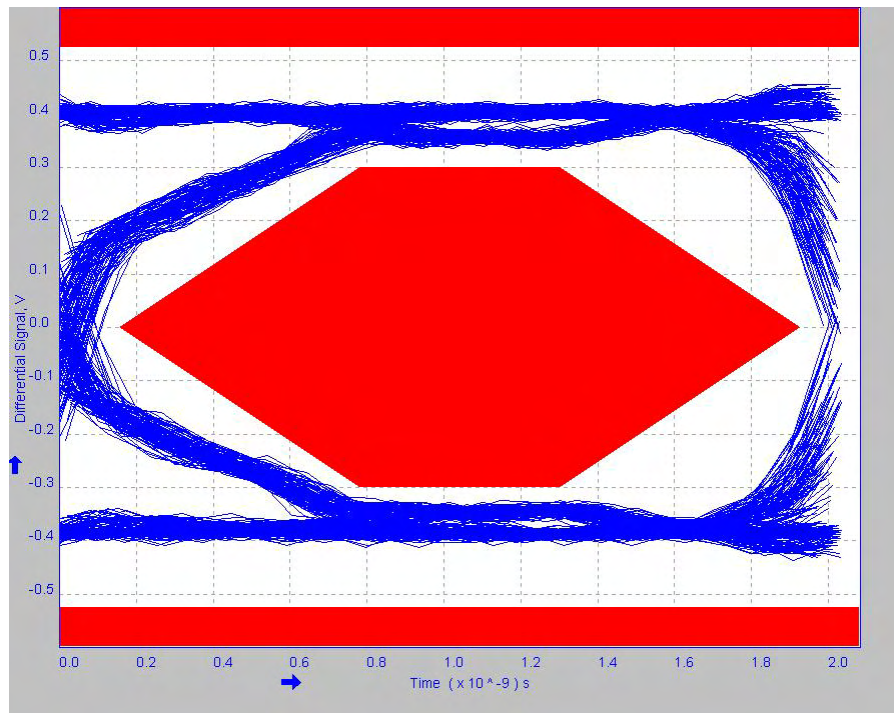
Figure 16: Device Mode Signal Quality Waveform



Required Tests

- Overall result: pass!
- Signal eye: Eye Diagram Test passes

Figure 17: Device Mode Signal Quality Eye Diagram



- EOP width: 16.55739 ns
EOP width passes
- EOP width (bits): 7.946519
EOP width (bits) passes
- Measured Signalling Rate: 479.9380 Mbps
Signal rate passes

Additional Information

- Consecutive Jitter range: -1.068 us to 764.1 ps RMS Jitter 488.9 ns
- KJ Paired Jitter range: 4.167 ns to 29.17 ns RMS Jitter 12.51 ns
- JK Paired Jitter range: 4.167 ns to 29.17 ns RMS Jitter 12.46 ns

Pin Descriptions

Table 19 shows pins on the ArcticLink Solution Platform that have a single function. See **Table 20** for recommended unused pin terminations.

Table 19: Single-Function Pin Descriptions

Pin	Direction	Function	Description
Dedicated Pin Descriptions			
GPIO(D:A)	I/O	CSSP dependent	CSSP dependent proven system block I/O.
CLK(B:A)	I	Global clock network pin low skew global clock	This pin provides access to a distributed network capable of driving the CLOCK, SET, RESET, all inputs to the Logic Cell, READ and WRITE CLOCKS, Read and Write Enables of the Embedded RAM Blocks, and I/O inputs. The voltage tolerance of this pin is specified by VCCIO(B:A).
DEDCLK(D)	I	Dedicated clock network pin low skew clock	This pin provides access to a distributed network capable of driving the CLOCK, SET, RESET, all inputs to the Logic Cell, READ and WRITE CLOCKS, Read and Write Enables of the Embedded RAM Blocks, and I/O inputs. The voltage tolerance of this pin is specified by VCCIO(D). This network can only be accessed from the DEDCLK(D) input pin.
CCMVCC	I	Power supply pin for CCM	CCM input voltage level. Configurable as 1.8 V only. The CCM is available in the ArcticLink 110-ball WLCSP and 196-ball TFBGA devices only.
CCMGND	I	Ground pin for CCM	Connect to ground. The CCM is available in the ArcticLink 110-ball WLCSP and 196-ball TFBGA devices only.
VLP	I	Very low power mode	Active low. Therefore, when VLP pin is low, the device will go into low power mode. Tie VLP to 3.3 V to disable low power mode.
VCC	I	Power supply pin	Connect to 1.8 V supply.
VCCIO(D:A)	I	Input voltage tolerance pin	This pin provides the flexibility to interface the device with either a 3.3 V, 2.5 V, or 1.8 V device. The letter inside the parenthesis means that the VCCIO is located in the bank with that letter. Every I/O pin in the same bank will be tolerant of the same VCCIO input signals and will drive VCCIO level output signals. This pin must be connected to either 3.3 V, 2.5 V, or 1.8 V.
GND	I	Ground pin	Connect to ground.
DQ ^a / GPIO(D)	I/O	Configurable pin can be declared as either a DDRIO DQ or as a general purpose I/O	The D inside the parenthesis means that the I/O is located in Bank D. If an I/O is not used, the development software provides the option of tying that pin to GND, VCCIO, or Hi-Z.
DQS ^a // GPIO(D)	I/O	Configurable pin can be declared as either a DDRIO DQS or as a general purpose I/O	The D inside the parenthesis means that the I/O is located in Bank D. If an I/O is not used, the development software provides the option of tying that pin to GND, VCCIO, or Hi-Z.
DQCK_N ^a / GPIO(D)	I/O	Configurable pin can be declared as either a DDRIO DQ, DDR negative clock, or as a general purpose I/O.	The D inside the parenthesis means that the I/O is located in Bank D. If an I/O is not used, the development software provides the option of tying that pin to GND, VCCIO, or Hi-Z.

Table 19: Single-Function Pin Descriptions (Continued)

Pin	Direction	Function	Description
DQCK_P ^a / GPIO(D)	I/O	Configurable pin can be declared as either a DDRIO DQ, DDR positive clock, or as a general purpose I/O.	The D inside the parenthesis means that the I/O is located in Bank D. If an I/O is not used, the development software provides the option of tying that pin to GND, VCCIO, or Hi-Z.
VREF(D)	I	Differential reference voltage	VREF(D) is the reference voltage pin for the SSTL1.8 and SSTL2 standards. The D inside the parenthesis means that INREF is located in Bank D. Tie this pin to GND if voltage referenced standards are not used.
VCCIO_ASSP	I	Input voltage tolerance pin	Voltage rail for SYS_RESET_n, OTG_CLK, and OTG_DRV_VBUS (connect to 3.3 V or 1.8 V depending on what the external charge pump can accept for the OTG_DRV_VBUS signal level).
JTAG Pin Descriptions			
TDI/RSI	I	Test data in for JTAG/RAM init. serial data in	Hold HIGH during normal operation. Connect to VCCIO(B) if unused.
TRSTB	I	Reset for JTAG	Active low. Hold LOW during normal operation. Connect to GND if unused. During JTAG, a high voltage is based on VCCIO(B).
TMS	I	Test mode select for JTAG	Hold HIGH during normal operation. Connect to VCCIO(B) if not used for JTAG.
TCK	I	Test clock for JTAG	Hold HIGH or LOW during normal operation. Connect to VCCIO(B) or GND if not used for JTAG.
TDO	O	Test data out for JTAG	Must be left unconnected if not used for JTAG. The output voltage drive is specified by VCCIO(B).
USB OTG Pins			
VBUS_OTG	I	Vbus	Pin used by the Hi-Speed USB 2.0 OTG Controller to monitor the Vbus.
OTG_DP	I/O	D+	Positive channel of serial USB cable.
OTG_DM	I/O	D-	Negative channel of serial USB cable.
OTG_ID	I	ID	USB ID pin of mini-AB connector.
VCCA_OTG	I	IO power	Analog 3.3 V supply for OTG PHY.
GND _A _OTG	I	IO ground	Analog ground for OTG PHY.
VCCP_OTG	I	PLL power	1.8 V supply pin for the OTG PHY PLL.
GND _P _OTG	I	PLL ground	Ground pin for the OTG PHY PLL.
OTG_RREF	Analog	Reference resistor	OTG external reference resistor. Tie to GND via a 5.76 K \pm 1% resistor.
OTG_DRV_VBUS	O	Vbus drive enable	This pin is used by the Hi-Speed USB 2.0 OTG Controller to enable the external 5 V power supply (charge pump) to drive the VBUS USB line.
System Pins			
SYS_RESET_n	I	System reset	Used as hardware reset for all fixed logic blocks.
OTG_CLK	I	OTG clock	12 MHz reference clock used for OTG PHY. Must be \pm 500 ppm.

a. The number following the DDRIO signal names in the pinout tables indicates the DDRIO set the pin corresponds to.

Recommended Unused Pin Terminations for the ArcticLink Solution Platform

All unused, general purpose I/O pins can be tied to VCCIO, GND, or Hi-Z (high impedance) internally. By default, QuickLogic QuickWorks software ties unused I/Os to GND.

Terminate the rest of the pins at the board level as recommended in **Table 20**.

Table 20: Recommended Unused Pin Terminations

Signal Name	Recommended Termination
Dedicated Pins	
CLK(B)	Connect to GND or VCCIO(B) if unused.
CLK(A)	Connect to GND or VCCIO(A) if unused.
CCMVCC	Connect to 1.8 V. If a CCM is used, do not attempt disable the CCM by tying the CCMVCC to GND.
DEDCLK(D)	Connect to GND or VCCIO(D) if unused.
VLP	Tie VLP to 3.3 V to disable low power mode.
VREF(D)	If the D I/O bank does not require the use of the VREF signal, connect the pin to GND.
JTAG Pins	
TDI	Connect to VCCIO(B) if not used for JTAG.
TRSTB	Connect to GND if not used for JTAG.
TMS	Connect to VCCIO(B) if not used for JTAG
TCK	Connect to VCCIO(B) or GND if not used for JTAG.
TDO	Must be left unconnected if not used for JTAG.
USB OTG Pins	
VBUS_OTG	If the designer does not intend to use the USB core, tie to GND.
OTG_DP	If the designer does not intend to use the USB core, leave unconnected.
OTG_DM	If the designer does not intend to use the USB core, leave unconnected.
OTG_ID	If the designer does not intend to use the USB core, leave unconnected.
VCCA_OTG	If the designer does not intend to use the USB core, tie this supply input to GND and configure the PHY for suspend mode by properly programming the global registers.
VCCP_OTG	If the designer does not intend to use the USB core, tie this supply input to GND and configure the PHY for suspend mode by properly programming the global registers.
OTG_RREF	If the designer does not intend to use the USB core, leave unconnected.
OTG_DRV_VBUS	If the designer does not intend to use the USB core, leave unconnected.

Multi-Function Pins

Table 21 shows I/O pins on the ArcticLink Solution Platform that have more than one function. These pins are normally GPIO pins unless the conditions in **Table 21** are met.

Table 21: Multi-Function Pin Descriptions

Pin Name	Direction	Description	Condition
SD/SDIO/MMC/CE-ATA => 10 pins			
ASSP_SD0_DATA[0]	I/O	SD/SDIO/MMC/CE-ATA data bit 0	AF_SD0_EN = 1
ASSP_SD0_DATA[1]	I/O	SD/SDIO/MMC/CE-ATA data bit 1	
ASSP_SD0_DATA[2]	I/O	SD/SDIO/MMC/CE-ATA data bit 2	
ASSP_SD0_DATA[3]	I/O	SD/SDIO/MMC/CE-ATA data bit 3	
ASSP_SD0_CLK	O	SD/SDIO/MMC/CE-ATA clock out	
ASSP_SD0_CMD	I/O	SD/SDIO/MMC/CE-ATA command bit	AF_SD0_EN = 1 and AF_SD0_8BIT_EN = 1
ASSP_SD0_DATA[4]	I/O	SD/SDIO/MMC/CE-ATA data bit 4	
ASSP_SD0_DATA[5]	I/O	SD/SDIO/MMC/CE-ATA data bit 5	
ASSP_SD0_DATA[6]	I/O	SD/SDIO/MMC/CE-ATA data bit 6	
ASSP_SD0_DATA[7]	I/O	SD/SDIO/MMC/CE-ATA data bit 7	
ULPI => 12 pins			
ASSP_ULPI_DATA[7]	I/O	ULPI data bit [7]	AF_ULPI_EXT_EN =1
ASSP_ULPI_DATA[6]	I/O	ULPI data bit [6]	
ASSP_ULPI_DATA[5]	I/O	ULPI data bit [5]	
ASSP_ULPI_DATA[4]	I/O	ULPI data bit [4]	
ASSP_ULPI_DATA[3]	I/O	ULPI data bit [3]	
ASSP_ULPI_CLK	I	ULPI clock input	
ASSP_ULPI_DIR	I	ULPI data direction	
ASSP_ULPI_DATA[2]	I/O	ULPI data bit [2]	
ASSP_ULPI_DATA[1]	I/O	ULPI data bit [1]	
ASSP_ULPI_DATA[0]	I/O	ULPI data bit [0]	
ASSP_ULPI_NXT	I	ULPI NXT signal	
ASSP_ULPI_STP	O	ULPI STP signal	

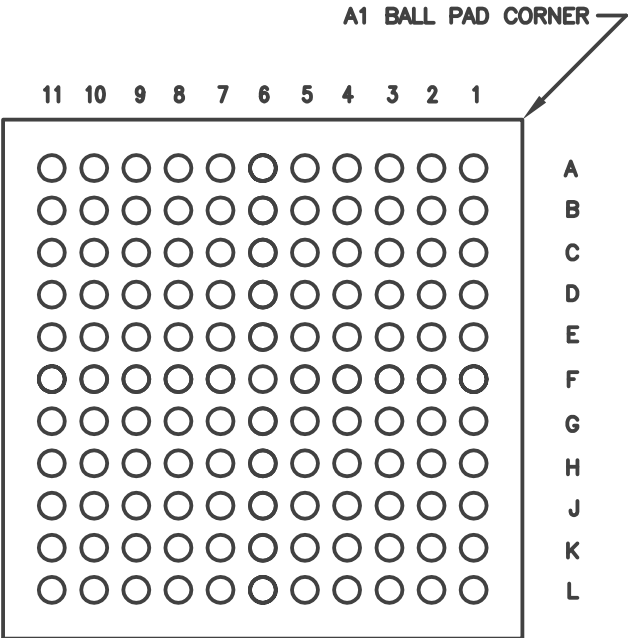
Packaging Pinout Diagrams

QL1A100 - 121 TFBGA Pinout Diagram

Top



Bottom

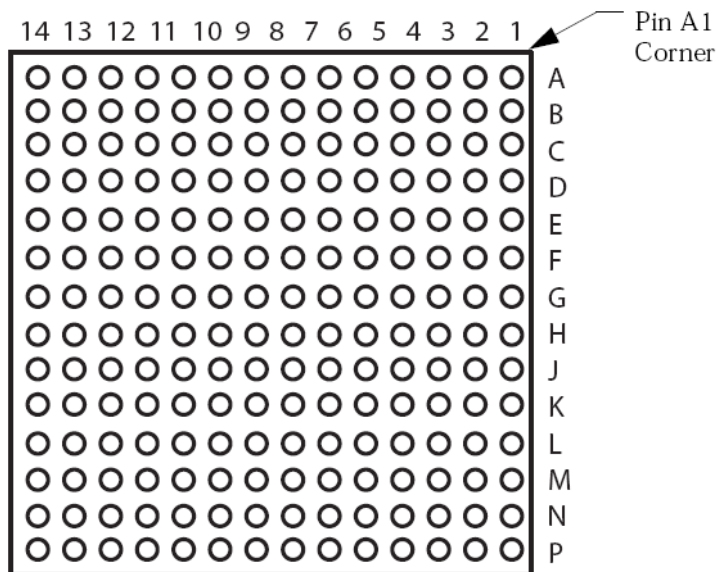


QL1A100 - 196 TFBGA (12 mm x 12 mm) Pinout Diagram

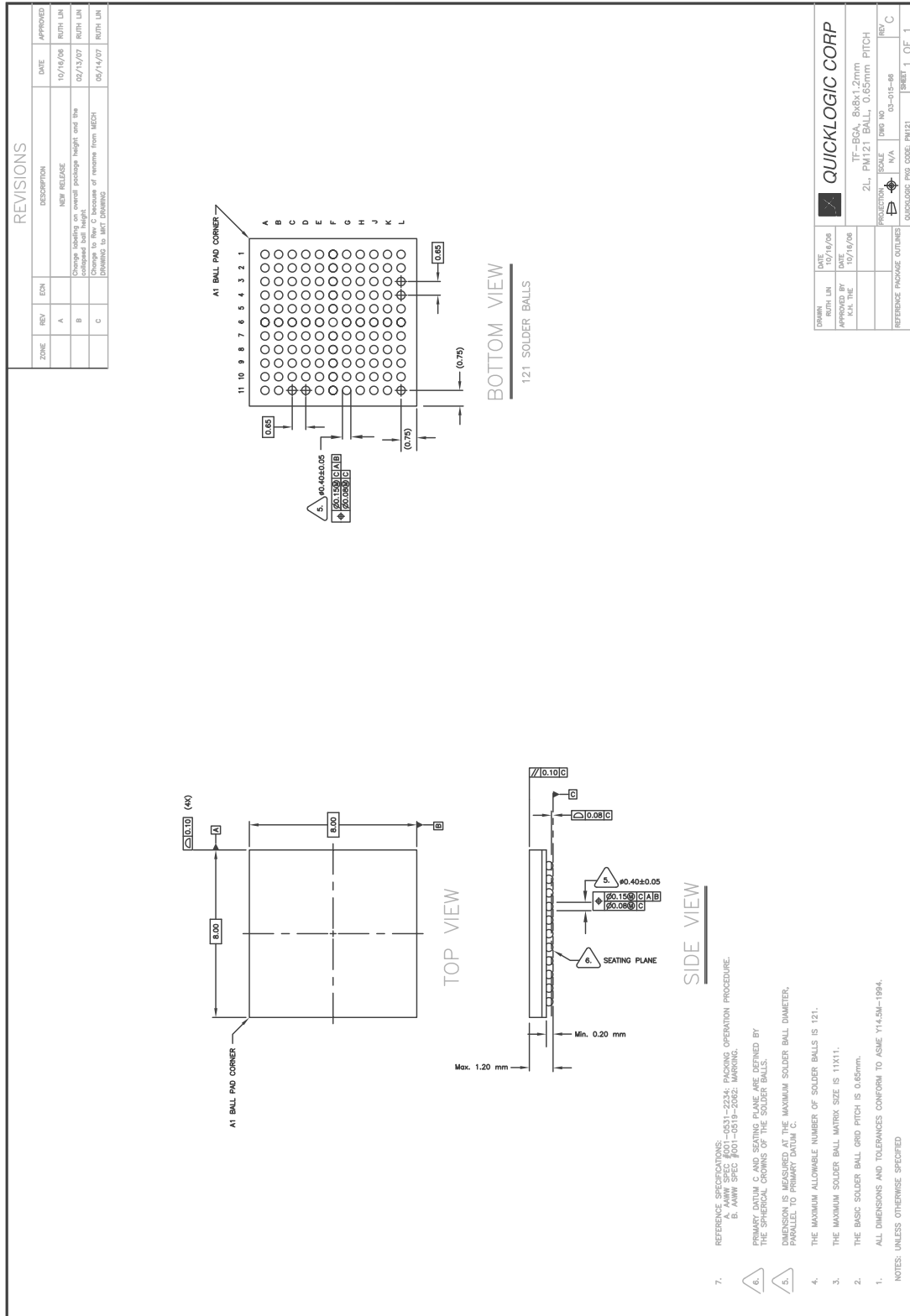
Top



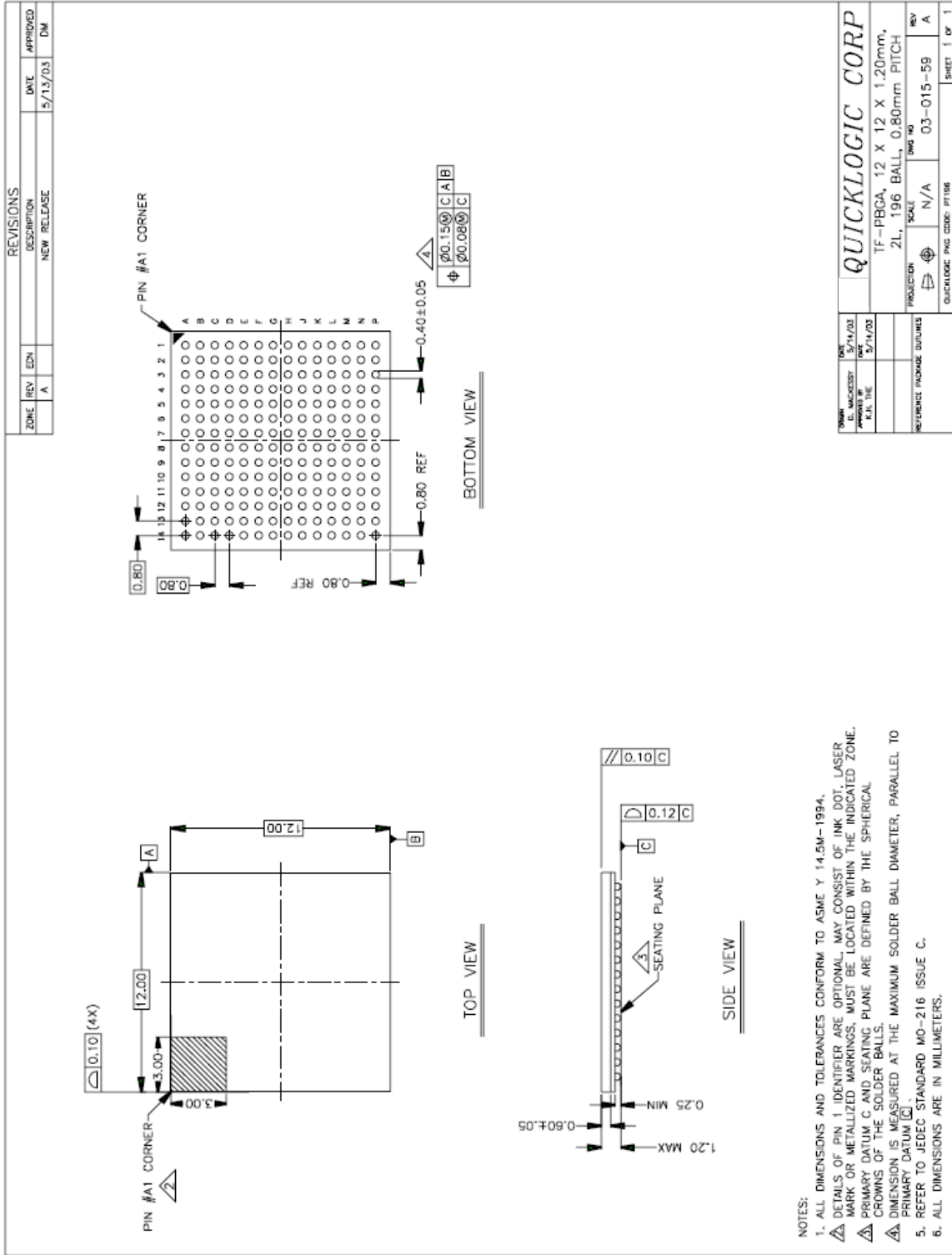
Bottom



121 TFBGA (8 mm x 8 mm) Package Drawing



196 TFBGA (12 mm x 12 mm) Package Drawing



- NOTES:
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y 14.5M-1994.
 2. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, MAY CONSIST OF INK DOT, LASER MARK OR METALLIZED MARKINGS, MUST BE LOCATED WITHIN THE INDICATED ZONE.
 3. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
 4. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
 5. REFER TO JEDEC STANDARD MO-216 ISSUE C.
 6. ALL DIMENSIONS ARE IN MILLIMETERS.

Packaging Information

The ArcticLink Solution Platform packaging information is shown in **Table 22**.

Table 22: Packaging Options

Device Information	QL1A100		
	Ball	Pb	Pb-Free
Package Definitions ^a	110 WLCSP (10 x 11 array) Pitch - 0.40 mm	-	X
	121 TFBGA (8 mm x 8 mm) Pitch - 0.65 mm	-	X
	196 TFBGA (12 mm x 12 mm) Pitch - 0.80 mm	-	X

a. TFBGA = Thin Profile Fine Pitch Ball Grid Array
WLCSP = Wafer Level Chip Scale Package

Ordering Information

ArcticLink Solution Platform Customer Specific Standard Products (CSSPs) have assigned part numbers, contact your local sales representative for your specific CSSP number.

Contact Information

Phone: (408) 990-4000 (US)
(647) 367-1014 (Canada)
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+(886) 2-2345-5600 (Asia)

E-mail: info@quicklogic.com

Sales: America-sales@quicklogic.com

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Asia-sales@quicklogic.com

Japan-sales@quicklogic.com

Support: www.quicklogic.com/support

Internet: www.quicklogic.com

Revision History

Revision	Date	Originator and Comments
A	June 2006	Judd Heape and Kathleen Murchek
B	December 2006	Stanley Hung, Judd Heape and Kathleen Murchek
C	March 2007	Judd Heape and Kathleen Murchek
D	July 2007	Judd Heape and Kathleen Murchek
E	September 2007	Howard Li and Kathleen Murchek Kept CSSP-related information only and removed DIY information for the ArcticLink Solution Platform Data Sheet.
F	November 2007	Judd Heape and Kathleen Murchek Updated Table 7. Recommended Operating Range.
G	January 2008	Howard Li and Kathleen Murchek Added conditional text and made minor updates.
H	July 2008	Kathleen Murchek Updated Disclaimer, Contact and Ordering information. Updated Table 3. Proven System Blocks Provided by QuickLogic. Added Theta-JC column to Package Thermal Characteristics table.
I	July 2008	Jason Lew and Kathleen Murchek Added 110 WLCSP pinout package information.
J	April 2009	Kathleen Murchek Updated trademark information.
J	September 2008	Jason Lew and Kathleen Murchek Updated QL1A100 - 110 WLCSP (10 x 11 array) Pinout Table
K	October 2008	Jason Lew and Kathleen Murchek Added "The CCM is available in the ArcticLink 110-ball WLCSP and 196-ball TFBGA devices only." to the pin descriptions for CCMVCC and CCMGND.
L	April 2009	Kathleen Murchek Updated trademark information.
M	May 2009	Kathleen Bylsma Removed pin tables, updated GPIO description and updated contact info.

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