

NAND Flash Controller Data Sheet



••••• Proven System Block (PSB) for QuickLogic Customer Specific Standard Products (CSSPs)

Features

The QuickLogic NAND Flash Controller has the following features:

- Support for NAND Flash devices with 8-bit or 16-bit I/O bus
- Internal 1-Kbyte Read and Write FIFOs for burst data transfers
- Low power consumption for use in battery-powered devices
- Support for multiple NAND Flash devices
- Support for large and small block NAND Flash devices
- Controlled Flash can be programmed with different access time, data width size and number of banks
- Supports flow-through DMA data transfers
- ECC with 1-bit correction and 2-bit detection

Overview

With ever-increasing density and decreasing price, NAND has been displacing hard disk drives as the primary storage devices in many handheld portable devices. Unlike hard disk drives, NAND flash does not have mechanical pieces and therefore is much more reliable and power efficient. The recent multi-level cell (MLC) NAND flash pushes the flash density to multiple Gigabit range with a very competitive price point.

Unlike its predecessor, the NOR flash, NAND flash faces three main challenges

- There is no industry standard for NAND Flash. Different vendors all have slightly different specifications, which makes it particularly difficult to build a universal NAND controller.
- NAND flash requires stronger error detection and correction algorithm that demands more hardware processing power.
- NAND does not support Execute-in-place (XIP) and special circuitry has to be put in place to handle booting from NAND flash.

QuickLogic's NAND Flash Controller adds flexible and high performance NAND flash interface to application processors, allowing designers to take advantage of the explosive growth in NAND Flash technology. It is built on QuickLogic's patented ultra-low power ViaLink programmable platforms specifically designed for power-sensitive portable devices.

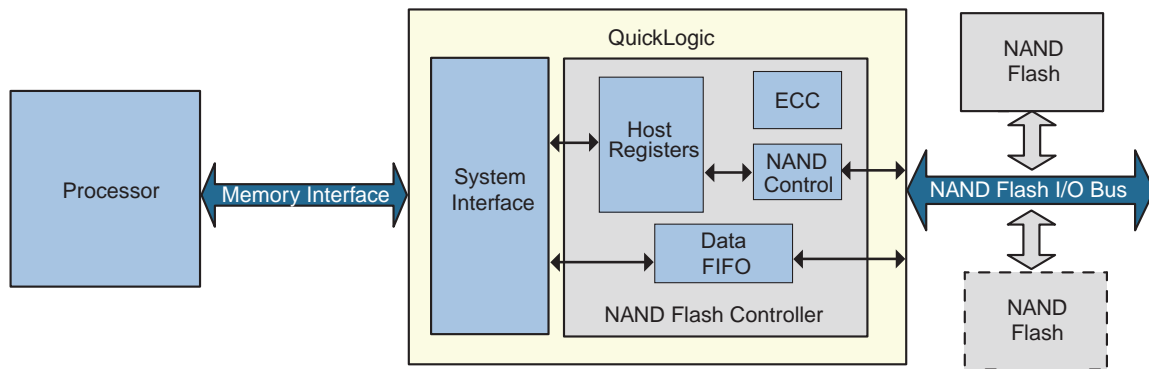
NAND Flash Controller Architecture

At full memory bandwidth the NAND Flash Controller supports burst access to the NAND Flash memory. Timing parameters of the controller are fully programmable so different memory speeds are supported regardless of the operating frequency of the controller. The NAND Flash Controller supports optional error correction code (ECC) that performs single-bit error correction and double-bit error detection. The core can automatically perform error detection and correction with error logging through internal control registers. The core can be configured to generate interrupt on ECC error. ECC error can also be injected into the NAND Flash device if desired for diagnostic purposes.

The Quicklogic NAND Flash Controller can be used to access large or small block NAND Flash devices. Additionally, the NAND Flash Controller FIFOs can be used when transferring data from large block NAND devices only (i.e., not small block NAND devices). Memory size, bus width, access timing, and number of banks are all programmable. Several user interface options are available. QuickLogic also provides different processor memory interfaces on customer request. This is available through the standard internal interface that is designed for on-chip system integration. It has separate address and data buses and command signals that supports burst transfer and wait state insertion. The NAND Flash Controller acts as a target or slave device on these buses. With these standard bus interfaces, the NAND Flash Controller can be integrated seamlessly with systems built on these standards.

Figure 1 shows the system level architecture of the NAND Flash Controller. Communication between the host processor and the NAND flash device is performed through the NAND Flash Controller. A 512-byte FIFO is embedded in the NAND Flash Controller and allows a page of data to be read or written a page at a time.

Figure 1: NAND Flash Controller System Level Architecture



Interface List and Description

As shown in **Table 1**, the NAND Flash Controller has two interfaces (Host and NAND Flash) and is implemented on the PolarPro QL1P100-256.

Table 1: NAND Flash Controller Interface

Signal Name	Direction	Description
SYS_CLK	I	System clock.
Host Interface Signals		
HOST_ADDR[15:0]	I	Address bus.
HOST_DATA[31:0]	I/O	Data bus. NOTE: If the host only has a 16-bit data bus, the upper 16 bits do not need to be connected.
HOST_RST	I	Reset signal.
HOST_CS#	I	Chip select strobe.
HOST_WE#	I	Write enable strobe.
HOST_OE#	I	Output enable strobe.
HOST_RDY	O	Ready signal.
HOST_INT	O	Interrupt signal.
HOST_DREQ	O	DMA request signal.
NAND Flash Interface Signals		
NAND_IO[15:0]	I/O	I/O bus. Used for commands, addresses and data for the NAND Flash.
NAND_ALE	O	Address latch enable. Indicates when an address byte is on the NAND_IO[15:0] lines.
NAND_CLE	O	Command latch enable. Indicates when a command byte is on the NAND_IO[15:0] lines.
NAND_CE#	O	Chip enable strobe.
NAND_RE#	O	Read enable strobe.
NAND_WE#	O	Write enable strobe.
NAND_WP#	O	Write protect signal.
NAND_RB	I	Ready/Busy signal.

Register Sets

Address Map

Table 2 shows the NAND Flash Controller address map.

Table 2: NAND Flash Controller Address Map

Name	Address	Size	Description
Registers	0x1000–0x101F	16-bit	Configuration and Status Registers
FIFO Read Port	0x2000	32-bit	Read data from RD FIFO
Read Data Port	0x3000	8-bit	Read data from NAND FIFO
FIFO Write Port	0x4000	32-bit	Write data to WR FIFO
Write Data Port	0x5000	8-bit	Write data to NAND Flash
Address Port	0x6000	8-bit	NAND Flash Address
Command Port	0x7000	8-bit	NAND Flash Command

Register Description

The NAND Flash Controller Configuration and Status Registers are mapped into the processor memory. The addresses are offsets from the base address of the chip select to which the NAND Flash controller is attached.

Configuration and Status Registers (0x1000 to 0x101F)

The Configuration and Status Registers are used to configure the operation of the NAND Flash Controller.

Name	Address	Size	Type	Description
CMD	0x1000	16-bit	R/W	FLASH Command
STAT	0x1004	16-bit	R/W	FLASH Status
CFG0	0x1008	16-bit	R/W	Controller Configuration 0
SET_ERR	0x100C	16-bit	R/W	Set Error
ECC_STAT0	0x1010	16-bit	RO	ECC Status 0
ECC_STAT1	0x1014	16-bit	RO	ECC Status 1
ECC_STAT2	0x1018	16-bit	RO	ECC Status 2
ECC_STAT3	0x101C	16-bit	RO	ECC Status 3

CMD — FLASH Command Register

Address Offset: 0x1000

Size: 16 bits

Type: R/W

Reset Value: 0x0000

The NAND Flash memory device’s read or write operations are controlled by this register.

Name	Bit(s)	Type	Reset Value	Function
Reserved	15:12	RO	0	N/A
WRITE_PAGE	1	R/W	0	Write Page. The Write Page bit is used to start the page writing function. This Write Page the bit automatically clears when the page write is completed. 0 – Idle 1 – Start page write using Write FIFO
READ_PAGE	0	R/W	0	Read Page. The Read Page bit is used to start the page reading function. This Read Page bit automatically clears when the page read is completed. 0 – Idle 1 – Start page read using Read FIFO

STAT — Flash Status Register

Address Offset: 0x1004

Size: 16 bits

Type: R/W

Reset Value: 0x0000

The status of the NAND Flash device can be read from this register.

Name	Bit(s)	Type	Reset Value	Function
INTERRUPT	15	RO	0	<p>Interrupt Status. The Interrupt bit indicates the state of the interrupt signal. This interrupt (when enabled) is asserted for the following events.</p> <ul style="list-style-type: none"> • After each 1 KByte block of data has been transferred from the NAND Flash device into the Read FIFO on a read transfer. • After each 1 KByte block of data has been transferred from the Write FIFO to the NAND Flash device on a write transfer. <p>This interrupt is cleared by writing a '0' to this bit.</p> <p>0 – Interrupt is NOT asserted 1 – Interrupt is asserted</p>
Write FIFO Empty	14	RO	–	<p>Request Write FIFO Status. The Write FIFO Empty status bit indicates when the Write FIFO is empty. The Write FIFO is 256-dwords (1-KByte) deep. To maximize efficiency on the CPU bus, DMA transfers should be 256-dwords in size and should start when the 'Write FIFO Empty' bit is set.</p> <p>0 – Write FIFO Status Request is NOT asserted 1 – Write FIFO Status Request is asserted</p>
Read FIFO Full	13	RO	–	<p>Request Read FIFO Status. The 'Read FIFO Full' status bit indicates when the Read FIFO is full. The Read FIFO is 1-KByte deep. To maximize efficiency on the CPU bus, transfers should be 1-KByte in size and should start when the 'Read FIFO Full' bit is set.</p> <p>0 – Read FIFO Status Request is NOT asserted 1 – Read FIFO Status Request is asserted</p>
Reserved	12:8	RO	0	N/A
Write Protect	7	RO	–	<p>NAND Flash Device Write Protect Status</p> <p>0 – Write protected 1 – NOT write protected</p>
Reserved	6	RO	0	N/A
Ready/Busy	5	RO	–	<p>NAND Flash Device Ready/Busy Status</p> <p>0 – Busy 1 – Ready</p>
Reserved	4:0	RO	0	N/A

CFG0 – Controller Configuration Register

Address Offset: 0x1008

Size: 16 bits

Type: R/W

Reset Value: 0x0000

This register controls the configuration of the NAND Flash Controller.

Name	Bit(s)	Type	Reset Value	Function
WP_EN	15	R/W	0	Write Protect 0 – Write protect is disabled 1 – Write protect is enabled
Reserved	14:9	RO	0	N/A
ENABLE_ECC	8	R/W	0	ECC Enable 0 – ECC is disabled 1 – ECC is enabled
OSC_EN	7	R/W	1	Oscillator Enable 0 – Oscillator is disabled 1 – Oscillator is enabled
Reserved	6:3	RO	0	N/A
DREQ_EN	2	R/W	0	DMA Request Signal Enable 0 – DREQ signal is disabled 1 – DREQ signal is enabled
INT_EN	1	R/W	0	Interrupt Enable 0 – Interrupt is disabled 1 – Interrupt is enabled
Reserved	0	RO	0	N/A

SET_ERR – Set Error Register

Address Offset: 0x100C

Size: 16 bits

Type: R/W

Reset Value: 0x0000

This register is used to set an error during read back of the NAND Flash memory device’s data to test ECC functionality.

Name	Bit(s)	Type	Reset Value	Function
Flash address offset	15:5	RO	0	Page read offset address. Page read offset address to apply NAND Flash data invert mask.
Flash data invert mask	4:0	R/W	0	NAND Flash data invert mask 0 – Do not invert data 1 – Invert data bit

ECC_STAT0 – ECC Status 0 Register

Address Offset: 0x1010

Size: 16 bits

Type: RO

Reset Value: 0x0000

This register provides the ECC status of the first 512-byte section of the NAND Flash page.

Name	Bit(s)	Type	Reset Value	Function
Reserved	15:14		0	
Error Status	13:12	RO	0	Error Status 00 – No error 01 – Fixable 1-bit error 10 – Unfixable 2-bit error 11 – Not Used
Error Location	11:0	RO	0	Error Byte Location

ECC_STAT1 – ECC Status 1 Register

Address Offset: 0x1014

Size: 16 bits

Type: RO

Reset Value: 0x0000

This register provides the ECC status of the second 512-byte section of the NAND Flash page.

Name	Bit(s)	Type	Reset Value	Function
Reserved	15:14		0	
Error Status	13:12	RO	0	Error Status 00 – No error 01 – Fixable 1-bit error 10 – Unfixable 2-bit error 11 – Not Used
Error Location	11:0	RO	0	Error Byte Location

ECC_STAT2 – ECC Status 2 Register

Address Offset: 0x1018

Size: 16 bits

Type: RO

Reset Value: 0x0000

This register provides the ECC status of the third 512-byte section of the NAND Flash page.

Name	Bit(s)	Type	Reset Value	Function
Reserved	15:14		0	
Error Status	13:12	RO	0	Error Status 00 – No error 01 – Fixable 1-bit error 10 – Unfixable 2-bit error 11 – Not Used
Error Location	11:0	RO	0	Error Byte Location

ECC_STAT3 – ECC Status 3 Register

Address Offset: 0x101C

Size: 16 bits

Type: RO

Reset Value: 0x0000

This register provides the ECC status of the fourth 512-byte section of the NAND Flash page.

Name	Bit(s)	Type	Reset Value	Function
Reserved	15:14		0	
Error Status	13:12	RO	0	Error Status 00 – No error 01 – Fixable 1-bit error 10 – Unfixable 2-bit error 11 – Not Used
Error Location	11:0	RO	0	Error Byte Location

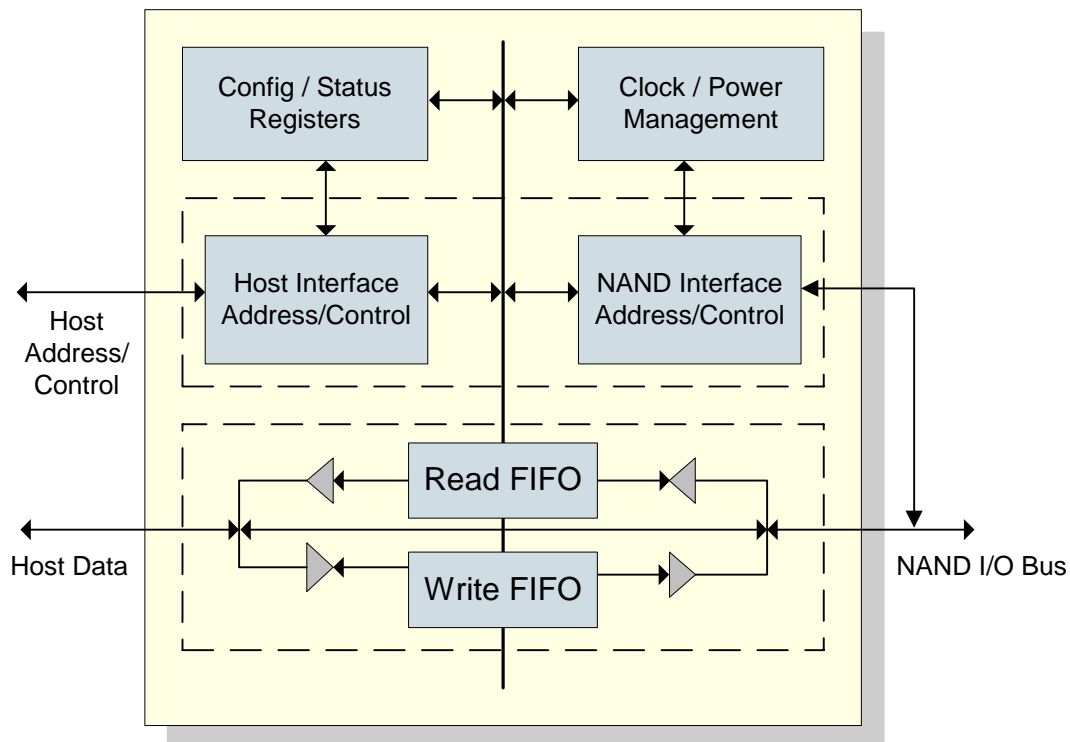
Functional and Module Description

The NAND Flash Controller provides connectivity between the processor and NAND Flash devices and consists of the following components:

- Configuration/status registers
- Clock and power management
- Host interface
- NAND Flash interface
- Read FIFO
- Write FIFO

Figure 2 shows the architecture and internal modules of the NAND Flash Controller.

Figure 2: NAND Flash Controller Architecture



Host Interface

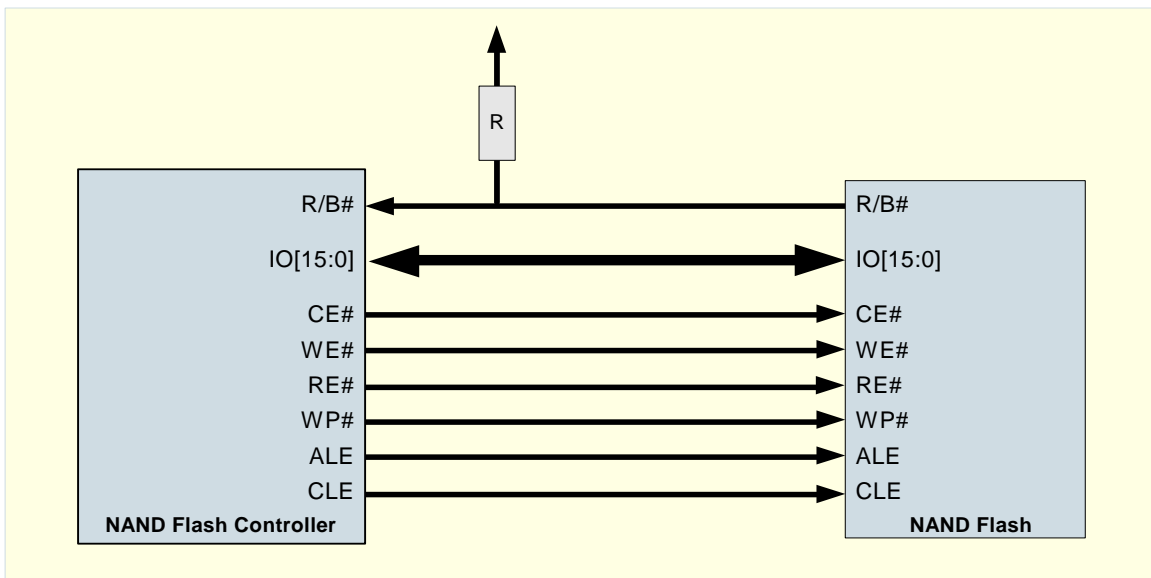
The QuickLogic NAND Flash Controller has a Host Interface that is similar to an SRAM interface but with an additional data ready output signal (RDY) that can be used to insert a variable number wait states to a connected processor. The data bus width of the Host Interface can be programmed to be either 16-bit or 32-bit.

During read or write cycles on the host interface, the connected processor samples the RDY signal on the rising edge of the static memory interface clock (MEMCLK). The RDY signal is level-sensitive and goes through a two-stage synchronizer at the input. When the synchronized internal RDY signal is high, the Host Interface is ready to complete the data transfer.

NAND Flash Interface

NAND Flash memory devices use a multiplexed 8-bit or 16-bit I/O bus to transfer commands, addresses and data. The five command signals (CLE, ALE, CE#, RE# and WE#) implement the NAND Flash command bus interface protocol. Two additional signals control hardware write protection (WP#) and monitor the NAND Flash device status (R/B#). **Figure 3** shows the NAND Flash Controller interface with the NAND Flash device.

Figure 3: NAND Flash Controller Interface with NAND Flash Device



Each NAND Flash memory device page consists of 2,112 bytes divided into a 2,048-byte data storage region and a separate 64-byte area used for error management functions.

The NAND Flash device’s internal memory array is accessed on a page basis. During a read access, a page of data is copied from the internal memory array into the internal data register. After the page is copied into the internal data register, the data is output one byte at a time on the I/O bus to the NAND Flash Controller.

The NAND Flash device’s internal memory array is programmed on a page basis. After the starting address is loaded into the internal address register, the data is written one byte at a time to the internal data register. When all of the page data has been written to the internal data register, the data is then programmed into the array.

NAND Flash Command Sequences

NAND Flash memory devices use these basic commands.

- Page Read
- FIFO Page Read
- Program Page
- FIFO Program Page

Page Read

Follow the steps listed below to read a page of data from the NAND Flash device using the Read Data Port (0x3000).

1. Write the first PAGE READ (00h) command to the Command Port (0x7000).
2. Write the required number (depending on the NAND Flash device) of address bytes to the Address Port (0x6000)
3. Write the second PAGE READ (30h) command to the Command Port (0x7000).
4. Wait until the READY/BUSY# Bit (bit5) in the STAT — FLASH Status Register (0x1004) is set
5. Read all 528-dwords (2,112 bytes) of the page data from the Read Data Port (0x3000).

FIFO Page Read

Follow the steps listed below to read a page of data from the NAND Flash Controller using the Read FIFO (0x2000):

1. Write the first PAGE READ (00h) command to the Command Port (0x7000).
2. Write the required number (depending on the NAND Flash device) of address bytes to the Address Port (0x6000).
3. Write the second PAGE READ (30h) command to the Command Port (0x7000).
4. Set the READ_PAGE Bit (bit 0) in the CMD — FLASH Command Register (0x1000).
5. Wait until the interrupt is asserted.
6. Clear the interrupt by writing '0' to the INTERRUPT Bit (bit 15) in the STAT — FLASH Status Register (0x1004).
7. Read 256 dwords (1,024 bytes) of the NAND Flash's page data from the FIFO Read Port (0x2000).
8. Wait until the interrupt is asserted.
9. Clear the interrupt by writing '0' to the INTERRUPT Bit (bit 15) in the STAT — FLASH Status Register (0x1004).
10. Read 272 dwords (1,024 data bytes plus 64 spare-area bytes) of the NAND Flash's page data from the FIFO Read Port (0x2000).

Program Page

Follow the steps listed below to program a page of data into the NAND Flash memory device using the Write Data Port (0x5000):

1. Write the first PROGRAM PAGE (80h) command to the Command Port (0x7000).
2. Write the required number (depending on the NAND Flash memory device) of address bytes to the Address Port (0x6000).
3. Write all 528 dwords (2,112 bytes) of the page data to the Write Data Port (0x5000).
4. Write the second PROGRAM PAGE (10h) command to the Command Port (0x7000).
5. Wait until the READY/BUSY# (bit5) in the STAT — FLASH Status Register (0x1004) is set.
6. Read bit 0 of the NAND Flash memory device's status register to determine if the program operation passed or failed.

FIFO Program Page

Follow the steps listed below to program a page of data into the NAND Flash Controller using the Write FIFO (0x4000):

1. Write the first PROGRAM PAGE (80h) command to the Command Port (0x7000).
2. Write the required number (depending on the NAND Flash memory device) of address bytes to the Address Port (0x6000).
3. Set the WRITE PAGE START Bit (bit 1) in the CMD — FLASH Command Register (0x1000).
4. Write 256 dwords (1,024 bytes) of the page data to the FIFO Write Port (0x4000).
5. Wait until the interrupt is asserted.
6. Clear the interrupt by writing '0' to the INTERRUPT Bit (bit 15) in the STAT — FLASH Status Register (0x1004).
7. Write 272 dwords (1,024 data bytes plus 64 spare-area bytes) of the page data to the FIFO Write Port (0x4000).
8. Wait until the interrupt is asserted.
9. Clear the interrupt by writing '0' to the INTERRUPT Bit (bit 15) in the STAT — FLASH Status Register (0x1004).
10. Write the second PROGRAM PAGE (10h) command to the Command Port (0x7000).
11. Wait until the READY/BUSY# (bit 5) in the STAT — FLASH Status Register (0x1004) is set.
12. Read bit 0 of the NAND Flash memory device's status register to determine if the program operation passed or failed.

Supported Operating Systems

The NAND Flash Controller PSB supports the following operating systems:

- Windows® CE
- Linux®

Contact Information

Phone: (408) 990-4000 (US)
(905) 940-4149 (Canada)
+(44) 1932-57-9011 (Europe)
+(852) 2567-5441 (Asia)

E-mail: info@quicklogic.com

Sales: America-sales@quicklogic.com

Europe-sales@quicklogic.com

Asia-sales@quicklogic.com

Japan-sales@quicklogic.com

Support: www.quicklogic.com/support

Internet: www.quicklogic.com

Revision History

Revision	Date	Originator and Comments
A	June 2008	First release.

Notice of Disclaimer

QuickLogic is providing this design, product or intellectual property "as is." By providing the design, product or intellectual property as one possible implementation of your desired system-level feature, application, or standard, QuickLogic makes no representation that this implementation is free from any claims of infringement and any implied warranties of merchantability or fitness for a particular purpose. You are responsible for obtaining any rights you may require for your system implementation. QuickLogic shall not be liable for any damages arising out of or in connection with the use of the design, product or intellectual property including liability for lost profit, business interruption, or any other damages whatsoever. QuickLogic products are not designed for use in life-support equipment or applications that would cause a life-threatening situation if any such products failed. Do not use QuickLogic products in these types of equipment or applications.

QuickLogic does not assume any liability for errors which may appear in this document. However, QuickLogic attempts to notify customers of such errors. QuickLogic retains the right to make changes to either the documentation, specification, or product without notice. Verify with QuickLogic that you have the latest specifications before finalizing a product design.

Copyright and Trademark Information

Copyright © 2008 QuickLogic Corporation. All Rights Reserved.

The information contained in this document and is protected by copyright. All rights are reserved by QuickLogic Corporation. QuickLogic Corporation reserves the right to modify this document without any obligation to notify any person or entity of such revision. Copying, duplicating, selling, or otherwise distributing any part of this product without the prior written consent of an authorized representative of QuickLogic is prohibited.

QuickLogic, PolarPro, the PolarPro design, and ViaLink are registered trademarks, and the QuickLogic logo is a trademark of QuickLogic. Other trademarks are the property of their respective companies.