

Smart Data Transfer (SDT) Between USB 2.0 OTG and IDE Interfaces Data Sheet



••••• Proven System Block (PSB) for QuickLogic Customer Specific Standard Products (CSSPs)

Features

Smart Data Transfer

This reconfigurable architecture has a Smart Data Transfer (SDT) engine which includes:

- On-chip intelligence that enables direct port-to-port data transfers without involving the Host CPU bus such as Hi-Speed USB 2.0 OTG Controller to/from PATA IDE Controller with UDMA support
- Supports up to 32 MBytes/sec. transfer rate between the HDD and the QuickLogic-supplied Hi-Speed 2.0 OTG interface port
- Significantly improved speed for large file transfer, enhancing the user experience and increasing battery life

Hi-Speed USB 2.0 OTG Controller

The Hi-Speed USB 2.0 OTG Controller main features include:

- USB 2.0 OTG controller with integrated PHY that is compliant with the *USB Revision 2.0 Specification*
- Integrated HS USB 2.0 OTG port capable of high-speed (HS) 480 Mbits/sec., full-speed (FS) 12 Mbits/sec., and low-speed (LS) 1.5 Mbits/sec. transfers
- Supports OTG Host Negotiation Protocol (HNP) and Session Request Protocol (SRP)
- Configurable power management features that supports suspend and remote wake-up

For more information about QuickLogic's Hi-Speed USB 2.0 OTG Controller, see the *ArcticLink Solution Platform User Manual*.

IDE Host Controller

The IDE Host Controller main features include:

- Supports PIO Mode 0 to PIO Mode 4
- Supports Multiword DMA Mode 0 to Mode 2 with maximum Multiword DMA Mode 2 performance up to 16.7 Mbytes/sec. (excluding OS overhead)
- Supports Ultra-DMA (UDMA) Mode 0 to Mode 4 with maximum UDMA Mode 4 performance 66 Mbytes/sec.
- Supports connection to hard disk drives and/or CD-ROM/DVD-ROM (ATAPI) devices and is also compatible with Compact Flash/PCMCIA card in TRUE-IDE/ATA mode
- Internal IDE sector buffering for increased performance ("prefetch" sector transfers)

For more information about QuickLogic's IDE Host Controller, see the *IDE Host Controller Data Sheet*.

Overview

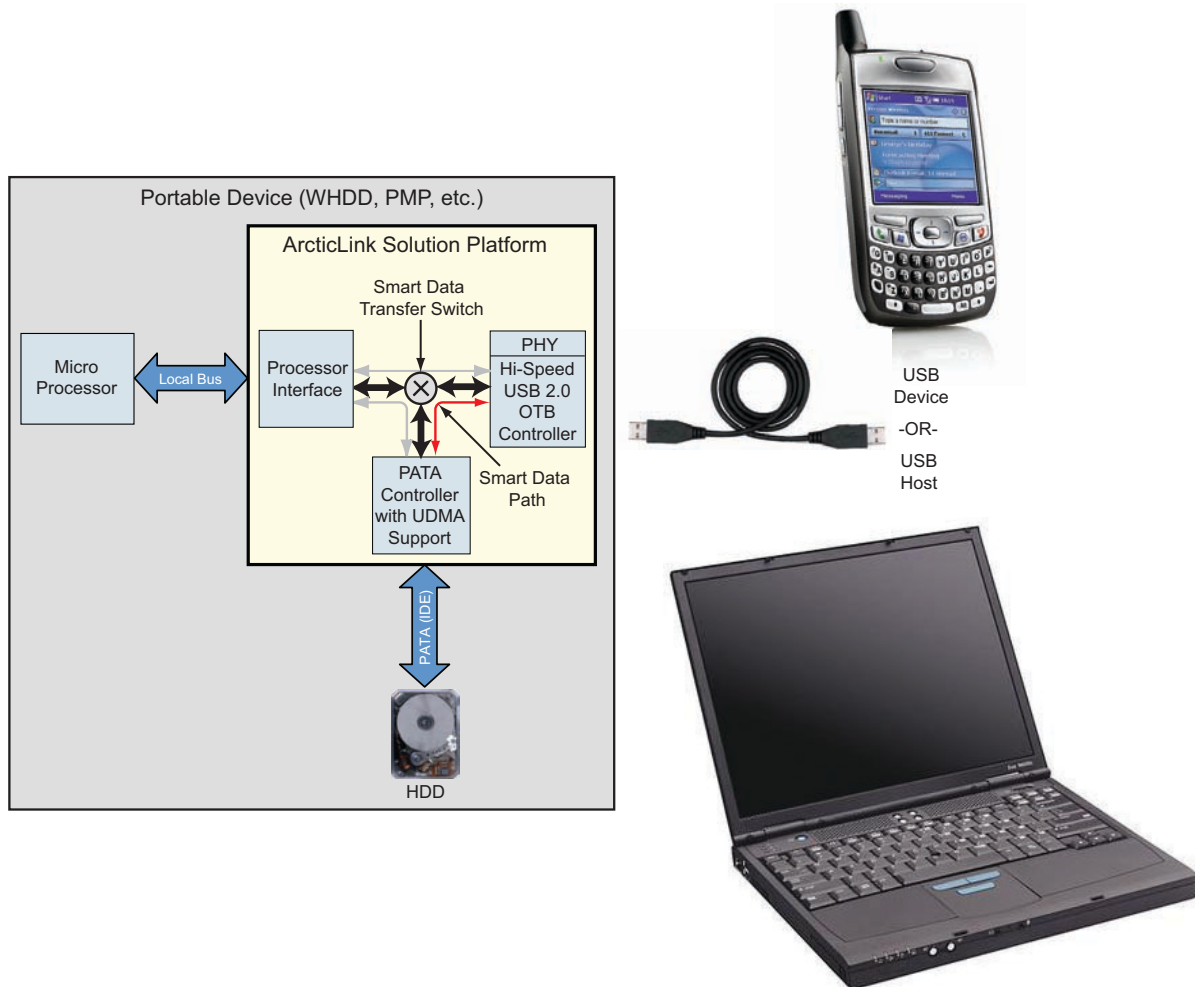
As a processor adds more capabilities, it has to support multiple high throughput data streams in the system, such as 3G, WiFi, USB and storage. When managing the data flows among different interfaces, the processor can easily become the bottleneck of the whole system performance. The conventional approach moves data first through one interface to the main memory and then writes it out through another interface which is highly inefficient in terms of performance and power consumption. A direct data path between two interfaces without processor intervention can achieve much higher throughput and lower power consumption at the same time.

QuickLogic's USB-IDE Smart Data Transfer (SDT) solution is designed to significantly improve the performance between the high speed USB to an IDE/PATA-based hard drive. It is implemented on QuickLogic's low power programmable ArcticLink Platform which features a Hi-Speed USB 2.0 OTG controller with built-in PHY. An integrated IDE/PATA controller supports both PIO, multiword DMA and UDMA mode. The data throughput with the direct path between the two interfaces is up to 32 Mbytes/sec. The programmable platform also offers a path to CE-ATA, a new lower pin count hard drive standard for the consumer electronics market.

Smart Data Transfer Architecture

Figure 1 is a system level block diagram that shows USB and IDE interface augmented by QuickLogic's SDT capability to achieve higher throughput and lower power consumption.

Figure 1: SDT System Level Block Diagram



Interface List and Description

The processor interface is customizable for different processor interfaces. **Table 1** shows an example pin description for the Marvell PXA3xx processor which includes the name, type, description of the ports, and the inputs/outputs that can connect off chip. The USB plus IDE module has a total of 11 external pins for the slave interface and 43 for the processor interface.

NOTE: All signals are active high unless otherwise indicated; signals with an “n” suffix are active low. The bank for each signal is shown where required.

Table 1: Example of a Marvell PXA3xx Processor Pin Description

Pin	Type	Description
System Interface		
RESET_N	I	System Reset. Used as hardware reset for USB and IDE Host Controllers.
CCLK	I	System Clock. 12 MHz system clock input.
MCLK	I	System Clock. 33 MHz system clock input.
VCCIO_ASSP	I	Input Voltage Tolerance Pin. Voltage rail for RESET_N, OTG_CLK, and OTG_DRV_VBUS (connect to 3.3 V or 1.8 V depending on what the external charge pump can accept for the OTG_DRV_VBUS signal level).
CPU Interface		
DF_I/O[15:0]	I/O	Data/Address. Bidirectional DFI data/address bus.
INT	O	Interrupt. Interrupt request from the CSSP.
DF_nWE	I	Write Enable. DFI write enable input.
DF_nOE	I	Output Enable. DFI output enable input.
NCS	I	Chip Select. DFI chip select.
DF_nLUA	I	Address Latch. Latch upper address.
DF_nLLA	I	Address Latch. Latch lower address.
RDY	O	Address Latch. Signal for inserting wait states to the CPU. 0: Wait 1: Ready
IDE Interface		
IDE_D[15:0]	I/O	ATA Data. Bi-directional data lines to external device.
IDE_nRESET	O	Reset. Active low reset output to external device.
IDE_nCS[1:0]	O	Chip Select. Chip selects for external device registers.
IDE_A[2:0]	O	Address. Address bits for registers in external device.
IDE_INTRQ	I	Interrupt. Interrupt request from external device.
IDE_DMARQ	I	DMA REQ. Indicates that the device is ready for a DMA transfer.
IDE_nDMACK	O	DMA ACK. Indicates that a DMA transfer is about to begin.
IDE_nDIOW	O	IO Write. Write strobe for device accesses.
IDE_nIOR	O	IO Read. Read strobe for device accesses.
IDE_IORDY	I	IO Ready. Indicates that external device is ready for access.
IDE_nPWR	O	IDE Power Control. Controls power switch to apply power to external device.

Table 1: Example of a Marvell PXA3xx Processor Pin Description (Continued)

Pin	Type	Description
USB OTG Interface		
VBUS_OTG	I	Vbus. Pin used by the Hi-Speed USB 2.0 OTG Controller to monitor the Vbus.
OTG_DP	I/O	D+. Positive channel of serial USB cable.
OTG_DM	I/O	D-. Negative channel of serial USB cable.
OTG_ID	I	ID. USB ID pin of mini-AB connector.
VCCA_OTG	I	IO Power. Analog 3.3 V supply for OTG PHY.
GND_A_OTG	I	IO Ground. Analog ground for OTG PHY.
VCCP_OTG	I	PLL Power. 1.8 V supply pin for the OTG PHY PLL.
GND_P_OTG	I	PLL Ground. Ground pin for the OTG PHY PLL.
OTG_RREF	Analog	Reference Resistor. OTG external reference resistor. Tie to GND via a 5.76 K $\pm 1\%$ resistor.
OTG_DRV_VBUS	O	Vbus Drive Enable. This pin is used by the Hi-Speed USB 2.0 OTG Controller to enable the external 5 V power supply (charge pump) to drive the VBUS USB line.
OTG_CLK	I	OTG Clock. 12 MHz reference clock used for OTG PHY. Must be ± 500 ppm.

QuickLogic CSSP

Memory Map

Table 2 shows an example of a QuickLogic CSSP memory map for the Marvell PXA3xx processor using the offset addresses. The QuickLogic CSSP is connected to one of the PXA3xx's chip selects and appears in the PXA3xx memory map as an offset from the base address of the chip select.

Table 2: Example CSSP Memory Map for a Marvell PXA3xx Processor

Offset Address [25:0]	Description
0x0000_0000 – 0x0000_0FFF	Common Registers
0x0000_1000 – 0x0000_1FFF	Reserved
0x0000_2000 – 0x0000_7FFF	Reserved
0x0000_8000 – 0x0000_9FFF	SRAM
0x0000_A000 – 0x0003_FFFF	Reserved
0x0004_0000 – 0x0007_FFFF	USB OTG
0x0007_FFFF – 0x00FF_FFFF	Reserved
0x0100_0000 – 0x0100_1FFF	IDE Host Controller
0x0100_2000 – 0x03FF_FFFF	Reserved

Register Description

Common Register Memory Map (0x0000_0000 – 0x0000_0FFF)

Name	Address	Size	Type	Description
COM_ID	0x0000000	32	R	Identification Register
COM_FEATURE	0x0000004	32	R	Feature Register
COM_INT_EN	0x0000008	32	R/W	Interrupt Enable Register
COM_INT_STAT	0x000000c	32	R	Interrupt Status Register
COM_FTR_EN	0x0000010	32	R/W	Feature Enable Register
COM_USB_MAP	0x0000014	32	R	USB Address Mapping Register
COM_CLK_EN	0x0000018	32	R/W	Clock Enable Register

COM_ID – Identification Register

Address Offset: 0x0000000

Size: 32-bits

Type: Read

Reset Value: 0x0047

Name	Bit(s)	Type	Reset Value	Description
RESERVED	31:12	R	-	Reserved
CSSP_ID	11:0	R	0x047	This is the identification number for this CSSP design.

COM_FEATURE – Feature Register

Address Offset: 0x00000004

Size: 32-bits

Type: Read

Reset Value: 0x0026

Name	Bit(s)	Type	Reset Value	Description
RESERVED	31:9	R	0x0	Reserved
USB_CFG	8	R	0x1	This bit is set to 1 to indicate that this CSSP has a USB controller.
RESERVED	7:4	R	0x0	Reserved
IDE_CFG	2	R	0x1	This bit is set to 1 to indicate that this CSSP has an IDE Host Controller.
SRAM_CFG	1	R	0x1	This bit is set to 1 to indicate that this CSSP has an internal SRAM.
BUS16_CFG	0	R	0x0	This bit is set to 0 to indicate that this CSSP has a 16-bit Host bus interface.

COM_INT_EN – Interrupt Enable Register

Address Offset: 0x00000008

Size: 32-bits

Type: Read/Write

Reset Value: 0x0000

Name	Bit(s)	Type	Reset Value	Description
RESERVED	31:29	R	-	Reserved.
IDE_INT_EN	28	R/W	0x0	IDE interrupt enable. If set to 1, the CSSP interrupts the processor when the IDE Host Controller generates an interrupt.
RESERVED	27:9	R	-	Reserved.
USB_INT_EN	8	R/W	0x0	USB interrupt enable. If set to 1, the CSSP interrupts the processor when the USB controller generates an interrupt.
RESERVED	7:0	R	-	Reserved.

COM_INT_STAT – Interrupt Status Register

Address Offset: 0x000000C

Size: 32-bits

Type: Read

Reset Value: 0x0000

Name	Bit(s)	Type	Reset Value	Description
RESERVED	31:29	R	-	Reserved.
IDE_INT_STAT	28	R	X	IDE interrupt status. If set to 1, the IDE Host Controller has generated an interrupt.
RESERVED	27:9	R	0x0	Reserved.
USB_INT_STAT	8	R	X	USB interrupt status. If set to 1, the USB controller has generated an interrupt.
RESERVED	7:0	R	-	Reserved.

COM_FTR_EN – Feature Enable Register

Address Offset: 0x0000010

Size: 32-bits

Type: Read/Write

Reset Value: 0x0000

Name	Bit(s)	Type	Reset Value	Description
RESERVED	31:19	R	-	Reserved
PHY_SUSPEND	18	R/W	0x0	USB PHY Suspend
VBUS_DISABLE	17	R/W	0x0	USB PHY VBUS Comparator Disable
BIST_ENABLE	16	R/W	0x0	USB PHY BIST Enable
RESERVED	15:5	R	-	Reserved
PHY_ENABLE	4	R/W	0x0	USB PHY Enable
USB_ENABLE	3	R/W	0x0	USB Enable
RESERVED	2:0	R	-	Reserved

COM_USB_MAP – USB Address Mapping Register

Address Offset: 0x0000014

Size: 32-bits

Type: Read

Reset Value: 0xF000

Name	Bit(s)	Type	Reset Value	Description
MAP_ADDR	31:28	R	0xF	Map Address
RESERVED	27:0	R	-	Reserved

COM_CLK_EN – Clock Enable Register

Address Offset: 0x1000018

Size: 32-bits

Type: Read/Write

Reset Value: 0x0000

Name	Bit(s)	Type	Reset Value	Description
RESERVED	31:5	R	-	Reserved
PHY_CLK_EN	4	R/W	0x0	USB PHY Clock Enable
SYS_CLK_EN	3	R/W	0x0	System Clock Enable
RESERVED	2:0	R	-	Reserved

IDE Host Controller Memory Map (0x0100_0000 – 0x0100_1FFF)

Name	Address	Size	Type	Description
IDE_CFG	0x1000040	16	R/W	Configuration Register
IDE_CTL_STAT	0x1000044	16	R/W	Status Register
IDE_T1	0x1000050	16	R/W	IDE Timing Register 1
IDE_T2	0x1000054	16	R/W	IDE Timing Register 2

IDE_CFG - Configuration Register

Address Offset: 0x1000040

Size: 16-bits

Type: Read/Write

Reset Value: 0x1300

Name	Bit(s)	Type	Reset Value	Description
REV_ID	15:12	RO	The current revision of the IP	Revision ID
RESERVED	11	RO	0	N/A
CLK_ENB	10	R/W	0	Internal Clock Enable 0 – Internal Clock enabled 1 – Internal Clock disabled
RP_EN	9	RO	1	Read Prefetching Enable 0 – PIO Read Prefetching disabled 1 – PIO Read Prefetching enabled
WP_EN	8	RO	1	Write Posting Enable 0 – PIO Write Posting disabled 1 – PIO Write Posting enabled
RESERVED	7	RO	0	N/A
MODE_SETTING	6:5	R/W	00	Operating Mode 00 – PIO mode 01 – Ultra DMA mode 10 – Multiword DMA mode 11 – reserved
RESERVED	4:3	RO	0	N/A
IDE_RST	2	R/W	0	IDE Reset 0 – IDE Reset de-asserted 1 – IDE Reset asserted
RESERVED	1	RO	0	N/A
IDE_PWR_TG	0	R/W	0	IDE Power Toggle 0 – IDE Power OFF 1 – IDE Power ON

IDE_CTL_STAT – Control/Status Register

Address Offset: 0x1000044

Size: 16-bits

Type: Read/Write

Reset Value: 0x0014

Name	Bit(s)	Type	Reset Value	Description
RESERVED	15:12	RO	0	N/A
SOFT_RST	11	R/W	0	IDE Host Controller soft reset
DMA_DIR	10	R/W	0	DMA direction bit, self-clearing 0 – UDMA datapath will be through CPU 1 – UDMA datapath will be through USB
WRITE_DMA_START	9	R/W	0	Write DMA start bit, self-clearing
READ_DMA_START	8	R/W	0	Read DMA start bit, self-clearing
RFIFO_THRESHOLD_EN	7	RO	0	Read FIFO threshold interrupt enable
WFIFO_THRESHOLD_EN	6	RO	0	Write FIFO threshold interrupt enable
RESERVED	5	RO	0	N/A
IDE_INT_EN	4	R/W	1	IDE Interrupt Enable 0 – IDE Interrupt disabled 1 – IDE Interrupt enabled
RFIFO_THRESHOLD	3	RO	0	Read FIFO threshold – Read FIFO has at least 512 bytes of data
WFIFO_THRESHOLD	2	RO	1	Write FIFO threshold – Write FIFO has room for at least 512 bytes of data
DMARQ	1	RO	Reflects the value of the IDE DMA request pin.	IDE DMA Request 0 – IDE DMA Request Signal NOT asserted 1 – IDE DMA Request Signal asserted
IDE_INT	0	RO	Reflects the value of the IDE interrupt input pin.	IDE Interrupt 0 – IDE Interrupt NOT asserted 1 – IDE Interrupt asserted

IDE_T1 – IDE Timing Register 1

Address Offset: 0x1000050

Size: 16-bits

Type: Read/Write

Reset Value: 0x0502

Name	Bit(s)	Type	Reset Value	Description
RESERVED	15:13	RO	0	N/A
T2	12:8	R/W	00101	DIOR#/DIOW# pulse width
RESERVED	7:2	RO	0	N/A
T1	1:0	R/W	10	Address valid to DIOR#/DIOW# setup

IDE_T2 – IDE Timing Register 2

Address Offset: 0x1000054

Size: 16-bits

Type: Read/Write

Reset Value: 0x0458

Name	Bit(s)	Type	Reset Value	Description
RESERVED	15:11	RO	0	N/A
Teoc	10:8	R/W	100	End of cycle time for PIO/MWDMA modes
RESERVED	7	RO	0	N/A
Tcvs	6:4	R/W	101	Data/CRC valid setup time for UDMA mode
Tcyc	3:0	R/W	1000	Cycle time for UDMA mode

USB Host Controller Memory Map

For more information about QuickLogic's Hi-Speed USB 2.0 OTG Controller registers, see the *ArcticLink Solution Platform User Manual*.

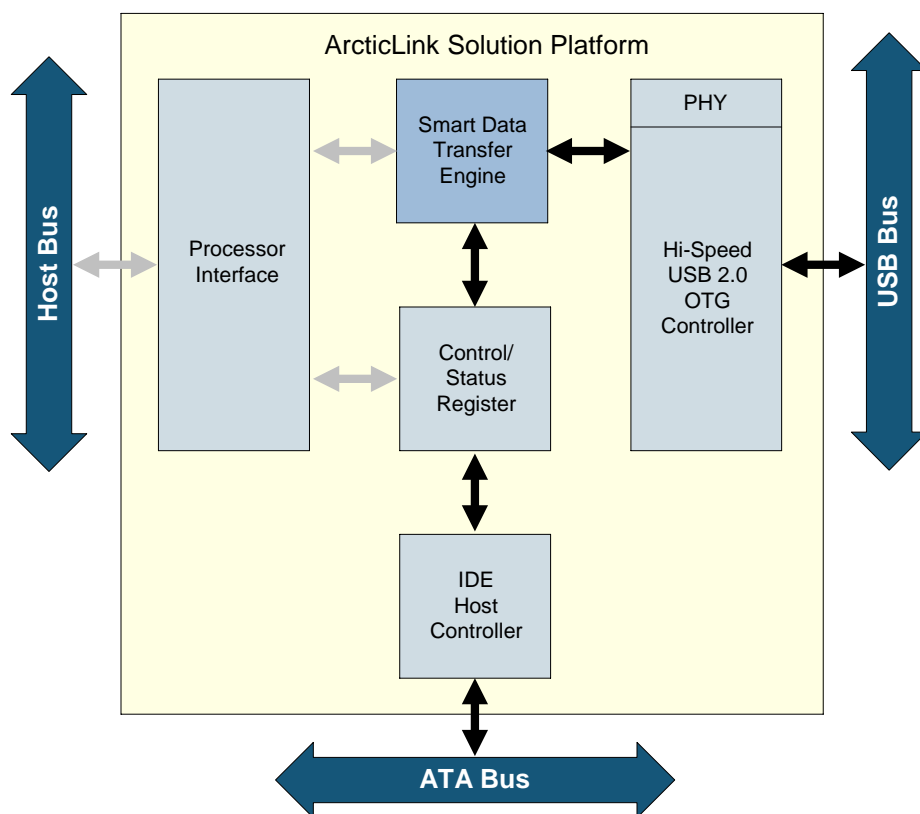
Functional and Module Description

The QuickLogic CSSP design consists of the following modules:

- Processor Interface
- IDE Host Controller
- Hi-Speed USB 2.0 OTG Controller
- SDT Engine
- Control/Status Registers

Figure 2 illustrates the logical connections between each module in the CSSP.

Figure 2: Quicklogic CSSP System Architecture



Processor Interface

The processor interface communicates to the Host bus. It is responsible for decoding the local address of the transfer, and steering the transaction to the CSSP registers, internal SRAM or the IDE interface. All local bus byte lanes are assumed to be enabled at all times.

The processor can access the hard-drive via this module. Depending on the decoded local address, this module will activate the IDE interface or internal registers to complete the transaction.

IDE Host Controller

The IDE interface can perform transfers to the hard-drive in any of the PIO Modes (0, 1, 2, 3 or 4), in Multiword DMA (MWDMA) Modes 0 to 2 and in UDMA Modes 0 to 4. The processor can control the access timing for PIO, MWDMA, and UDMA modes via the *IDE_T1* and *IDE_T2* registers.

The IDE interface has a 512-word Read FIFO. The Read FIFO allows read-prefetching in PIO/MWDMA modes to increase the PIO/MWDMA data transfer rates. Data prefetching is initiated when an IDE data port read occurs. The first data port read of an IDE device sector is called the demand read. Subsequent data port reads from the same sector are called prefetch reads. In UDMA mode the Read FIFO is filled automatically when the DMA is started and not on a port read.

Similarly, the IDE interface has a 512-word Write FIFO that allows the Host write transactions to complete faster. This module will concurrently perform the IDE write transfers to the IDE data port as the data is being written into the Write Posting Buffer.

The hard-drive's ATA registers are memory-mapped so they are accessible to the processor. Refer to **IDE Host Controller Memory Map (0x0100_0000 – 0x0100_1FFF)** on page 8 for more details about IDE-related registers.

For more information about QuickLogic's IDE Host Controller, see the *IDE Host Controller Data Sheet*.

Hi-Speed USB 2.0 OTG Controller

The Hi-Speed USB 2.0 OTG Controller contains the USB OTG Controller core, integrated PHY, dedicated Rx and Tx FIFO, and dedicated DMA engine. The Hi-Speed USB 2.0 OTG Controller core connects to the peripheral bus SRAM interface (in which case Programmable Fabric is master) or Fast Peripheral Bus SRAM interface (in which case ASSP is master) and communicates with the application and off-chip system memory. The Hi-Speed USB 2.0 OTG Controller is a Dual-Role Device (DRD) controller that supports host and device functions, and can be configured as host-only or device-only.

The Hi-Speed USB 2.0 OTG Controller provides two modes of operation:

- Slave-only mode (optional)
- Internal DMA mode (USB 2.0 OTG Controller core to/from scratchpad 8 KB SRAM or Programmable Fabric)

By default, Internal DMA mode is enabled. In this mode, the dedicated DMA controller manages the data transfer between system memory (or the internal scratchpad 8 KB SRAM) and the dedicated FIFOs through the Fast Peripheral Bus SRAM interface. The Fast Peripheral Bus SRAM interface allows the application to access the Rx and Tx Data FIFOs when Internal DMA mode is enabled via the scratchpad 8 KB SRAM.

For more information about QuickLogic's Hi-Speed USB 2.0 OTG Controller, see the *ArcticLink Solution Platform User Manual*.

SDT Engine

The CSSP device is capable of transferring data from the USB to the IDE directly without the need for the data to be transferred off chip. Direct data path transfers use the USB DMA engine to move the BULK IN and BULK OUT data directly to the IDE read and write FIFOs. Software running on the attached CPU programs the USB DMA engine based on the requests it receives from the USB connected Host computer. The CPU processes the USB Mass Storage requests received on the BULK OUT endpoint. When the request indicates a disk read, the CPU first programs the IDE Host Controller to begin to read the data in UDMA mode from the hard disk and then programs the USB BULK IN endpoint DMA registers to transfer the requested data. The USB DMA engine uses the IDE Host Controller's read FIFO threshold signal to determine when data is available. When data is available the USB DMA engine reads the data from the IDE read FIFO and transfers it onto the USB bus. When the request indicates a disk write the CPU first programs the IDE Host Controller to begin to a write transaction in UDMA mode to the hard disk and then programs the USB BULK OUT endpoint DMA registers to transfer the requested data. The USB DMA engine uses the IDE Host Controller's write FIFO threshold signal to determine when space is available in the FIFO. When space is available the USB DMA engine reads the data from the USB bus and writes it to the IDE write FIFO. Once the IDE Host Controller has been programmed to start the transaction and the USB DMA registers have been programmed to perform the data movement the CPU is no longer involved in the data transfer until it is completed and an interrupt is generated from the USB DMA engine to the CPU.

Control/Status Registers

The control/status registers can be used to manage the behavior of the CSSP, and report the status of various flags.

There are three sets of registers in the CSSP:

- Common register set
- IDE register set
- USB register set

Each of these register sets are memory-mapped to the processor, and are only accessible by the processor. Writing to reserved registers has no effect, and reading from reserved registers yields undefined values. Refer to **Memory Map** on page 4 details about each register.

Supported Operating Systems

The SDT between USB 2.0 OTG and IDE interfaces PSB supports the following operating systems:

- Windows® CE
- Linux®

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Revision History

Revision	Date	Originator and Comments
A	June 2008	Stanley Hung, Howard Li, and Kathleen Murchek

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