QuickLogic Reliability Report 2011

Introduction

This report summarizes QuickLogic Product Reliability. QuickLogic has established aggressive reliability objectives to assure that all products exhibit reliability exceeding customer reliability requirements for purchased components. In addition, the QuickLogic quality standard results in a culture requiring continuous product improvement in quality and reliability. This report includes data from the QuickLogic technology families (0.65 µm, 0.35 µm, 0.25 µm, and 0.18 µm).

Product Reliability data is accumulated as a result of new product Qualification Plan activities as well as from the Reliability and Quality Monitoring Program. All reliability test samples are obtained from standard production material. Sample selection is based on generic product families. These generic products are designed with similar design rules and manufactured from a core set of processes. The reliability strategy requires that every failure encountered during reliability testing be subjected to failure analysis to determine the failure mechanism. A corrective action is then implemented to prevent future failures. The result of this process is continuous improvement in product performance and reliability.

Reliability and Quality Monitoring Programs

The Reliability and Quality Monitoring Programs of new processes, new products/devices and new package/assembly vendors are designed to ensure that QuickLogic products satisfy the internal and external customer requirements before transferring into production.

The Reliability and Quality Monitoring program requirements are outlined in **Table 1** through **Table 4**.

Table 1: Requirement for Wafer Process Qualification

Test No.	Reliability Test	Reference Spec. Mil-Std-883/ JEDEC/STACK	Condition	Duration	Lot Qty.	SS/Lot	Acceptance
A	High Temperature Operating Life (HTOL)	Mil-Std-833 Mtd 1005	T = 125°C[a], Vccmax Dynamic OR Vccmax, T = 125°C	168, 1,000 hours Optional Read Pt 500 OR 168, 500 hours	3	50	0 fail
B	Low Temperature Operating Life (LTOL)	Mil-Std-833 Mtd 1005	T = -55°C Vccmax, 1 MHz	168, 500 hours	3	50	0 fail
C	Temperature Humidity Bias (THB) with Preconditioning OR High Accelerated Stress Test (Biased HAST) with Preconditioning	JESD22-A101, JEDEC22-A113 OR JESD11-A110, JEDEC22-A113	T = 85°C 85% R.H., Pins alt. Bias Vccmax OR T = 110°C 85% R.H., 17.7 psia, Pins alt. Bias Vccmax	Post Preconditioning, 168, 500, 1,000 hours OR Post Preconditioning, 264 hours	1 or 2	45 (min. sample size)	LPTD = 5 @90% confidence
D	Temperature Cycling (TC) with Preconditioning	JESD22-A104, JEDEC22-A113	T = -65°C/+150°C OR for Laminate T = -55°C/+125°C[b]	300 cycles OR 1,000 cycles	1 or 2	45 (min. sample size)	LPTD = 5 @90% confidence
E	High Temperature Storage (HTS)	Mil-Std-883 Mtd 1008	T = 150°C, unbiased	168 Opt., 500 Opt., 1,000 hours	1 or 2	45 (min. sample size)	LPTD = 5 @90% confidence
F	SEM Analysis or Construction Analysis				1	1	

a. For 0.35 µm and older technology, the temperature is 150°C.
b. For Plastic Quad Flat Pack (PQFP) packages use conditions of -65°C/+150°C (air to air) and 300 cycles.
For Plastic Ball Grid Array (PBGA) packages use conditions of -55°C/+125°C (air to air) and 1,000 cycles.

Table 2: Requirement for Device Qualification

Reliability Test	Reference Spec. Mil-Std-883/ JEDEC/STACK	Condition	Duration	Lot Qty.	SS/Lot	Acceptance
ESD	Mil-Std-883 Mtd 3015.7/JEDEC	HBM	>2,000 Volts all pins	1	3	0 fail
Latch-Up	EIA/JESD78	QL Spec. 08-003	Current injection T = 25°C	1	6	0 fail

Table 3: Requirement for Plastic Package/Assembly Qualification

Test No.	Reliability Test	Reference Spec. Mil-Std-883/ JEDEC/STACK	Condition	Duration	No. of Lots	SS	Acceptance
1	Temperature Humidity Bias (THB) with Preconditioning OR High Accelerated Stress Test (Biased HAST) with Preconditioning	JESD22-A101-B, JESD22-A113 OR JESD22-A101, JESD22-A113	T = 85°C 85% R.H., Pins alt. Bias Vccmax OR T = 110°C 85% R.H., 17.7 psia, Pins alt. Bias Vccmax	Post Preconditioning, 168, 500, 1,000 hours OR Post Preconditioning, 264 hours	1 or 2	45	LPTD = 5 @90% confidence
2	Temperature Cycling (TC) with Preconditioning	JESD22-A104, JEDEC22-A113	T = -65°C/+150°C OR for Laminate T = -55°C/+125°C	300 cycles OR 1,000 cycles	1 or 2	45	LPTD = 5 @90% confidence
3	High Temperature Storage (HTS)	Mil-Std-833 Mtd 1008	T = 150°C, unbiased	168 Opt., 500 Opt., 1,000 hours	1 or 2	45	LPTD = 5 @90% confidence
4	Pressure Pot with Preconditioning[a] OR Unbiased HAST with Preconditioning[a]	JESD22-A102-C, JEDEC22-A113 OR JESD22-A118, JEDEC22-A113	T = 121°C, 30 psia, saturated steam OR T - 110°C, 85% R.H., 17.7 psia	96 hours OR 264 hours	1 or 2	45	LPTD = 5 @90% confidence
5	Moisture Sensitivity	J-STD-020	Per Spec. J-STD-020		1 or 2	45	Determine Level
6	Solderability				1	3	0 fail
7	Ball Shear				1	5	0 fail
8	Bond Pull				1	5	0 fail
9	Physical Dimension				1	15	LPTD = 15 @90% confidence

a. Unbiased HAST for BGA package and Pressure Pot for all other packages.

Table 4: Qualification Requirement Summary

Technology	New Process, New Device	Qualified Process, New Device	Qualified Process and Device, New Package	Qualified Process and Device, Package, New Assembly Facility
0.65 µm[a]	Table 1, 2, 3	Table 1, 2, 3	Table 3	Table 3
0.35 µm[b]	Table 1, 2, 3	Table 1, 2, 3	Table 3	Table 3
0.25 µm[c]	Table 1, 2, 3	Table 1, 2, 3	Table 3	Table 3
0.18 µm[d]	Table 1, 2, 3	Table 1, 2, 3	Table 3	Table 3

a. pASIC1 and pASIC2 products.
b. pASIC3, QuickRAM, and QuickPCI products.
c. Eclipse, EclipsePlus, and QuickPCI products.
d. Eclipse II, EclipseE, QuickPCI, PolarPro, ArcticLink, and ArcticLink II products.

Failure Rate Calculation

Reliability is the probability that a semiconductor device will perform its specified function in a given environment for a specified period of time. In other words, reliability is quality over time and environmental conditions.

The most frequently used reliability measure for semiconductor devices is the failure rate (λ). The failure rate is obtained by dividing the number of failures observed by the product of the number of devices on test and the interval in hours, usually expressed as percent per thousand hours or failures per billion device hours (FITS). The relationship between failure rate and the chi-square distribution is as follows:

$$\text{Failure Rate} = \lambda = \frac{\chi^2(\alpha, df)}{2t}$$

Where:

λ = failure rate

χ^2 = chi-square function

α = (100 – confidence level) / 100

df = degrees of freedom = 2r + 2

r = number of failures

t = device hours (number of devices x number of hours x acceleration factor)

In the failure rate calculation, acceleration factors (AF) are used to derate the failure rate from the thermally accelerated life test conditions to a failure rate indicative of actual use temperature. The acceleration factor is calculated using the Arrhenius equation:

$$AF = \exp\left\{\frac{Ea}{K}\left[\frac{1}{T_{use}} - \frac{1}{T_{stress}}\right]\right\}$$

Where:

AF = Acceleration Factor

Ea = Thermal Activation Energy (0.7ev is assumed and used in the failure rate calculation)

K = Boltzmann's Constant (8.63×10^{-5} ev/K)

T_{use} = use Temperature (°C + 273)

T_{stress} = Life Test Stress Temperature (°C + 273)

Data Summaries

Table 5 summarizes the High Temperature Life test data.

Table 5: HTOL Summary for QuickLogic Devices

Technology	0.65 µm	0.35 µm	0.25 µm	0.18 µm
Failure	9 fails	7 fails	0 fail	2 fail
Equivalent Device hours at 55°C	7.30E+08	4.40E+08	3.10E+07	100E+08
FIT Rate[a]	14.4	18.9	29.6	28.0
MTBF[b]	6.94E+07	5.29E+07	3.38E+07	3.57E+07

a. FIT is calculated based on 0.7ev, 60% C.L. and T_j of 55°C.
b. MTBF is calculated as MTBF = 10E+09/FIT rate.

Table 6 through **Table 11** summarize the reliability results:

Table 6: HTOL Results

Technology	Number of Units Tested	Number of Failures
0.65 µm	6,424	9[a]
0.35 µm	2,957	7[b]
0.25 µm	997	0
0.18 µm	1,640	2[c]

a. Causes of failures for 0.65 µm technology:
1. due to gate oxide.
2. due to a particle.
3. and 4. due to metal short.
5., 6., 7., 8., and 9. due to noise in Vcc supply signal.

b. Causes of failures for 0.35 µm technology:
1. and 2. due to incorrect power supply
3. and 4. due to latch up.
5., 6., and 7. due to incorrect programming algorithm.

c. Causes of failures for 0.18 µm technology:
1. and 2. due to particles.

Table 7: LTOL Results

Technology	Number of Units Tested	Number of Failures
0.65 µm	3,635	4[a]
0.35 µm	554	0
0.25 µm	930	0
0.18 µm	2,623	0

a. Causes of failures for 0.65 µm technology:
1. and 2. due to metal short.
3. and 4. due to surge on power supply.
None of the failures were related to the programmed ViaLink.

Table 8 summarizes the ESD and latch-up testing.

Table 8: ESD and Latch-Up Summary

Technology	ESD Summary			Latch-Up Summary		
	Voltage	Reference Spec. Mil-Std-883/JEDEC	Condition	Itrigger Limit	Reference Spec.	Condition
0.65 µm	2,000 V	Mil_Std_883 Mtd 3015.7	HBM	±200 mA	EIA/JESD78	QL Spec. 08-003
0.35 µm	2,000 V	Mil_Std_883 Mtd 3015.7	HBM	±200 mA	EIA/JESD78	QL Spec. 08-003
0.25 µm	2,000 V	Mil_Std_883 Mtd 3015.7	HBM	±100 mA	EIA/JESD78	QL Spec. 08-003
0.18 µm (QL8xxx and QL58xx)	2,000 V[a]	JEDEC	HBM	±100 mA	EIA/JESD78	QL Spec. 08-003
0.18 µm (QL6xxxE)	2,000 V[b]	JEDEC	HBM	±100 mA	EIA/JESD78	QL Spec. 08-003
0.18 µm (QL1Pxxxx)	2,000 V	Mil_Std_883 Mtd 3015.7	HBM	±100 mA	EIA/JESD78	QL Spec. 08-003
0.18 µm (QL1Axxx and QL2xxxx)	2,000 V	JEDEC	HBM	±100 mA	EIA/JESD78	QL Spec. 08-003

a. 2 KV JEDEC except when being zapped with respect to Vded, 1 KV JEDEC when being zapped with respect to Vded.
b. 208 QFP package is 750 V.

Table 9 through **Table 14** summarize the package reliability testing.

Table 9: 0.65 µm Technology – Leaded Package Data

Reliability Test	PLCC		PQFP		TQFP		PBGA	
	No. of Units Tested	No. of Failures	No. of Units Tested	No. of Failures	No. of Units Tested	No. of Failures	No. of Units Tested	No. of Failures
Temperature Humidity Bias (THB) OR High Accelerated Stress Test (Biased HAST)	482	3[a]	167	0	150	1[b]		
Temperature Cycling (TC)	918	1[c]	1,197	4	671	1[d]	90	0
High Temperature Storage (HTS)	210	0	225	0	135	0		
Pressure Pot OR Unbiased HAST	582	0	270	0	219	0	45	0

a. The THB failures were due to a particle.
b. The HAST failure was due to a metal short.
c. The temperature cycle failures were due to lifted bond.
d. See footnote c. above.

Table 10: 0.35 µm Technology – Leaded Package Data

Reliability Test	PLCC		PQFP		TQFP		PBGA	
	No. of Units Tested	No. of Failures	No. of Units Tested	No. of Failures	No. of Units Tested	No. of Failures	No. of Units Tested	No. of Failures
Temperature Humidity Bias (THB) with Preconditioning OR High Accelerated Stress Test (Biased HAST) with Preconditioning	45 (Biased HAST)	0	50 (THB)	0	45	0	46 (Biased HAST)	0
Temperature Cycling (TC) with Preconditioning	274	0	1,836	1[a]	425	0	547	0
High Temperature Storage (HTS)	45	0	135	0	45	0	45	0
Pressure Pot with Preconditioning OR Unbiased HAST with Preconditioning	219 (Pressure Pot)	0	280 (Pressure Pot)	0	100	0	261	0

a. The failure was due to Vcc and GND short.

Table 11: 0.25 µm Technology – Leaded Package Data

Reliability Test	PQFP		PBGA		FBGA	
	No. of Units Tested	No. of Failures	No. of Units Tested	No. of Failures	No. of Units Tested	No. of Failures
Temperature Humidity Bias (THB) with Preconditioning OR High Accelerated Stress Test (Biased HAST) with Preconditioning	135	0	90 (Biased HAST)	0	90 (Biased HAST)	0
Temperature Cycling (TC) with Preconditioning	181	0	325	0	135	0
High Temperature Storage (HTS)	45	0	45	0	45	0
Pressure Pot with Preconditioning OR Unbiased HAST with Preconditioning	136 (Pressure Pot)	0	325 (Unbiased HAST)	0	135 (Unbiased HAST)	0

Table 12: 0.18 µm Technology – Leaded Package Data

Reliability Test	MQFP		TQFP		TFBGA		LFBGA		PBGA	
	No. of Units Tested	No. of Failures	No. of Units Tested	No. of Failures	No. of Units Tested	No. of Failures	No. of Units Tested	No. of Failures	No. of Units Tested	No. of Failures
Temperature Humidity Bias (THB) with Preconditioning OR High Accelerated Stress Test (Biased HAST) with Preconditioning	90	0	45	0	45 (Biased HAST)	0	45 (Biased HAST)	0	45 (Biased HAST)	0
Temperature Cycling (TC) with Preconditioning	180	0	180	0	180	0	45	0	180	0
High Temperature Storage (HTS)	135	0	180	0	90	0	45	0	180	0
Pressure Pot with Preconditioning OR Unbiased HAST with Preconditioning	90 (Pressure Pot)	0	135 (Pressure Pot)	0	180 (Unbiased HAST)	0	45 (Unbiased HAST)	0	180	0
Preconditioning	495	0	675	0	495	0	225	0	635	0

Table 13: 0.18 µm Technology – Lead-Free Package Data

Reliability Test	PQN		PSN		PFN		PUN		PTN	
	No. of Units Tested	No. of Failures	No. of Units Tested	No. of Failures	No. of Units Tested	No. of Failures	No. of Units Tested	No. of Failures	No. of Units Tested	No. of Failures
Temperature Humidity Bias (THB) with Preconditioning OR High Accelerated Stress Test (Biased HAST) with Preconditioning	45	0	45 (Biased HAST)	0	45 (Biased HAST)	0	45 (Biased HAST)	0	45 (Biased HAST)	0
Temperature Cycling (TC) with Preconditioning	45	0	375	0	90	0	510	0	443	0
High Temperature Storage (HTS)	45		90		45	0	339294	0	355	0
Pressure Pot with Preconditioning OR Unbiased HAST with Preconditioning	45 (Pressure Pot)	0	90 (Un-biased HAST)	0	90 (Un-biased HAST)	0	90 (Un-biased HAST)	0	285 (Un-biased HAST)	0
Preconditioning	90	0	370	0	90	0	790	0	90	0

Table 14: 0.35 µm Technology – Lead-Free Package Data

Reliability Test	PQN		PSN		PFN		PTN		PBN	
	No. of Units Tested	No. of Failures	No. of Units Tested	No. of Failures	No. of Units Tested	No. of Failures	No. of Units Tested	No. of Failures	No. of Units Tested	No. of Failures
Temperature Humidity Bias (THB) with Preconditioning OR High Accelerated Stress Test (Biased HAST) with Preconditioning	90	0	45 (Biased HAST)	0	45 (Biased HAST)	0	0	0	0	0
Temperature Cycling (TC) with Preconditioning	180	0	90	0	45	0	90	0	90	0
High Temperature Storage (HTS)	90		90		45	0	0	0	0	0
Pressure Pot with Preconditioning OR Unbiased HAST with Preconditioning	90 (Pressure Pot)	0	90 (Unbiased HAST)	0	45 (Unbiased HAST)	0	0	0	90 (Unbiased HAST)	0
Preconditioning	90	0	90	0	45	0	0	0	180	0

Table 15: 0.18 µm Technology – WLCSP Package Data

Reliability Test	CSSP-EWDN110		CSSP-GWUN99		CSSP-XWDN64	
	No. of Units Tested	No. of Failures	No. of Units Tested	No. of Failures	No. of Units Tested	No. of Failures
Temperature Cycling (TC) with Preconditioning	90	0	45	0	95	0
Preconditioning	180	0	90	0	250	0

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Revision History

Revision	Date	Originator and Comments
Q2 2002 - Rev. A	August 2002	Brian Faith and Paul Micallef
Q1 2003 - Rev. A	June 2003	Brian Faith and Kathleen Murchek
Q4 2004 - Rev. A	April 2005	Sandya Radhakrishna and Kathleen Murchek
Q4 2004 - Rev. B	May 2005	Sandya Radhakrishna and Kathleen Murchek Updated equivalent device hours and FIT rate in Table 5 for 0.25 µm and 0.18 µm technologies.
Q1 2007 - Rev. A	April 2007	Sandya Radhakrishna and Kathleen Murchek Updated Tables 5 through Table 11. Added Lead-Free data, Table 13 and Table 14.
2008 - Rev. A	March 2008	Sandya Radhakrishna and Kathleen Murchek Updated Tables 1, 4, 5, 6, 7, 8,13, and 14.
2009 - Rev. A	July 2009	Sandya Radhakrishna and Kathleen Murchek Updated Tables 5, 6, 7, 13, and 14. Added Table 15.
2011 - Rev. A	July 2011	Sandya Radhakrishna and Kathleen Bylsma Updated Tables 5, 6, 7, 12, 13, and 15.

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