Solution Brief

QuickLogic® Connectivity Companion Devices

For the Marvell® PXA Processor Families

Solution Highlights

Value Proposition

- Turn-key solutions
- Fast time-to-market
- Cost-effective and customizable
- Low power consumption
- Ability to protect and leverage existing hardware/software

Solution Pack

- Proven IP solutions
- Software drivers
- Reference design files such as Gerber files, reference schematics, etc.
- User guide and documentation
- QuickLogic development boards (daughter card forPXA270 Developer's Kit (DVK))
- QuickLogic development software
- Customer support and access to QuickLogic's *MyDesign* website

Processors

- Marvell PXA2xx processor up to 624 MHz
- Marvell PXA3xx processor up to 800 MHz

Companion Devices

- IDE
  - IDE hard drive
  - DVD ROM
- PCI
  - 10/100/1000 Ethernet
  - Wi-Fi
  - USB 2.0
- SDIO
  - Wi-Fi
  - SD Card memory
  - Mobile TV
- CE-ATA
  - CE-ATA hard drive

Introduction

QuickLogic Companion Devices are low power, small form factor, cost-effective solutions that allow designers to reuse existing hardware/software and decrease the time-to-market. These pre-programmed turnkey solutions work right out of the box allowing customers to simply drop it into their system and accelerate their design cycle. Further customization is possible with QuickLogic's programmable FPGA technology, enabling the customers to meet specific design needs.

The types of connectivity available using QuickLogic Companion Devices are:

- **10/100/1000 Ethernet, Wi-Fi, or USB 2.0** via an integrated PCI controller
- **Hard Disk Drive or DVD ROM** via an integrated IDE controller
- **SD Card/SDIO, Wi-Fi, or Mobile TV** via an integrated SDIO controller
- **CE-ATA-Based Hard Disk Drive** via an integrated CE-ATA controller

These Companion Devices leverage QuickLogic's low power FPGA architectures to provide intelligent bridging solutions. They include IP, software drivers and evaluation boards, and have been proven on the Marvell® PXA2xx and PXA3xx families.

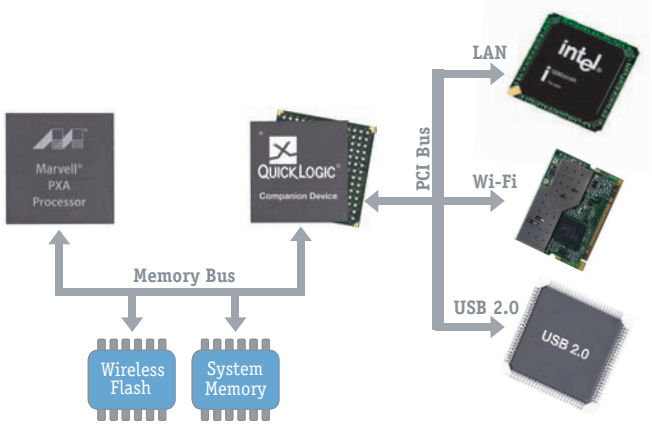
Figure 1: Complete QuickLogic Companion Device Solution

QuickLogic Companion Device with Integrated PCI Controller

PCI System Overview

Figure 2 illustrates a basic system block diagram that connects low cost chip sets such as 10/100/1000 Ethernet, Wi-Fi or USB 2.0 to the Marvell PXA2xx processor using the QuickLogic Companion Device with integrated PCI Controller. The processor serves as a host that configures and manages the system. The companion device operates as the host PCI bridge with a built-in arbiter, and can support multiple PCI agents, providing the ability to add multiple peripherals to the system such as Wi-Fi, 10/100/1000 Ethernet, and USB. DMA is supported for fast data transfer between PCI agents and system memory.

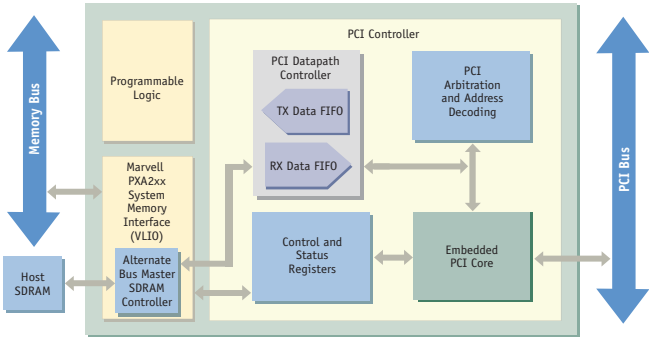
Figure 2: PCI Connectivity System Architecture



PCI Bridge Overview

The QuickLogic Companion Device with integrated PCI Controller implements connectivity to 10/100/1000 Ethernet, Wi-Fi or USB 2.0, and consists of the following functional blocks as shown in **Figure 3**.

Figure 3: PCI Companion Device Block Diagram



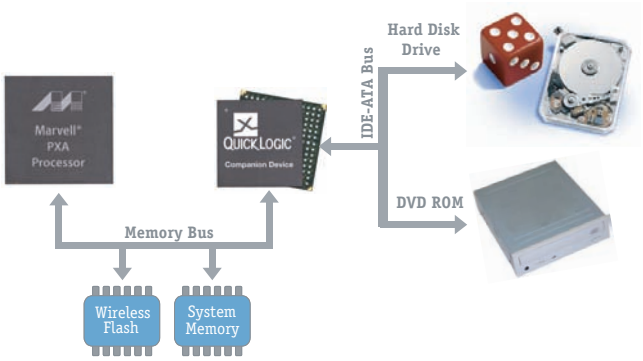
- **PXA VLIO Interface:** The local bus interface, through use of the RDY signal, handles the PXA's Variable Latency Input and Output (VLIO) bus automatically. The RDY signal is used to properly synchronize the companion device's responses to the CPU read and write commands during high-speed bus operation.
- **Programmable Logic:** This block provides designers with programmable logic to implement additional functionality. This can be used to integrate board level glue logic, consolidate various digital functions or implement custom functions.
- **PCI Core:** Manages communications between the host interface and the PCI bus to perform the desired transaction on the PCI bus. The PCI core is a 32-bit/ 33-MHz Host/Master/Target controller that connects to the PCI bus. See www.quicklogic.com/pci for detailed information on QuickLogic PCI products.
- **PCI Arbiter and Decode:** Responsible for managing PCI bus control between the companion device, and other PCI agents on the bus. It also handles address decoding during PCI accesses and support for several agents on the PCI bus.
- **PCI Datapath Controller:** Provides the PCI agents access to host SDRAM and allows the PXA processor the ability to initiate read/write transactions to PCI memory and configuration spaces.
- **SDRAM Controller:** Arbitrates for the host processor memory bus and controls the host SDRAM during transfers initiated from PCI.
- **Control/Status Registers:** Accessible from Host Interface block to provide control/status information for the local processor.

QuickLogic Companion Device with Integrated IDE Controller

IDE System Overview

Figure 4 illustrates the basic system block diagram of adding HDD or DVD ROM storage to the Marvell PXA2xx and PXA3xx processors using the QuickLogic Companion Device with integrated IDE Controller. The processor serves as the host in the system and manages traffic to and from the HDD. The companion device connects to the CPU through its static memory interface (VLIO interface). Utilizing the hardware DMA on the processor, the companion device offloads the CPU during data transfers to and from the HDD, providing improved system performance and reduced system power.

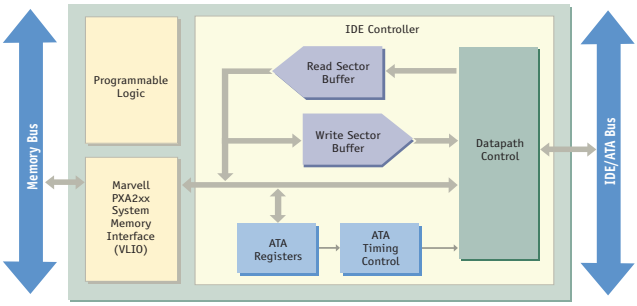
Figure 4: IDE Connectivity System Architecture



IDE Bridge Overview

The QuickLogic Companion Device with integrated IDE Controller implements connectivity for HDD or DVD ROM to the Marvell PXA2xx and PXA3xx processors, and consists of the following functional blocks as shown in **Figure 5**.

Figure 5: IDE Companion Device Block Diagram



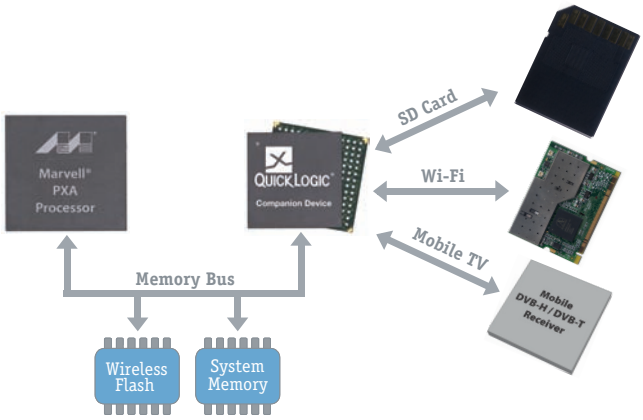
- **Programmable Logic:** This block provides designers with programmable logic to implement additional functionality. This can be used to integrate board level glue logic, consolidate various digital functions or implement custom functions.
- **PXA VLIO Interface:** The local bus interface, through use of the RDY signal, handles the PXA's Variable Latency Input and Output (VLIO) automatically. Use of the flow-through DMA feature results in reduced CPU overhead and more available bandwidth for transfers to the external HDD.
- **ATA Registers:** The ATA Registers block has several registers used for setting the controller mode, indicating the state machine status, and setting the PIO mode timings related to the chosen input clock frequency.
- **ATA Timing Control:** The ATA Timing Control is used to control any device supporting PIO modes 0 through 4. The PIO mode timing is determined from the PIO mode timing registers. All timing is based on the frequency of the input clock.
- **Sector Buffers:** The companion device includes two sector buffers, each of which can hold 512 bytes of information for read and write. The buffers can also be configured in bypass mode.
- **Datapath Control:** The datapath control module manages the ATA signal I/O pins and supports multi-word DMA (MWDMA) operation.

QuickLogic Companion Device with Integrated SDIO Controller

SDIO System Overview

Figure 6 illustrates the basic system block diagram that connects Wi-Fi, Mobile TV, or SD Card memory to the Marvell PXA2xx and PXA3xx processors using the QuickLogic Companion Device with integrated SDIO Controller. The processor serves as a host that configures and manages the system. The companion device provides a bridging solution from the embedded processor to SDIO memories and SDIO-based peripherals.

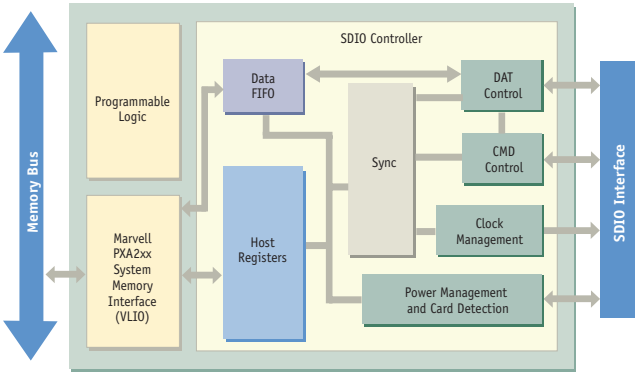
Figure 6: SDIO Connectivity System Architecture



SDIO Bridge Overview

The QuickLogic Companion Device with integrated SDIO Controller implements a Host Controller for Wi-Fi, Mobile TV, or SD Card memory connectivity, and consists of the following functional blocks as shown in **Figure 7**.

Figure 7: SDIO Companion Device Block Diagram



- **Programmable Logic:** This block provides designers with programmable logic to implement additional functionality. This can be used to integrate board level glue logic, consolidate various digital functions or implement custom functions.
- **Power Management and Card Detection:** The Power Management logic is designed for power saving purposes. It can turn SD bus power on or off by controlling the external power supply component.
- **PXA VLIO Interface:** The local bus interface, through use of the RDY signal, handles the PXA's Variable Latency Input and Output (VLIO) automatically.
- **Synchronization:** The Sync block is used to synchronize the signals across different clock domains.
- **Host Registers:** The Host Registers block consists of the standard SD/SDIO host register set, interrupt logic, and auto error reporting logic.

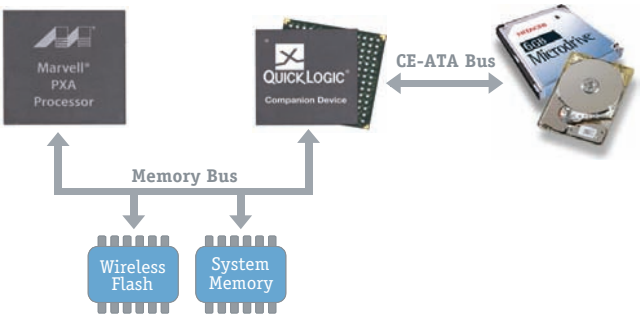
  The Host Controller provides a 32-bit interface and supports byte accesses to the host registers. If the system bus is 8 or 16 bits wide, the System Interface Logic can convert it to the appropriate width.
- **Data FIFO:** There are two asynchronous 512x8-bit Data FIFOs: TX_FIFO for buffering transmit data and RX_FIFO for receiving data.
- **CMD Control:** CMD Control is responsible for sending commands, receiving responses, and checking errors. It contains a state machine and the Command Line sub-module.
- **DAT Control:** DAT Control is responsible for transferring data between the Data FIFO and the SD data bus, and for detecting the SDIO interrupt.
- **Clock Management:** The Clock Management block is used to divide and enable/disable the SD clock. It consists of a Clock Divider and SD Clock Control Logic.

QuickLogic Companion Device with Integrated CE-ATA Controller

CE-ATA System Overview

Figure 8 illustrates the basic system block diagram that connects a CE-ATA hard drive to the Marvell PXA2xx and PXA3xx processors through the CE-ATA interface using the QuickLogic Companion Device with integrated CE-ATA Controller. The processor serves as a host that configures and manages the system. The companion device provides a bridging solution from the processor to high-capacity CE-ATA-based micro hard drives required by the ever-increasing demand for storage in applications such as MP3 players, PMPs and GPS systems.

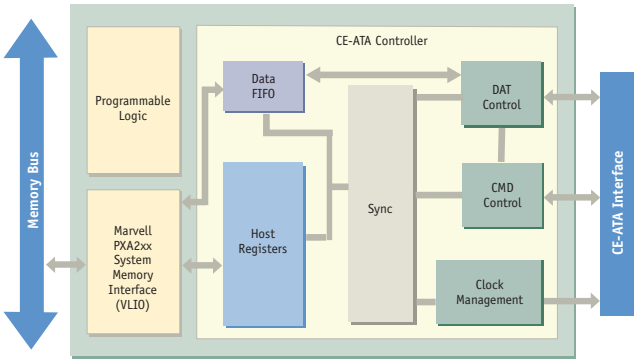
Figure 8: CE-ATA Connectivity System Architecture



CE-ATA Bridge Overview

The QuickLogic Companion Device with integrated CE-ATA Controller implements a Host Controller for CE-ATA hard drives through the CE-ATA interface targeting portable power sensitive applications. The companion device consists of the following functional blocks as shown in **Figure 9**.

Figure 9: CE-ATA Companion Device Block Diagram



- **Programmable Logic:** This block provides designers with programmable logic to implement additional functionality. This can be used to integrate board level glue logic, consolidate various digital functions or implement custom functions.
- **PXA VLIO Interface:** The local bus interface, through use of the RDY signal, handles the PXA's Variable Latency Input and Output (VLIO) automatically.
- **Synchronization:** The Sync block is used to synchronize the signals across different clock domains.
- **Host Registers:** The Host Registers block consists of the standard CE-ATA host register set, interrupt logic, and auto CMD12 logic.

  The Host Controller provides a 32-bit interface and supports byte accesses to the host registers. If the system bus is 8 or 16 bits wide, the System Interface Logic can convert it to the appropriate width.
- **Data FIFO:** There are two asynchronous 512x8-bit Data FIFOs: TX_FIFO for buffering transmit data and RX_FIFO for receiving data.
- **CMD Control:** CMD Control is responsible for sending commands, receiving responses, and checking errors. It contains a state machine and the Command Line sub-module.
- **DAT Control:** DAT Control is responsible for transferring data between the Data FIFO and the CE-ATA data bus, and for detecting the CE-ATA interrupt.
- **Clock Management:** The Clock Management block is used to divide and enable/disable the CE-ATA clock. It consists of a Clock Divider and CE-ATA Clock Control Logic.

Reference Platform

QuickLogic provides development platforms as daughter cards for PXA270 DVK. **Figure 10** shows the QuickLogic Mobile Applications Board that integrates with the PXA270 DVK to provide a platform for adding 10/100/1000 Ethernet, Wi-Fi, USB 2.0, Mobile TV, DVD-ROM, HDD, CE-ATA hard drive, and SD Card connectivities.

Figure 10: QuickLogic PolarPro™ Mobile Applications Board

Solutions Pack

The QuickLogic development package includes:

- Proven IP solutions
- Software drivers
- Reference design files such as Gerber files, reference schematics, etc.
- User guide and documentation
- QuickLogic development boards (daughter cards for PXA270 DVK)
- QuickLogic development software located at www.quicklogic.com/software
- Customer support and access to QuickLogic's *MyDesign* website

Solutions Support

For additional support and services:

- Design Services – www.quicklogic.com/mydesign
- E-mail – support@quicklogic.com
- Web portal – www.quicklogic.com/support

QuickLogic Contact Information

Phone	**QuickLogic US** (408) 990-4000
	QuickLogic Canada (905) 940-4149
	QuickLogic Europe Sales (Except Germany and Benelux) +(44) 1932-57-9011
	QuickLogic Germany/Benelux Sales +(49) 89-930-86-170
	QuickLogic Asia (Except Japan) +(86) 21-6867-0273
	QuickLogic Japan +(81) 45-470-5525
E-mail	info@quicklogic.com
Sales	www.quicklogic.com/sales
Support	www.quicklogic.com/support
Website	www.quicklogic.com

www.quicklogic.com

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