SuperH™ Companion Device for Wi-Fi Connectivity

Solution Highlights

Value Proposition

- Fast time-to-market
- Low power consumption
- Cost effective solution
- Customizable solution
- Ability to protect and leverage existing hardware/software

Processor

- Renesas SH7720 SuperH Reduced Instruction Set Computer (RISC) engine
- SH3-DSP processor core
- Low power dissipation
- Large cache
- Sophisticated peripherals
  - USB host/function
  - Color LCD controller
  - I2C
  - PCMCIA interface
- Optional – other SH processor cores

Companion Device

- Programmable low power bridge
- Seamless processor local bus interface
- Seamless Wi-Fi device interface
  - 32-bit/33 MHz Mini PCI
  - Host/Master/Target support
- Customizable/adaptable interface
  - To other processors
  - To other Wi-Fi devices

Applications

- Voice over IP phones
- Wireless POS terminals
- Surveillance systems
- Wireless access systems
- Printers
- Wireless handhelds and PDAs

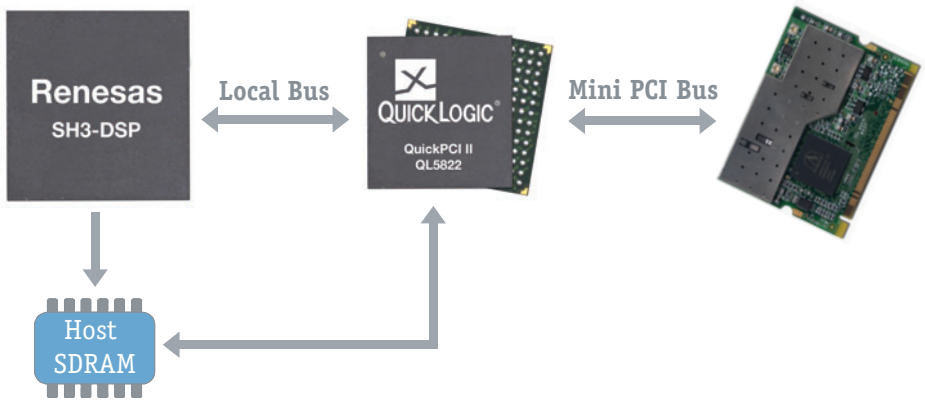
Introduction

Wireless technology is finding its way into a variety of applications once reserved for wired technologies. It is becoming increasingly more important as short and medium range wired connections are being replaced by radio links. Cellular networks have already revolutionized telephone systems, and soon wireless technologies will eliminate many of the wired Ethernet connections. As we move from a wired world to a wireless world, it becomes critical to leverage all the investments made in the wired world. Two such investments are the processor software and hardware development.

System Overview

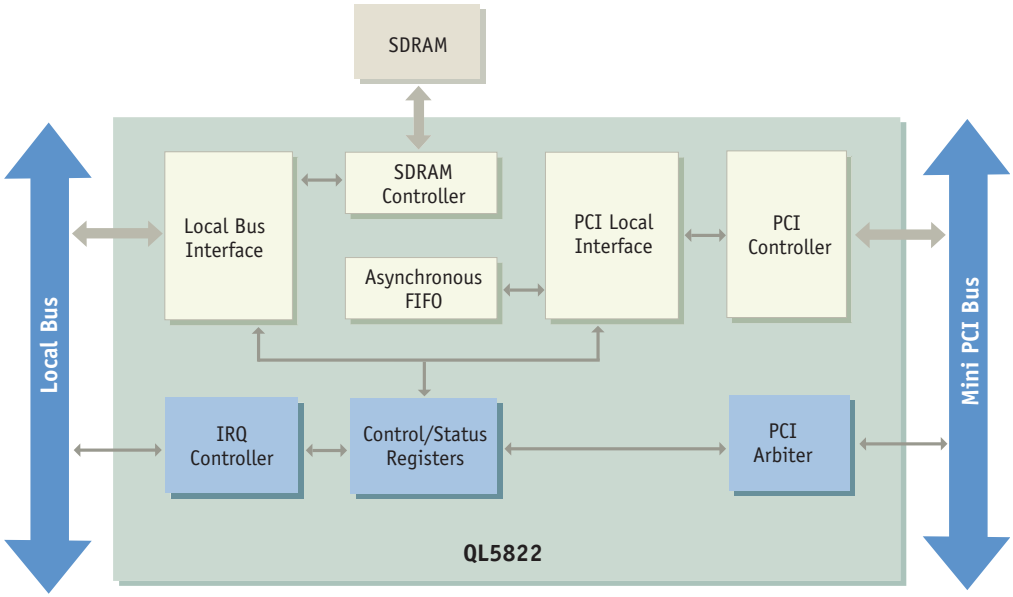
Figure 1 illustrates the basic system block diagram. The SH7720 processor data is streamed to and from the 802.11b/g chipset module through the local-to-PCI bus bridge implemented on the QuickLogic QuickPCI® device (QL5822).

Figure 1: System Architecture



The SH3 companion device implements a bridge between the SH7720 processor and the PCI bus. The bridge provides a communication link between the SH7720 processor and the 802.11b/g chipset. Data is transmitted in both directions between the SH7720 processor and the 802.11b/g chipset. The SH7720 local bus and the 802.11b/g chipset Mini PCI interface are connected using the QL5822 in a 196-pin ball grid array. The application described here uses a 802.11b/g chipset from the Conexant® Prism family. The programmable architecture of the bridge device makes it easy to adapt the design for different Wi-Fi chipsets and applications.

Figure 2: Companion Device Block Diagram



Processor Overview

The SH7720 is part of the Renesas 32-bit RISC Microcomputer SuperH RISC Engine family of processors. It includes the SH3-DSP CPU as its core and integrates a set of sophisticated peripheral functions.

- CPU Core: SH3-DSP core, 133 MHz (173 MIPS) @ 1.5 V
- Cache: 32 KB cache memory, 16 KB internal memory
- Peripherals: USB host and function, color LCD controller, I2C, PCMCIA, DMA, IrDA and others
- Low Power: ~2.0 mA/MHz (typical)
- Package: BGA 256 (17 mm^2 or 11 mm^2)

Bridge Overview

The SH3 companion device is a low power seamless bridge from the SH7720 processor to a standard Mini PCI 802.11a/b/g Wi-Fi module. It is implemented in the QuickPCI QL5822 device. The design consists of the following blocks (or modules) as shown in **Figure 2**:

- **PCI Core:** A 32-bit/33-MHz Host/Master/Target that interfaces between the PCI local interface block and the PCI bus that is connected to the 802.11b/g chipset. See www.quicklogic.com/PCI for detailed information on QuickLogic PCI products.
- **Local Bus Interface:** Communicates with the SH7720 local bus and is responsible for steering data and control transactions to/from the Control/Status Registers and the PCI Bus Interface.
- **PCI Arbiter:** Responsible for managing the PCI bus mastership between the 802.11b/g chipset and PCI Controller.
- **PCI Bus Interface:** Communicates with the PCI Controller. The Local Bus Interface block communicates with the PCI Bus Interface to perform the desired transaction on the PCI bus. The PCI Bus Interface is also responsible for providing the WLAN chip access to the asynchronous FIFO.
- **SDRAM Controller:** Provides the interface between the asynchronous FIFO and SDRAM device for data transfer between the WLAN and SDRAM.
- **Asynchronous FIFO:** Provides four temporary locations of 32-bit word storage for burst transactions between the WLAN and SDRAM.
- **Interrupt Controller:** Accessible from Local Bus Interface block, it alerts the SH3 processor when any one of the flags has been set in the interrupt register of the control status registers.
- **Control/Status Registers:** Accessible from the Local Bus Interface block, reports the status of various control flags.

Wi-Fi Overview

There are a variety of Wi-Fi vendors to choose from and interface with. Most will have a standard Mini PCI or CardBus interface. Some of the more popular vendors are:

- Atheros®
- BroadCom®
- Conexant®

Development Platform

Figure 3 shows the VoIP reference platform available from Renesas (part no. RTS7720IPP-DS3).

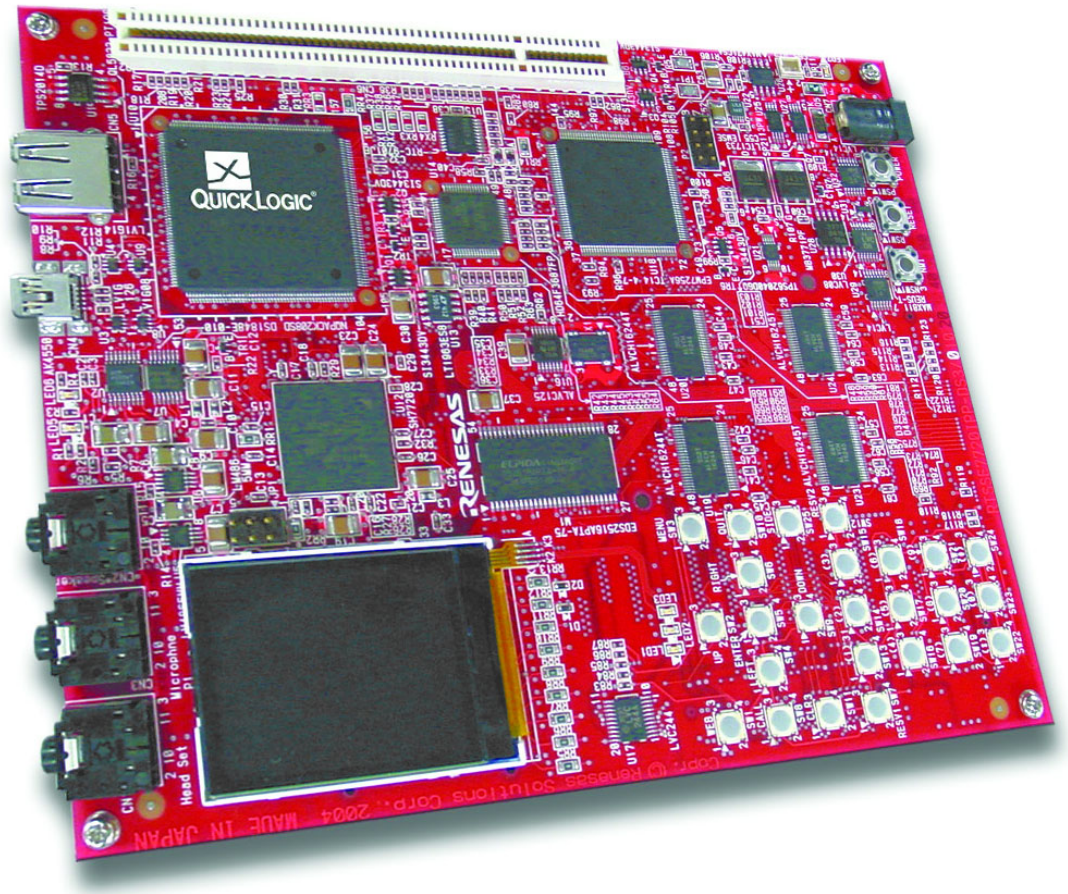
Solutions Support

For specific solution information on:

- QL5822 reference design files
- QL5822 volume pricing
- RTS7720IPP-DS3 reference platform
- Software drivers
- QuickLogic development tools
- Design services

E-mail wifi@quicklogic.com.

Figure 3: Renesas SuperH Wi-Fi IP Phone Reference Design



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Printed in USA

QL-SH-SB-3