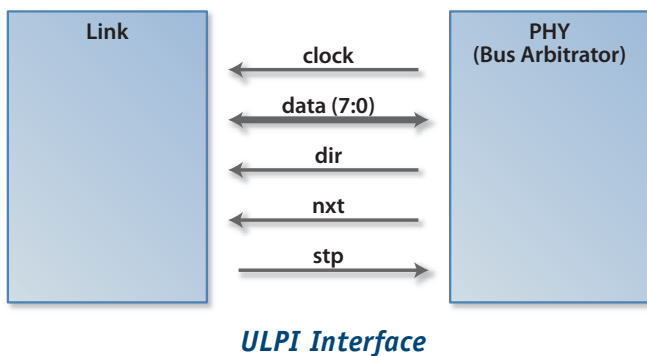


QuickLogic's PHY-less ULPI Chip-to-Chip Connectivity Solution

INTRODUCTION

The Universal Serial Bus (USB) interface has become the industry standard in the world of computing and consumer electronics. This stems from the PC industry's desire to replace legacy serial and parallel interfaces with 'plug & play', making it extremely easy to connect peripheral devices to a computer. More recently, USB has been widely adopted by mobile devices as the high-speed interface used for multimedia, data transfer and synchronization. The latest USB2.0 standard supports Hi-Speed with up to 480Mbps/sec throughput. The On-the-Go (OTG) capability allows two devices to connect to each other without the use of a computer.

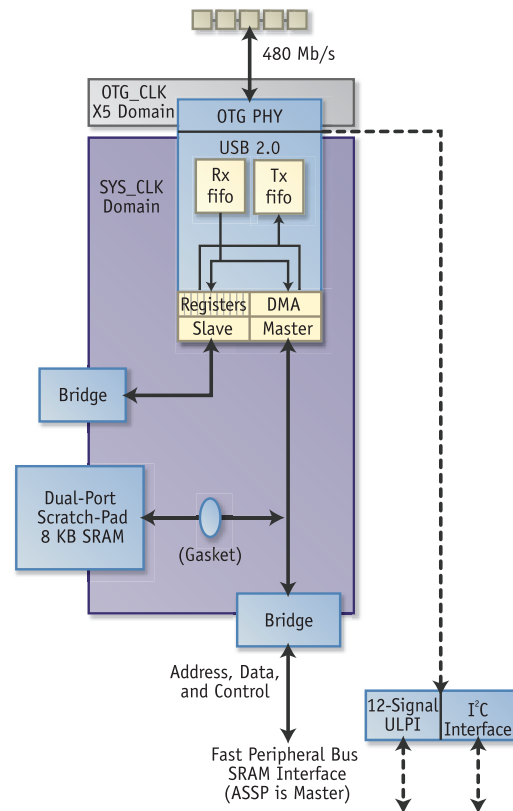
The traditional interface between the USB link layer and USB Transceiver Macrocell (PHY) is UTMI/UTMI+, which requires 54+ pins. The latest ULPI specification significantly reduces the interface to only 8 or 12 signals, driving down system cost, routing complexity and board space.



PHY-LESS ULPI INTERCONNECT

QuickLogic's ArcticLink™ Solution Platform combines Hi-Speed USB 2.0 OTG, SDIO and CE-ATA Host Controllers with an embedded ultra-low-power programmable fabric, all in a single-chip solution. It is a highly integrated and flexible platform designed to solve connectivity challenges for the mobile device market.

The USB block supports Hi-Speed USB2.0 OTG with built-in PHY. The 12-signal ULPI interface from the USB controller is routed internally to the programmable I/Os for external connections.

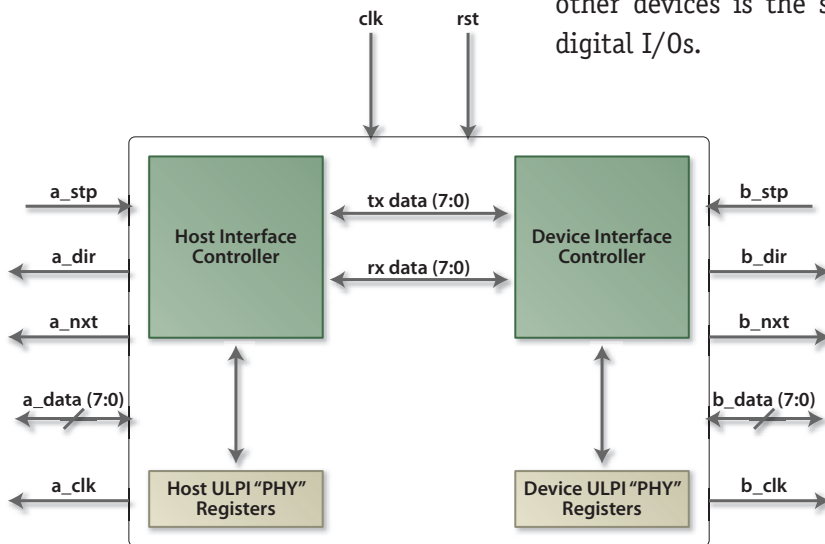


Hi-Speed USB2.0 OTG Block Diagram

QuickLogic's Solution Guide for Phy-less ULPI

As USB becomes more ubiquitous, system designers have also adopted it for chip-to-chip interconnect. Traditionally, for two chips to communicate with each other, each would require a PHY - one for the Host port and the other for the Device port. A PHY contains digital processing logic and an analog transceiver. Running at high-speed, it consumes well over 50mA power. The requirement to have PHYs on both sides of the connections leads to higher cost, space and most importantly power consumption, which is a big concern for these power sensitive mobile devices.

QuickLogic's ArcticLink provides the unique capability of implementing a pair of "pseudo" PHYs in the programmable fabric. This PHY-less ULPI block acts as a bridge to communicate between a ULPI Host link and a ULPI Device link at high-speed without the high power transceivers. The PHY-less ULPI emulates actual PHY functionality, which includes: ULPI PHY register read and write accesses, RXCMD, and TXCMD without actually having to go through D+/D- on the USB wires, making this block ideal for chip-to-chip interconnect in a mobile device. The interface to other devices is the standard ULPI protocol using 3.3V digital I/Os.



QuickLogic "pseudo" PHY Block Diagram

PHY-LESS ULPI KEY FEATURES

- Supports ULPI specification with 12-signal interface through ArcticLink's programmable fabric
- Complete logic implementation to minimize power consumption
- Supports USB data at High Speed (480Mbits/sec), Full Speed (12Mbits/sec) and Low Speed (1.5Mbits/sec)
- Supports USB PHY register set for settings and status information
- OTG specific handshake such as SRP and HNP are not supported



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