

Reliability of the Amorphous Silicon Antifuse



••••• QuickLogic® White Paper

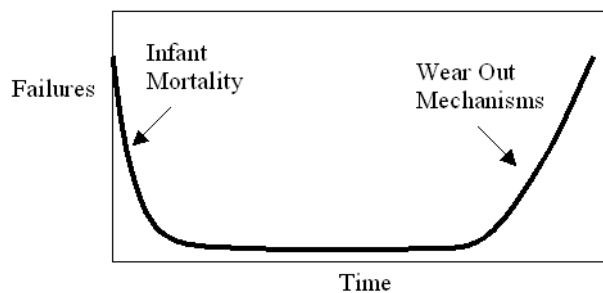
Abstract

Development processes at QuickLogic control the reliability of the QuickLogic ViaLink® antifuse. ViaLink reliability is built into the silicon at every step, beginning with design rules and device characterization. But unlike other fab processes, the reliability work continues with the layout rules, test methodology, place and route software, ViaLink programming sequence, programming algorithm, qualification plans, and quality assurance process. All these factors come together to create the reliable QuickLogic ViaLink.

Introduction

Semiconductor reliability has been studied and characterized [1]. The initial failure rate, also called infant mortality, is high due to defects. The midterm life of a semiconductor component has a low failure rate. Most of the defects have already failed, and the wear out failure for mechanisms has not started. At the end of the semiconductor component life, many elements of the semiconductor begin to wear out. Physical changes to the metals, semiconductor, and dielectrics cause the component to no longer meet the original specification. These failures are predictable and increase with time. This high-low-high failure rate is known as the bathtub curve and is shown in **Figure 1**.

Figure 1: Bathtub curve for semiconductor failure rate.



Semiconductor manufacturers have reduced the infant mortality by decreasing the number of defects and screening for the remaining defects. Defects have been reduced with improved and automated wafer handling, improved equipment and improved processes. Automatic inspections have been added during wafer fabrication for the purpose of detecting wafers with defects. Wafers that cannot be reworked are scrapped. After fabrication, wafers are tested for correct electrical parameters. Any wafers failing this test are rejected. All passing wafers then have the individual die tested for functionality and for electrical parameters. Defective die are marked for scrap. In addition, good die on unusually low yielding wafers are also scrapped. Yield improvement teams are continuously determining and correcting the reason for the low yield. Defect reduction is a major goal in wafer fabrication.

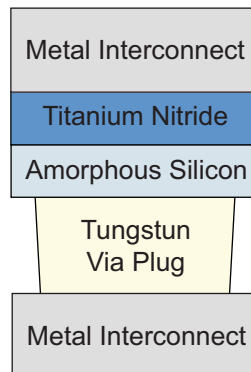
The wear out failures cannot be avoided or screened. They are due to the physics of the materials, the voltages and the currents applied. However, they can be studied and understood so that the materials, voltages and currents can be modified to ensure that the wear out failures occur beyond the lifetime of the semiconductor component. Wear mechanisms such as electromigration, hot carrier injection and dielectric breakdown are well characterized. Metals, semiconductor junctions and dielectrics have been modified to improve the lifetimes due to these and many other failure mechanisms.

Thus, with tests in place to screen for infant mortality, and with the improved material and transistor quality, modern semiconductor component failure rates remain in the center region of the bathtub curve. QuickLogic's semiconductor components also include the ViaLink. As shown in the following sections, the infant mortality and wear out mechanisms of the ViaLink have been studied, and test screens, materials, and rules are in place to ensure that the ViaLink also operates in the center region of the bathtub curve.

QuickLogic ViaLink Structure

A ViaLink is two electrodes separated by a dielectric. The QuickLogic ViaLink uses undoped amorphous silicon as the ViaLink dielectric. The structure of the ViaLink is shown in **Figure 2**.

Figure 2: QuickLogic ViaLink structure.



The amorphous silicon is deposited on top of a planarized tungsten via plug. For areas where regular vias are to be created, the amorphous silicon is removed. The top layer metal is deposited with a barrier metal in contact with the amorphous silicon. The top metal and amorphous silicon are then patterned at the same time. This structure is easily integrated into a standard foundry process. There are only two additional processing steps, the amorphous silicon deposition and the removal of amorphous silicon in unwanted areas.

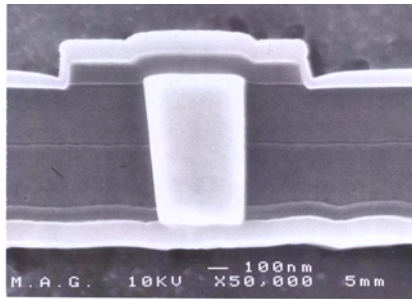
The ViaLink has two states:

- Unprogrammed — low leakage (very high resistance)
- Programmed — low resistance connection

Unprogrammed ViaLink Reliability

The typical unprogrammed ViaLink (see **Figure 3**) has a leakage current of less than 1 nA with the nominal supply voltage V_{cc} applied. This leakage has been fully characterized [2]. During a voltage stress, the leakage current increases with time and then saturates, remaining constant with further stress. Characterization, process control and process monitors ensure that the increase in leakage through the unprogrammed ViaLinks will remain below the data sheet limit for the lifetime of the device.

Figure 3: Unprogrammed ViaLink



The ViaLink does not exhibit the time-dependent dielectric breakdown as observed by other dielectrics such as the SiO_2 gate oxide. The ViaLink's leakage mechanism is not catastrophic at the voltage levels seen in use.

Programmed ViaLink Characteristics

The programmed ViaLink (see **Figure 4**) resistance is a function of the programming current, programming algorithm and material properties of the ViaLink. QuickLogic controls these properties so that the programmed ViaLink is a stable, reliable, linear resistor.

Figure 4: Programmed ViaLink

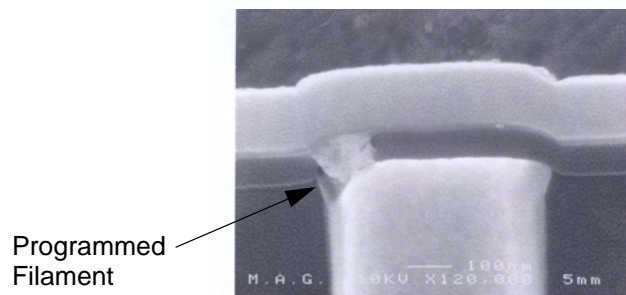
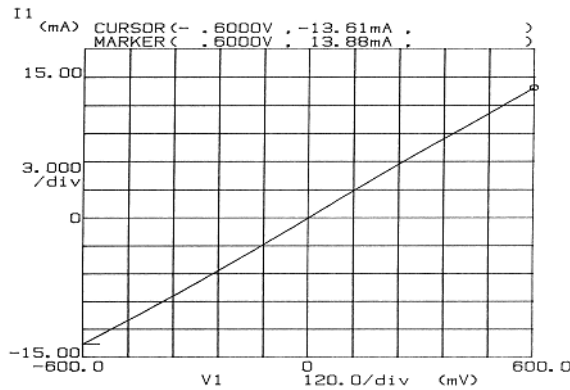


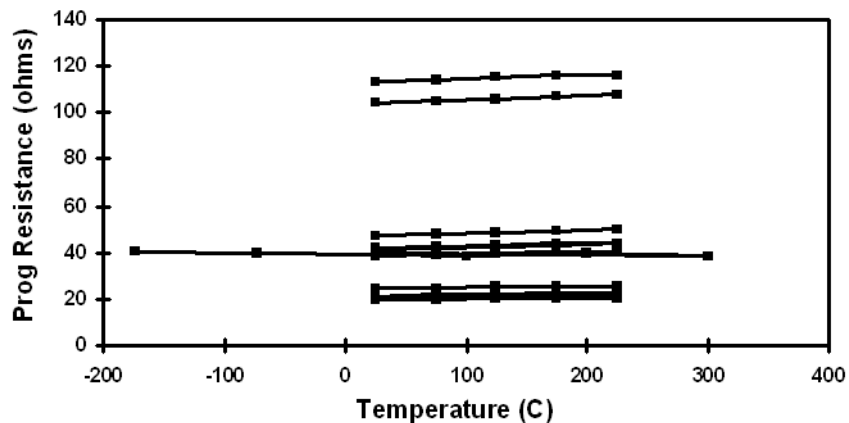
Figure 5 shows the IV characteristics of a ViaLink programmed with 15 mA of programming current. The programmed ViaLink clearly behaves as a linear resistor.

Figure 5: IV characteristic of a ViaLink programmed with 15 mA.



In an attempt to characterize temperature dependence, several ViaLinks were programmed with various resistances. The resistances of the ViaLinks were then measured from 20°C to 225°C (with one tested from -180°C to 300°C). Figure 6 shows that the programmed ViaLink resistance does not exhibit a significant temperature dependence.

Figure 6: The resistance of various programmed ViaLink over temperature.



Programmed ViaLink Reliability

The programmed QuickLogic ViaLink must remain in its low resistance state during the lifetime of the component. The reliability of the low resistance programmed ViaLink has been fully characterized [5]. To determine the characteristics of a programmed ViaLink taken to failure, bench studies were performed with high DC current. Once the programmed ViaLink has failed, it is no longer stable [6]. Figure 7 shows that the

damaged programmed state has a nonlinear IV characteristic as well. **Figure 8** shows that the damaged programmed state is not stable during a high temperature bake, while the undamaged programmed ViaLink does not change during an 18-hour 300°C bake.

Figure 7: The IV characteristics of a damaged programmed ViaLink.

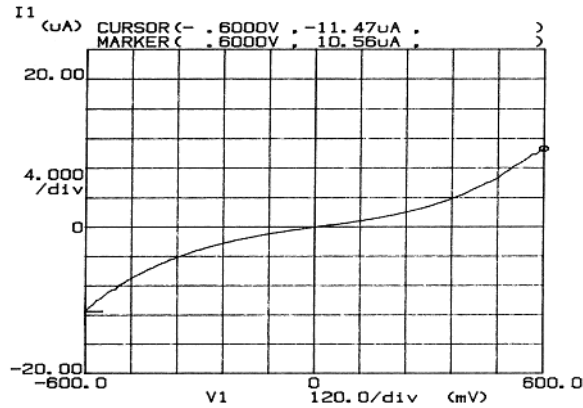
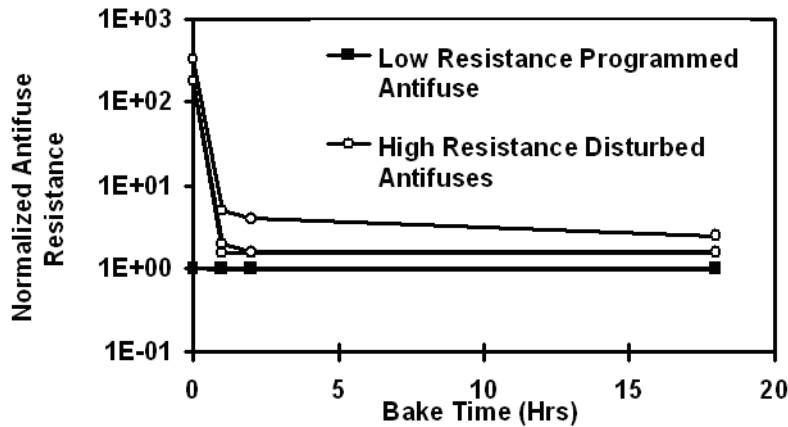


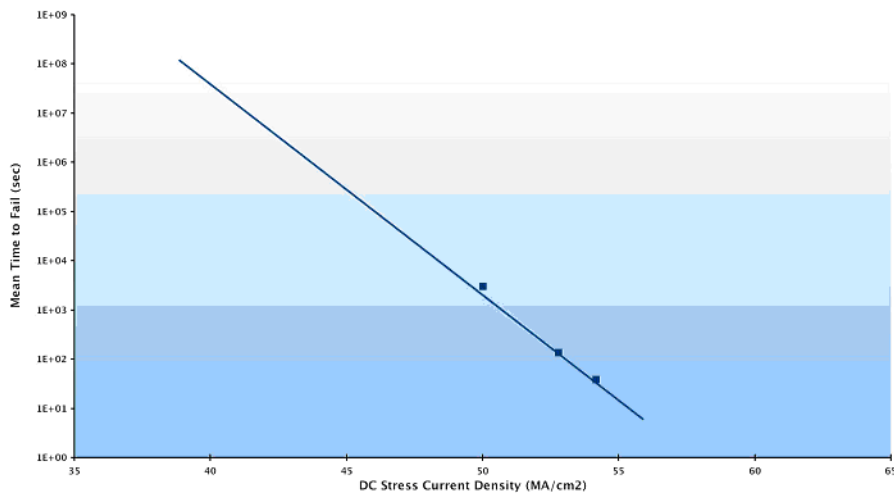
Figure 8: Programmed ViaLink resistance during a 300°C bake. The resistance is normalized to its initial programmed resistance.



The damaged programmed ViaLink is unstable and unreliable. The resistance is nonlinear and can vary from a 100 ohms to 10,000 ohms. This resistance variation may be satisfactory where a programmed ViaLink is used to tie a gate low or high, and no significant current goes through the ViaLink. However, the damaged programmed ViaLink should never be used in a path where the resistance variation can affect the performance of the component. In cases where the damaged programmed ViaLink is in the speed path, the delay may change from nanoseconds to microseconds, due to the variations in the ViaLink resistance.

Excessive DC current through the antifuse is the typical cause of damage. **Figure 9** shows the mean time to failure for programmed antifuses as a function of DC current density, i.e., the actual current divided by the cross sectional area of the antifuse’s conducting pathway. The cross sectional area of the pathway is a function of the programming current and programming algorithm along with the height, width and polarity of the programming pulses.

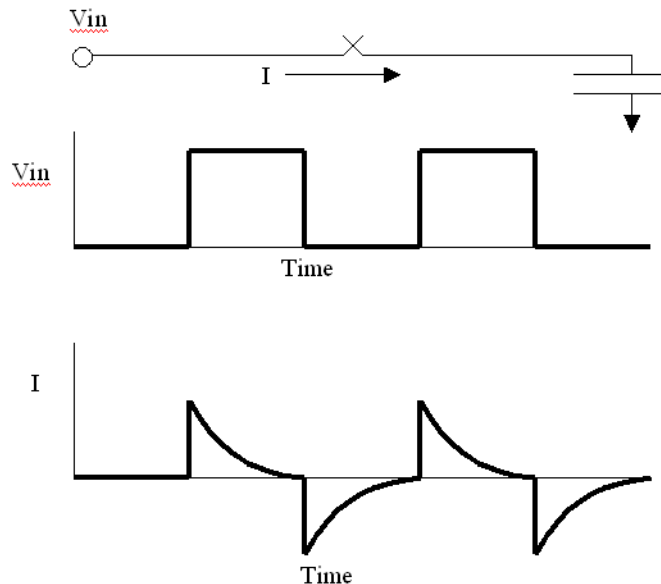
Figure 9: The accelerated mean time to failure for a programmed ViaLink stress with a constant DC current.



The DC data for the programmed ViaLink is useful for showing the strong acceleration of the programmed ViaLink failures by increasing the current density through the programmed filament. This strong dependence also means that reducing the operating current can significantly increase the lifetime of the programmed ViaLink.

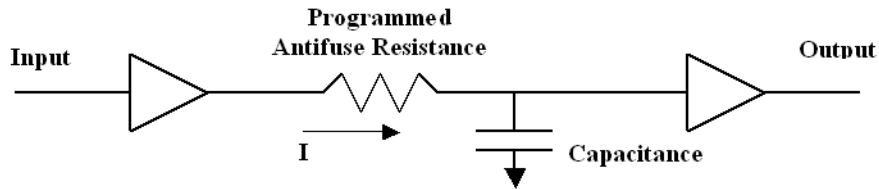
The actual use of a programmed ViaLink is to connect a CMOS driver circuit to a capacitive network. In this case, the programmed ViaLink is subjected only to an AC capacitive current, where the current flows quickly when the driver is turned on and then drops as the capacitor discharges. **Figure 10** shows the application of the ViaLink, the voltage of the CMOS driver and the resulting IV characteristics.

Figure 10: The current through a programmed ViaLink is caused by the charging and discharging of an RC network.



A test chip with a CMOS inverter driving a capacitive load through a programmed ViaLink was built to characterize the programmed ViaLink stress with an AC capacitive current. The CMOS inverter and the capacitance were identical to that used in a typical QuickLogic product. The peak current through the programmed ViaLink is determined by the CMOS inverter, the ViaLink resistance, downstream capacitance and the frequency. See **Figure 11**.

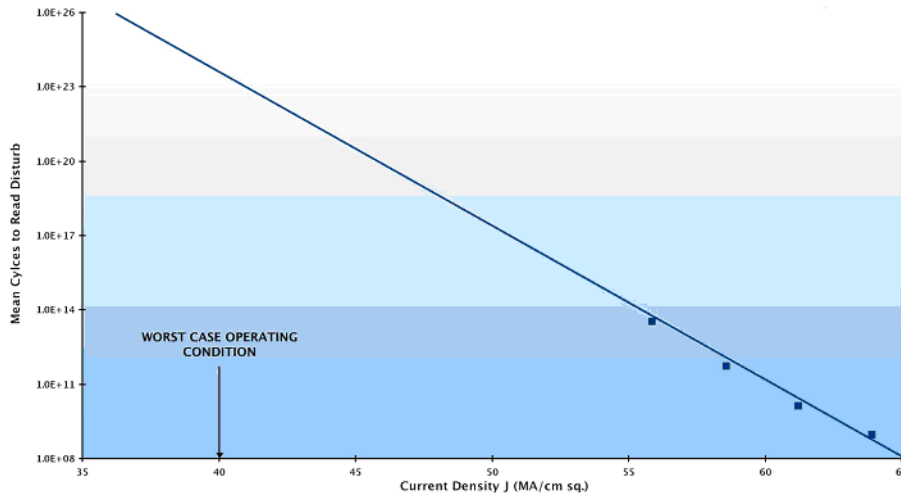
Figure 11: Schematic of the test circuit used to stress the programmed ViaLink.



The input to the CMOS inverter was toggled and the output delay was monitored. Any change in the programmed ViaLink resistance will change the RC time constant and therefore the delay through the circuit. Any cycle where the circuit delay increases above the measurement error is considered a ViaLink failure.

Figure 12 shows the mean cycles to failures for the programmed ViaLink as a function of the peak AC current density through the ViaLink. To accurately control the current through the programmed ViaLink, the downstream capacitance was kept large and the frequency was kept low so that the capacitor would fully charge and discharge during each cycle. The peak AC current in this case was limited to the maximum drive strength of the CMOS circuit. The drive strength was controlled by varying the supply voltage and by changing the size of the CMOS inverter. The simulated peak AC current was within 5% of the measured DC drive of the CMOS inverter.

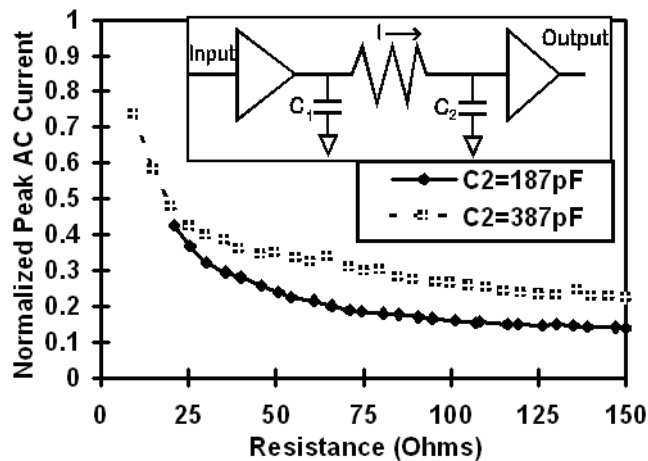
Figure 12: Accelerated mean cycles to failure for the programmed ViaLink as a function of the peak AC current density.



The peak AC current density accelerates the programmed ViaLink failure mechanism significantly. This characteristic is incorporated into the electrical design rules that govern the use of ViaLinks in QuickLogic components. QuickLogic design engineers only use the ViaLink in circuits where the peak AC current density is low, which guarantees a reliable programmed ViaLink.

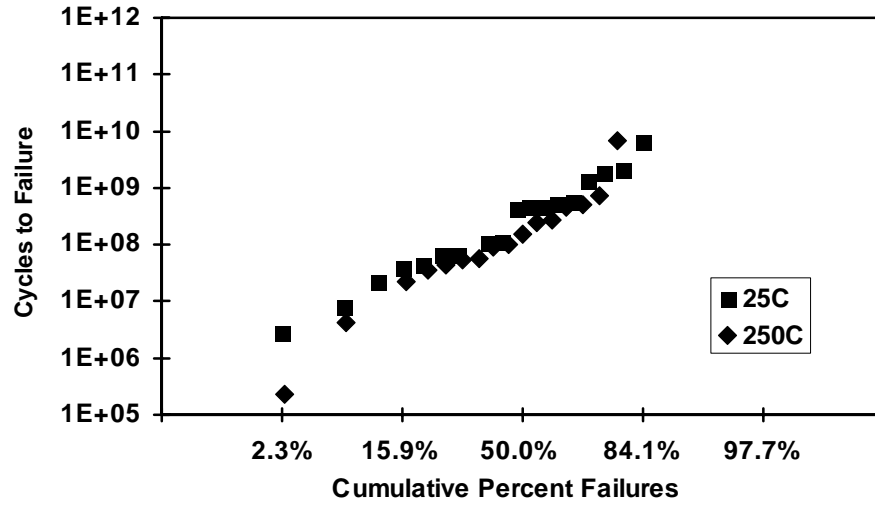
To determine the ambient temperature acceleration of the programmed ViaLink failure mechanism, a second AC test circuit was built where the CMOS driver and output buffer were separated from the ViaLink. This allowed the ViaLink temperature to be varied without changing the temperature or characteristics of the CMOS circuitry. The parasitic capacitances of connecting the CMOS driver and CMOS output driver to the ViaLink were significant. However, the peak AC current across this structure could be calculated by measuring the voltage across the ViaLink. **Figure 13** shows the peak AC current as a function of the ViaLink resistance for two different downstream capacitances.

Figure 13: Peak AC current through a programmed ViaLink. The AC current is normalized to the maximum DC drive of the CMOS inverter. The parasitic capacitance C_1 is 65 pf.



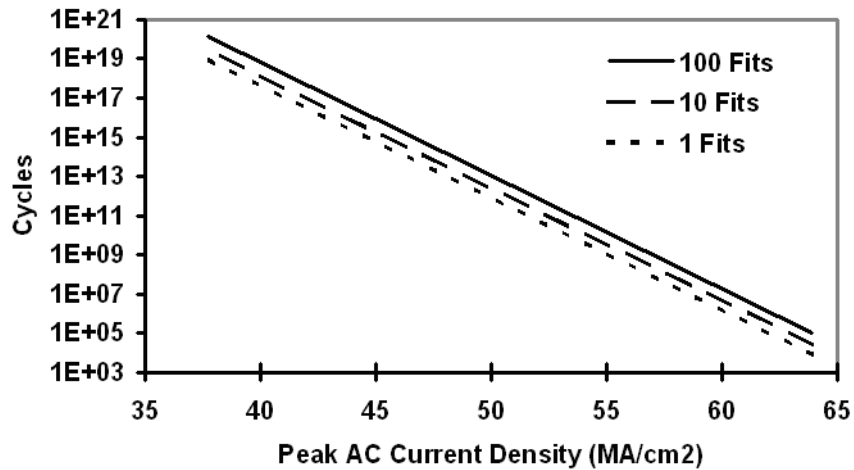
For the ambient temperature dependence of characterization, the ViaLinks were programmed to approximately the same resistance. Since the ViaLink resistance is constant with temperature, the AC stress current is the same at different temperatures. **Figure 14** shows that the distributions of cycles to failure for programmed ViaLinks stressed at 25°C and 250°C are similar. The lack of an ambient temperature dependence is most likely due to a high self-heating of the conducting filament in the programmed ViaLink, which makes the change in ambient temperature negligible.

Figure 14: Cumulative cycles to fail at 25°C and 250°C.



Only a small percentage of the total programmed ViaLinks within a QuickLogic component are stressed at the worst-case condition. For the worst case to occur, the programming current must be low and the downstream capacitance must be high. Figure 15 shows calculated FIT for a product with 2000 ViaLinks operating at the worst-case current density. Any failure in one of these worst-case ViaLinks is considered a component failure. For the QuickLogic design at 40 MA/cm², a component will experience 1 FIT after 10¹⁷ cycles, which is equivalent to a part running at 250 MHz for over 10 years. The QuickLogic reliability design rules account for the largest number of worst-case ViaLinks in any product.

Figure 15: Calculated FIT for a part with 2000 worst-case ViaLinks.



The QuickLogic Approach to ViaLink Reliability

ViaLink reliability is the combination of many factors. The QuickLogic development and manufacturing processes ensure that the ViaLinks are reliable. The fab process, electrical design rules, layout design rules, test development, design routing, ViaLink sequencing, programming methodology, qualification plans and quality assurance procedures work together to create the reliable ViaLink.

Fab Process

QuickLogic has installed the amorphous silicon ViaLink process in more than six different fabs since the 1990. The ViaLink process at each fab has been brought up with excellent yield and reliability. To add the amorphous silicon ViaLink to an existing fab process, two steps are added and one step modified.

The modified step is the planarization of the tungsten via plug. Although this is generally a standard manufacturing step, the ViaLink requires a more planar surface. QuickLogic engineers have developed an improved CMP process that results in ViaLinks with tight electrical parameters.

The additional steps are the amorphous silicon deposition and the amorphous silicon patterning. The process has been characterized so that the power and chemistry during the deposition produces an amorphous silicon film with minimal leakage currents. Several factors influence the electrical properties of the film. The film thickness directly relates to the programming voltage, but is not the only factor. The interfaces between the amorphous silicon and the metal electrodes, the topology, and the deposited film thickness all determine the voltage and current characteristics of the ViaLink. These variations must be monitored and controlled. In addition, the design of the programming circuitry must also take the variations in account.

The second addition step is a noncritical masking step where the amorphous silicon is removed from the areas where standard vias are to be created. This is a standard mask and silicon etch.

The ViaLink fab process has been developed by QuickLogic engineers to be simple and easily controlled, so that it can be installed into any fab with reproducible results.

Design

Design rules ensure that the unprogrammed and programmed ViaLink will be reliable.

To prevent inadvertent programming of ViaLinks during normal operation, no ViaLink can be directly connected to any external signal or power bus. Noise on external signal or transients on the power and ground buses can program a ViaLink by creating high voltage across an unprogrammed ViaLink.

To ensure that there are no failures of programmed ViaLinks, the programming path and operating currents are carefully simulated. The reliability design rule for a programmed ViaLink can be stated as a maximum allowed ratio of the worst-case peak AC operating current through a programming ViaLink, and the programming current of that ViaLink.

$$\text{Programmed ViaLink Reliability ratio} = \frac{\text{Worst case peak AC current}}{\text{Programming current}}$$

The series resistance of the programming path determines the programming current during programming. Every programming path in the design is simulated to determine its programming current. To ensure proper control of the reliability ratio, QuickLogic designs the circuits such that the operating current is limited.

QuickLogic designs its programming transistors so that they are not degraded during programming. Any degradation in the programming transistors would reduce the programming current. Design rules limit the drain to source voltage when the transistor is “on” to prevent hot electron degradation and snapback. Both of these effects can damage a programming transistor. A damaged programming transistor may still supply the voltage to program a ViaLink, but the programming current may be limited. This would create a lower reliability ViaLink. As mentioned later in this paper, the programming current is monitored and if it is too low for a ViaLink, the component is rejected.

Layout

The QuickLogic ViaLink uses layout techniques to increase the uniformity of the via plug planarization. The planarization process results are better if the density of the ViaLinks is constant. As discussed previously, this results in improved electrical characteristics.

After the amorphous silicon is patterned, the top electrode is patterned and etched. This creates a step on the surface of the wafer. The subsequent barrier metal may be thin over these steps creating a poor barrier for amorphous silicon diffusion. As a result, silicon may penetrate the barrier and cause premature programming. Layout techniques ensure that these areas are eliminated from the design by prohibiting their layout, or by ensuring that these areas are removed during subsequent processing.

QuickLogic runs automated design rule checks to verify that all layout rules have been followed.

Test

QuickLogic screens 100% of the unprogrammed ViaLinks at the wafer level to ensure they meet a minimum voltage requirement. This ensures that the all the ViaLinks will not program below a certain voltage, and that they will remain in their high resistance unprogrammed state. A similar check at final test ensures that the unprogrammed ViaLinks were not damaged during packaging. A final check is done on the programmer prior to programming to ensure that the ViaLinks were not damaged after test.

The unit is rejected if any ViaLink fails these tests. Reject limits and maverick lot limits are set so that if any lot has a high reject rate, engineers are notified. If the failure rate for this test exceeds the maverick limit, the entire lot is rejected and engineering is notified. A failure rate above the maverick limit indicates that the lot exceeds the expected failure distribution and should not be shipped to customers.

QuickLogic also does verification of the programming circuitry. At wafer level and final test the programming circuitry is verified that it can pass the proper voltages and currents. The unit is rejected if any programming path fails either test. Again reject and maverick limits apply to these tests.

Design Routing

Customer designs are placed and routed into the part by the QuickLogic development software. The routing software creates the routing networks that determine the effective downstream capacitance for each programmed ViaLink. If the downstream capacitance can be lowered below a certain value, the capacitance would limit the peak AC current through the programmed ViaLink to less than the CMOS drive strength. The router software can reduce the number of ViaLinks operating at high currents by limiting the downstream capacitance. The router can select less capacitive wire lengths for different speed applications, or buffer large networks to create smaller less capacitive networks. This routing methodology lowers the number of ViaLink operating at the high currents and increases the reliability of the programmed part.

ViaLink Sequencing

Another tool in the QuickLogic software is the sequencer, which determines the order in which the ViaLinks are programmed.

The sequencer software tool prevents unprogrammed ViaLinks from being biased inadvertently with a high DC voltage. As nets are being formed during programming, large networks and their associated programming paths can cause an unprogrammed ViaLink to become biased via so-called sneak paths. The ViaLink can become programmed or damaged, creating a yield or even a reliability problem. The sequencer software avoids sneak paths and finds an alternate sequence.

Another inadvertent programming condition occurs during programming related to the capacitance of large networks. When a programming pulse is applied to one network, there may be a ViaLink crossing over to another high capacitive network, which may then program. The sequencer software avoids these conditions and finds an alternate sequence.

Similarly, the sequencer also determines the effective downstream capacitance for every programmed ViaLink. If the downstream capacitance is small enough to limit the peak AC operating current below the drive strength of the CMOS inverter, the programming algorithm can be modified to save programming time. The minimum programming requirements are calculated for each antifuse to be programmed.

ViaLink Programming

QuickLogic measures the programming current as each ViaLink is programmed. If the programming current is less than the minimum required by the reliability ratio, the part fails programming. The programming current is measured again at a lower voltage to ensure that the IV characteristics of the programmed ViaLink meets specifications. Although the part may function properly when one of the measured currents is outside the specification limits, the part may not be reliable, and is thus classified as a reject.

Qualification Plans

QuickLogic uses an industry standard qualification test to verify the reliability of final product. To address the reliability of the unprogrammed ViaLink, High Temperature Operation Life (HTOL) stresses all the unprogrammed ViaLinks in a part with a high voltage and at a high temperature. The total ViaLink leakage current will contribute to the standby current of the part. Therefore, the standby current is carefully checked on each part after 168 hours, 500 hours and 1000 hours of this life test.

Since the programmed ViaLink failure mode is not affected by ambient temperature and is accelerated by high current, the worst-case life test is at low temperatures. The low temperature increases the electron mobility, increasing the current drive capability of the CMOS inverters. QuickLogic performs the Low Temperature Operating Life (LTOL) test at -55°C and at a high voltage.

QuickLogic performs qualification tests for new products and when required because of changes in the fab, design, layout, test, router software, sequencer software, and programming algorithm. The qualification procedures are outlined in QuickLogic qualification specifications.

Quality Assurance

After product development, qualification, and product release the work to ensure quality is not done. During the lifetime of the product many tests are repeated on a regular basis. The results are added to the reliability report and the FIT rates are updated.

Conclusion

The reliability of the QuickLogic ViaLink is a combination of many factors. Maintaining this reliability is a team effort among many groups within the company. The needed knowledge is embedded in the process flow, design rules, product qualification and software tools. As a result, the customer does not need to have a thorough knowledge of the ViaLink to realize a reliable design. As long as the electrical limits in the data sheet are met, the QuickLogic component will be reliable (see the *QuickLogic Reliability Report* for current FIT rates [6]).

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Revision	Date	Originator and Comments
A	June 2008	First release.

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