Clock Networks in the ArcticLink® Solution Platform

QuickLogic® Application Note 92

Introduction

The ability to provide robust clocking to various logic elements in a device is critical. Poor clock networks are inflexible, prone to high skew, contain long path delays, and limit the clock loads that can be placed on the network. These issues can prevent the implementation of complex designs. In addition, performance can be severely hindered by clock skew and poor routing. The QuickLogic ArcticLink solution platform addresses these problems by providing efficient clock routing throughout the chip.

This application note discusses the routing structure of the clock networks, the logic blocks and ASSP ports that each clock network can drive, and the use and advantages of each clock network.

Fabric Clock Network Overview

The QuickLogic ArcticLink solution platform contains a programmable fabric block and dedicated ASSP region within a single package. There is one dedicated 12 MHz USB clock input on the ASSP as well as three clock input pads located on the top, right, and bottom of the device as shown in **Figure 1**. In addition, two clock input ports are provided on the Fabric-ASSP interface to route clock signals into the ASSP region. See **ASSP Clock Input Ports** on page 9 for more information about this interface. The Fabric clock networks consist of a two-level H-tree network as shown in **Figure 2**. The first level of each clock tree spans from the clock pad through the center of the fabric, and to the center of each quadrant. The second level spans from the center of the quadrant to everywhere inside that quadrant. This architecture allows for two different clock networks: global and quad-net.

Figure 1: Clock Pad and Configurable Clock Manager Order

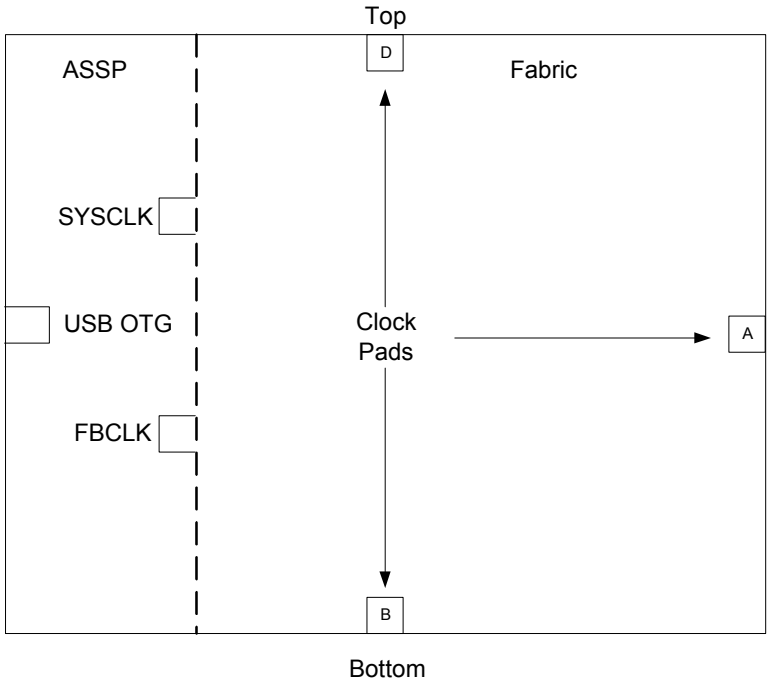
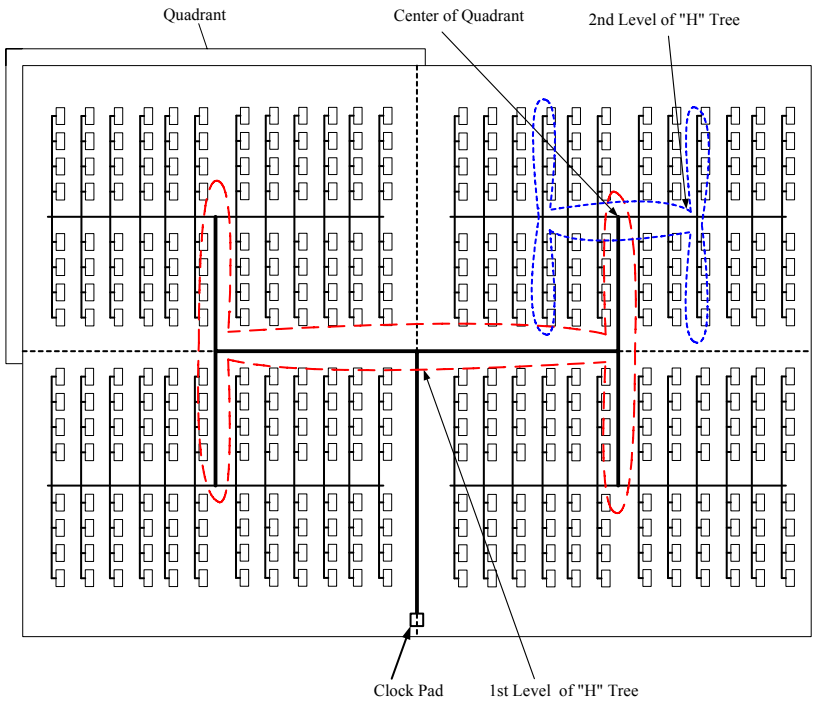


Figure 2: Fabric H-Tree Clock Network Structure



ArcticLink Solution Platform Fabric Global Clock Networks

The QuickLogic ArcticLink solution platform has five global clock networks. Three of these networks are driven directly by clock pads and the remaining two by Configurable Clock Manager (CCM) outputs. The relationship between clock pads and CCM is discussed in **CCM and Clock Network** on page 8. In addition, four internally generated signals can be routed to the clock network through four 2-input muxes located in the middle of the die. These 2-input global clock muxes are also called global H structure clock (HSCK) muxes as shown in **Figure 3** and **Figure 4**. The fifth clock goes from a clock pad directly to the clock network, and is used as a dedicated fast clock. Each global clock network drives four sub-networks called quad-nets, which are discussed in **ArcticLink Solution Platform Fabric Quad-Net Networks** on page 4. The quad HSCK muxes are used for selecting the source for quad-nets. Column clocks are discussed in **ArcticLink Solution Platform Fabric Column Clocks** on page 6.

Figure 3: ArcticLink Solution Platform Fabric Clock Network

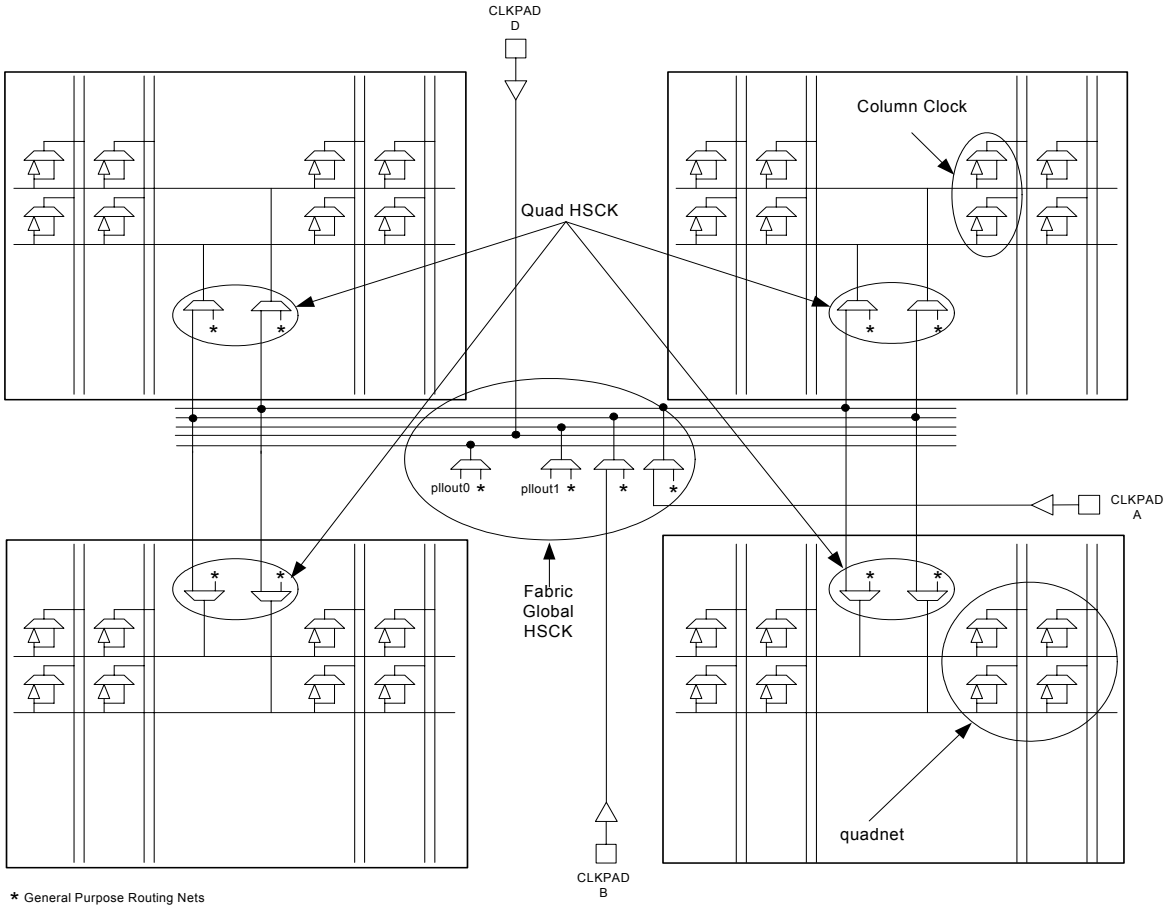
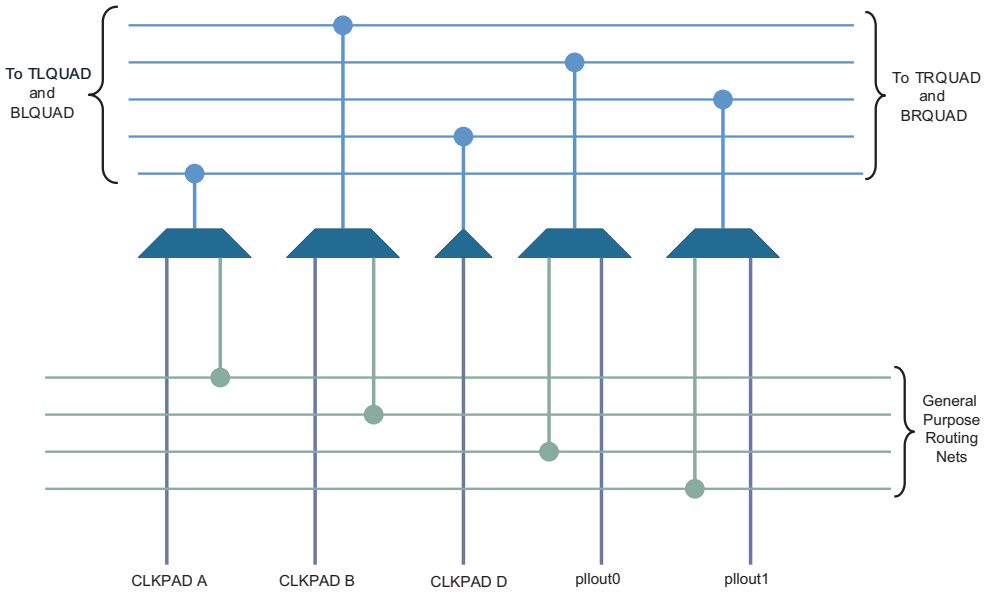


Figure 4: ArcticLink Solution Platform Global HSCK MUX



ArcticLink Solution Platform Fabric Quad-Net Networks

The QuickLogic ArcticLink solution platform comes with five quad-net networks in each quadrant. Quad-nets originate from the five global networks that are routed to each quadrant for a total of 20 quad-nets in a device. However, each quad-net can exist as a standalone clock network. This architecture offers the possibility to have several fast and low skew signals driving the various logic clocks. For example, if a signal on a global clock network drives logic in only two quadrants, the remaining segments of this clock network in the other two quadrants can be used for other signals. To achieve this flexibility of the quad-nets, a two-input multiplexer is used in each quadrant for each global clock net. One input is driven by the output of the global clock mux in the center of the die and the other is accessible to any internally generated signal. **Figure 5** and **Figure 6** show a quad-net with the two-input multiplexer.

Internally generated clocks can be placed on the global or quad-net clock network by instantiating a global clock buffer macro, GCLKBUFF, in the design. QuickLogic SpDE software determines which type of clock network to place the clock on.

Figure 5: Quad-Net with the 2-Input Multiplexer

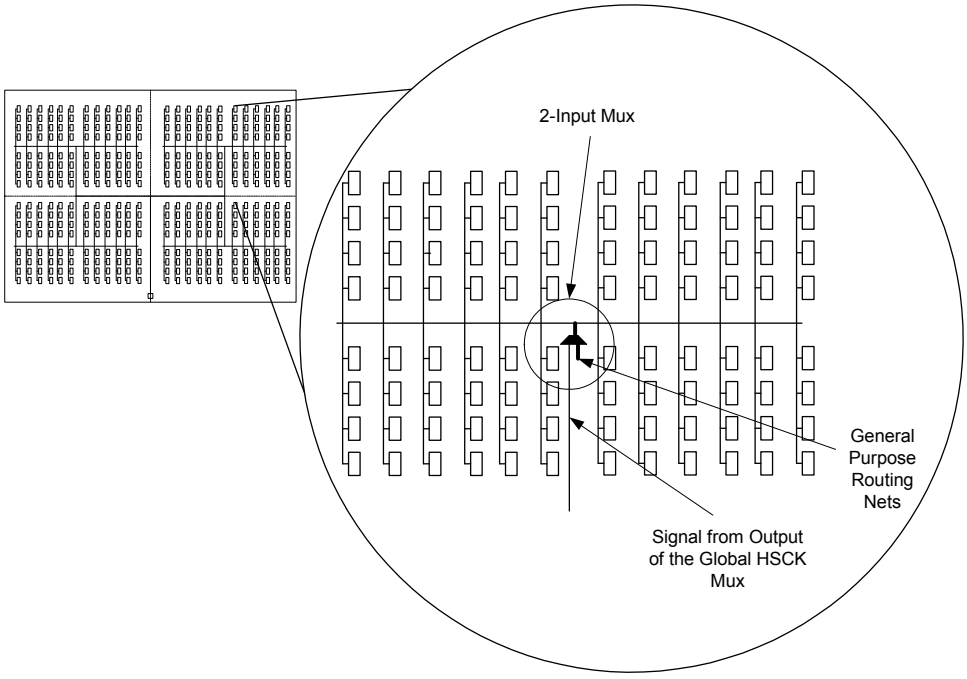
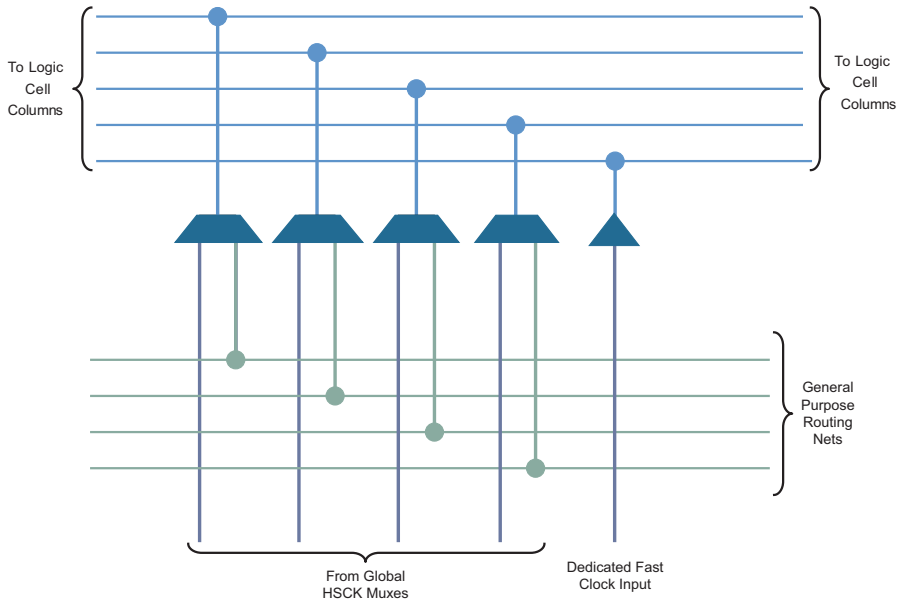


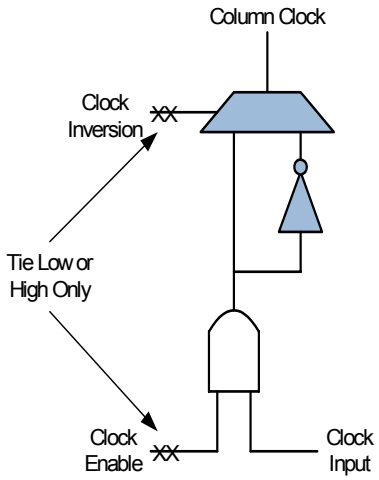
Figure 6: ArcticLink Solution Platform Quad-Net MUX (Single Quad (1/4))



ArcticLink Solution Platform Fabric Column Clocks

Each logic cell column in the Fabric of the ArcticLink solution platform has access to the five column clocks. The designer can select to use either an inverted clock or a non-inverted version of the clock. If the column clock buffer is not used, it will be disabled to provide power savings. **Figure 7** shows the ArcticLink solution platform Fabric column clock buffer in detail.

Figure 7: ArcticLink Solution Platform Fabric Column Clock Buffer



Nets Driven by Global and Quad-Net Networks

Global clock networks can connect to the inputs of the logic, I/O, and RAM cells as shown in **Table 1**. They can drive all the inputs of the logic cell (see **Figure 8**) as well as the clock, reset and enable signals of the INPUT and OUTPUT flip-flops of the I/O cells. Conversely, the clock input drives the clock and reset signals only of the ENABLE flip-flop of the I/O cells (see **Figure 9**). In addition, the clock can drive all the inputs (WCLK, RCLK, WEN[1:0], RD_SEL, WE_SEL, WD[17:0], WA[8:0] and RA[8:0]) to the RAM blocks.

Table 1: Inputs Driven by the Clock Networks

Clock Type	Input Driven in Logic Cells	Input Driven in RAM Cells	Input Driven in I/Os
Global/Quad-Net	All	WEN[1:0], WCLK, RCLK, RD_SEL, WE_SEL, WD[17:0], WA[8:0], RA[8:0]	INPUT flip-flop: Clock, Reset, Enable OUTPUT flip-flop: Clock, Reset, Enable ENABLE flip-flop: Clock, Reset

Figure 8: ArcticLink Solution Platform Logic Cell

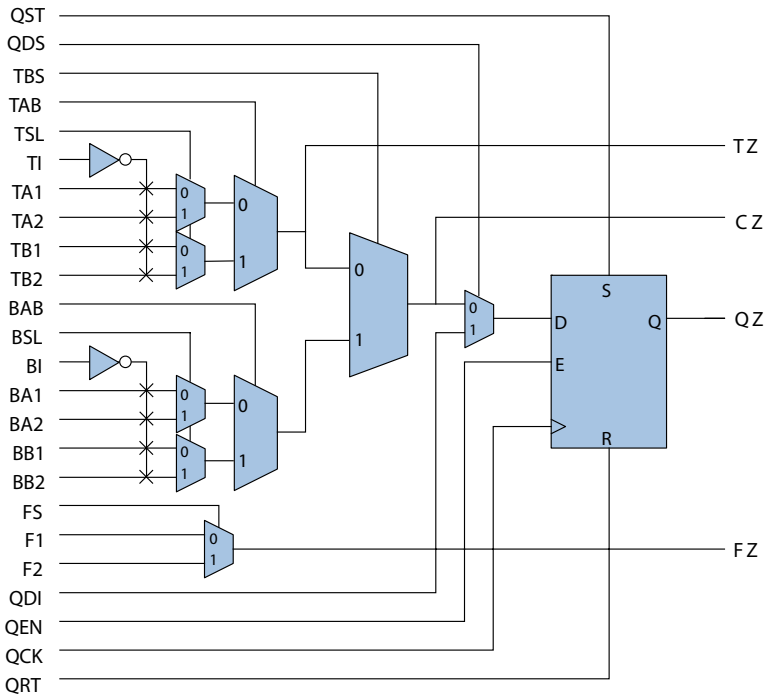
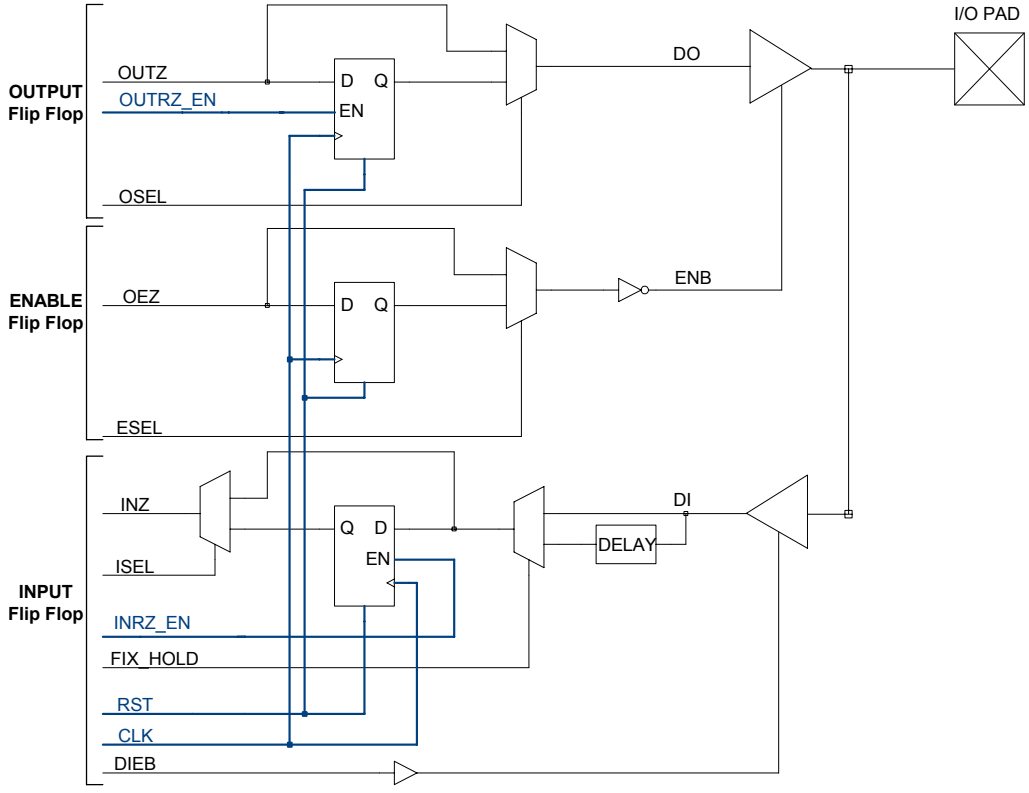


Figure 9: ArcticLink Solution Platform I/O Cell



CCM and Clock Network

The QuickLogic ArcticLink solution platform contains one CCM located in the upper-right corner of the chip (this feature is supported for 196-ball TFBGA package only). Each CCM output (pllout0 and pllout1) can drive a global clock network through a global HSCK mux, or the other input can be connected to an internally generated signal. The clock input to the CCM is provided by CLKPAD <A>, and can simultaneously drive the clock network when enabled by the clock buffer (see **Clock Input Pad Disable** on page 10 for more information about clock disable). In addition, the dedicated feedback path is routed by QuickLogic software tools to ensure that the destination logic clock and CCM input clock are aligned. Once the CCM has synchronized the output clock to the incoming clock, the lock signal is asserted to indicate that the output clock is valid. This lock signal can be routed to internal logic or an output pad and requires at least 10 µs after reset before the signal is asserted. The CCM reset signal can be routed from a clock pad or generated using internal logic. **Figure 10** illustrates the CCM wiring, input pin wiring, and the global HSCK mux.

The ArcticLink solution platform CCM has three modes of operation, based on the input frequency and desired output frequency as shown in **Table 2**. In addition, pllout0 has a 0° phase shift and pllout1 has an optional 0°, 90°, 180°, or 270° phase shift plus a programmable delay up to 2.5 ns at 250 ps intervals.

Figure 10: CCM Wiring to the Global Clock Networks

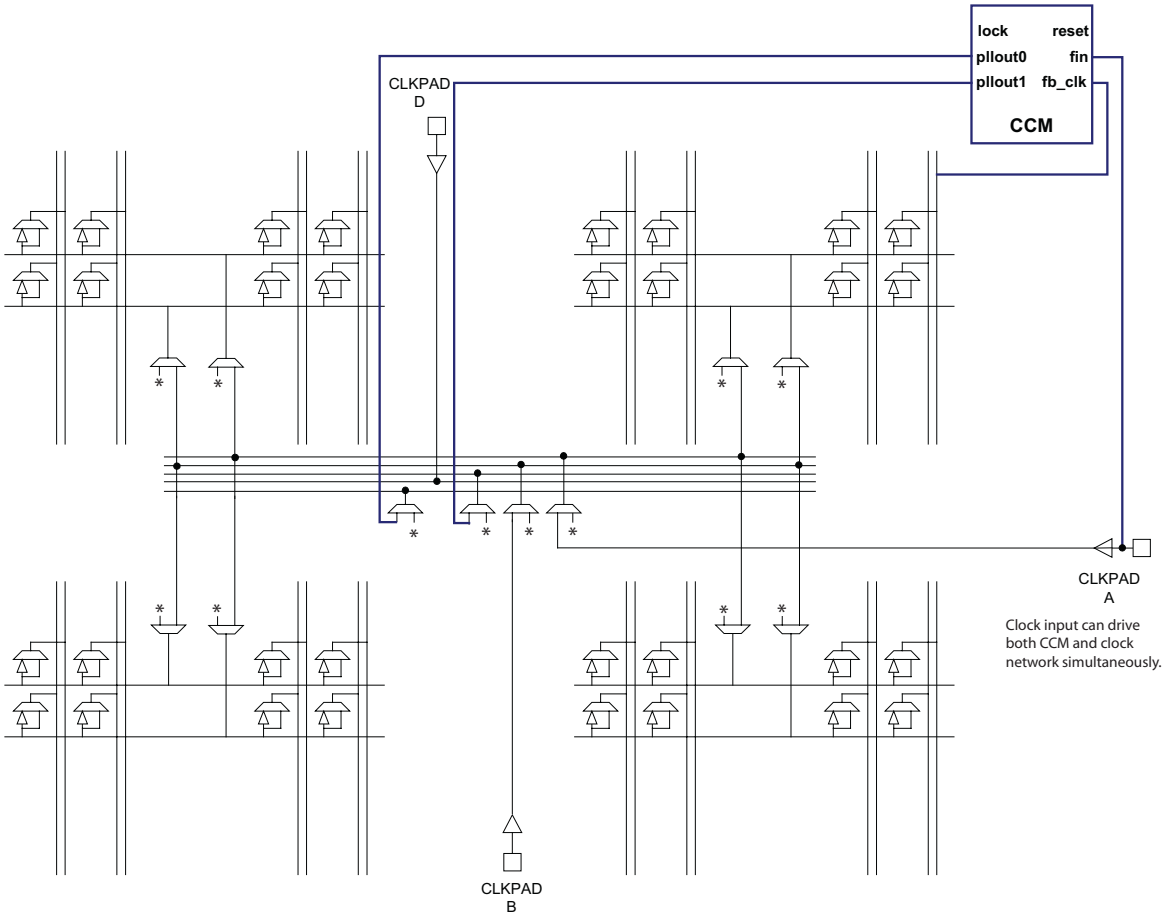


Table 2: CCM PLL Mode Frequencies

Output Frequency	Input Frequency Range	Output Frequency Range	PLL Mode
x1	25 MHz to 200 MHz	25 MHz to 200 MHz	PLL_MULT1
x2	15 MHz to 100 MHz	30 MHz to 200 MHz	PLL_MULT2
x4	10 MHz to 50 MHz	40 MHz to 200 MHz	PLL_MULT4

ASSP Clock Input Ports

The QuickLogic ArcticLink solution platform contains a non-programmable ASSP with two accessible clock inputs at the Fabric-ASSP interface. SYS_CLK is used entirely within the ASSP and shares no timing relationship with the fabric. This signal provides the clock input for the OTG USB Controller (including USB OTG Controller core, dedicated Rx and Tx FIFO, and dedicated DMA engine) as well as the 8 KB Scratch Pad SRAM used for communicating asynchronously with the host processor interface in the fabric. This architecture allows the USB controller to run independently and at higher frequency than the Fabric clock. In addition, SYS_CLK is the base clock frequency for generating the clock in the SD/SDIO/CE-ATA Controller. The SD/SDIO/CE-ATA clock frequency is SYS_CLK/2n where n equals the divider value loaded into the Clock Control Register. Unlike SYS_CLK, FB_CLK remains synchronous with the Fabric. This clock interfaces with host registers and data FIFOs at the host interface of the SD/SDIO/CE-ATA Controller and connects to the Scratch Pad SRAM used for USB data transfers.

Within the Fabric, all five global clock nets and any general purpose routing net can drive SYS_CLK and FB_CLK. This flexibility allows the designer to customize an ASSP clock input. For example, the designer can choose a 25 MHz input on CLKPAD <A> for lower EMI and generate a 100 MHz output using the CCM. This CCM output clock can then be routed to SYS_CLK in the ASSP. In addition, an optional clock divider can be implemented within the fabric to generate FB_CLK from this 100 MHz CCM output. Using the CCM in this way can potentially reduce clock components on the PCB.

To ensure the correct timing requirements between the ASSP FB_CLK domain and the fabric clock networks, the designer must instantiate a global clock macro for the fabric clock as shown in **Figure 11**. This macro is located in the default directory `c:/pasic/spde/data/arcticlink/clk_skew_buff.v`.

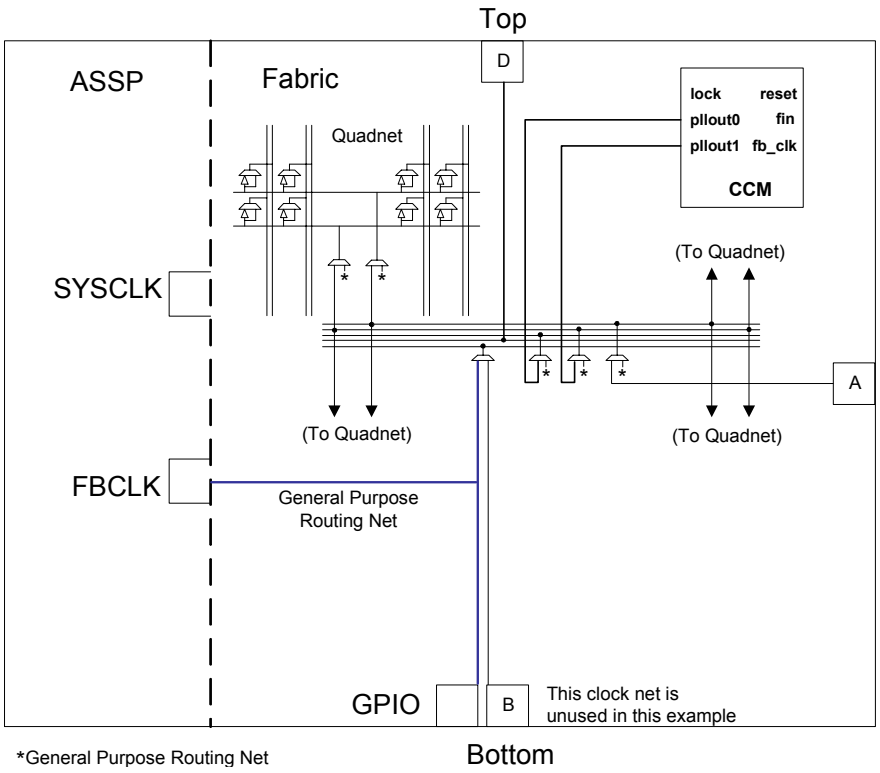
Figure 11: Global Clock Skew Macro

The macro "P" input can be connected to any global clock network driven by a CCM output or CLK pad, and must be implemented when not using a GPIO pin to drive the ASSP FB_CLK input. (The GPIO option is described in the following paragraph.) When this clock skew macro is used, the "Q" output is routed to the global HSCK multiplexers in the center of the fabric and is used to drive all the fabric clock loads. Also, the macro "P" input must be tied directly to the ASSP FB_CLK input by the designer. This layout ensures minimum clock skew between the two domains.

In addition to minimizing clock skew, the designer can reduce power overhead by routing the clock into a GPIO pin as shown in **Figure 12**. This clock signal is driven from the GPIO pin directly to the FB_CLK input of the ASSP using a *general purpose routing net*. Moreover, a GCLKBUFF macro must be instantiated by the designer to drive all the fabric clock loads. With this implementation, the "A" input of the GCLKBUFF macro must be tied to this same general purpose net, while the "Z" output is routed to the global HSCK multiplexers. Using a GPIO pin instead of a CLK input pad reduces the number of utilized clock networks and minimizes the power consumption of the overall clock tree.

NOTE: If the design uses Fabric VLP mode, the system must turn off the GPIO clock input prior to entering low power mode or the designer must ensure that the logic is tolerant of clock glitching. Refer to Application Note 88 at http://www.quicklogic.com/images/appnote88.pdf for more information about using VLP mode.

Figure 12: Recommended ASSP FB_CLK Routing from GPIO



Clock Input Pad Disable

To further improve power consumption and prevent clock glitching in VLP mode, each clock pad input can be disabled by programmable control signals. **Figure 13** and **Table 3** show the clock disable logic that is controlled by two clock enable signals. CLKEN2 is tied high or low and cannot be accessed by an internally generated signal. When this enable signal is set to zero, the clock output is permanently disabled. In contrast, when CLKEN2 is set to one, the clock output can be changed by driving CLKEN1 from internal logic.

NOTE: For CLKPAD <A>, the clock input goes directly to the CCM before entering the clock input pad disable logic.

Figure 13: Clock Input Pad Disable

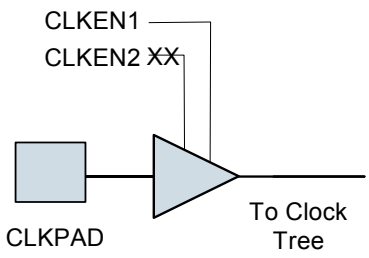


Table 3: Clock Settings

CLKEN1	CLKEN2[a]	Setting
X	0	Permanent disable
0	1	Dynamic disable
1	1	Dynamic enable

a. This signal is not accessible by the user's design, but can be controlled by the QuickLogic software tools.

Conclusion

The QuickLogic ArcticLink solution platform provides flexible clock networks that meet clock signal demands such as signal frequency, propagation delay, and signal skew. This flexibility includes the capacity to disable clock pads and quad-net networks, which can lower power consumption. Moreover, the ability to place a large number of critical signals on the clock network allows complex designs to attain better performance. In addition to these benefits, the CCM can generate internal clock signals from an external clock input, and the dedicated ASSP block can access clock networks and general purpose routing nets via two clock inputs at the Fabric-ASSP interface.

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Revision History

Revision	Date	Originator and Comments
A	April 2007	James Deihl and Kathleen Murchek
B	July 2007	James Deihl and Kathleen Murchek
C	November 2008	Kathleen Murchek Updated contact and trademark info. Added Notice of Disclaimer.
D	April 2009	Kathleen Murchek Updated trademark info.

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