ArcticLink® III BX6 Solution Platform Data Sheet

Platform Highlights

Serial Peripheral Interface (SPI) Master

- Serial interface to control sensors, peripherals, and/or displays.

I²C Client

- CPU interface for configuring and controlling internal registers and look-up tables (LUT).

NOTE: The MIPI interface can also be used instead of I²C.

Onboard Clock Generation

- Integrated, very low power phase-locked loop (PLL) for generating the clocks.

Small Form Factor Packaging

- 120-ball, 4.5 mm x 4.5 mm WLCSP, 0.4 mm ball pitch.

Applications Overview

The ArcticLink III BX6 solution platform is a display interface bridge device enabling the connection of a MIPI 2-lane or MIPI 4-lane processor with a MIPI/RGB, LVDS/RGB, or MIPI/LVDS display, with up to a maximum resolution of 1920x1200 at 60 fps. Featuring a small 4.5 mm x 4.5 mm package, the ArcticLink III BX6 solution platform is a low power solution designed for smartphones and tablets.

ArcticLink III BX6 Solution Platform Variants

The ArcticLink III BX6 solution platform features six distinct variants as described in **Table 1**.

Table 1: ArcticLink III BX6 Solution Platform Variants

QuickLogic Part Order Number	Part Name	Device Input	Device Output	Max. Resolution[a] (60 FPS)	Primary Application
CSSP-BDFDN120	BX6B2E	MIPI-2[b]	MIPI-2[b] and RGB	1366 x 768	Smartphones and tablets with pico projectors
CSSP-BFFDN120	BX6B3E	MIPI-4[c]	MIPI-4[c] and RGB	1920 x 1200	Smartphones and tablets with pico Projectors
CSSP-BUFDN120	BX6B2G	MIPI-2[b]	LVDS-1[d] and RGB	1280 x 800	Tablets with a secondary need for HDMI/MHL encoders
CSSP-BXFDN120	BX6B3G	MIPI-4[c]	LVDS-2[e] and RGB	1920 x 1200	Tablets with a secondary need for HDMI/MHL encoders
CSSP-CAFDN120	BX6B2H	MIPI-2[b]	MIPI-2[b] and LVDS-1[e]	1280 x 800	Tablets with a secondary need for HDMI/MHL encoders
CSSP-CBFDN120	BX6B3H	MIPI-4[c]	MIPI-4[c]and LVDS-2[f]	1920 x 1200	Tablets with a secondary need for HDMI/MHL encoders

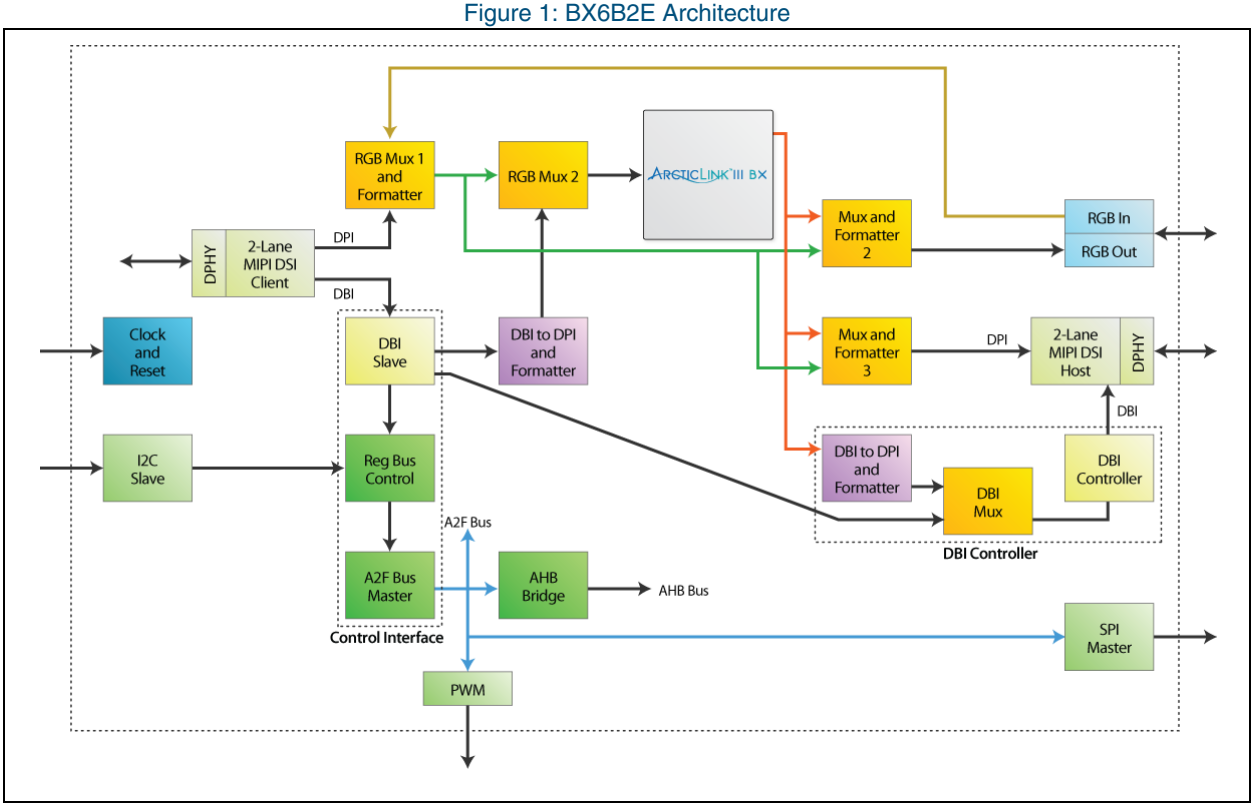
a. MIPI “video mode” only.
b. MIPI-2: Two lane MIPI.
c. MIPI-4: Four lane MIPI.
d. LVDS-1: One channel LVDS.
e. LVDS-2: Two channel LVDS

Data Paths

BX6B2E — MIPI-2 to MIPI-2 and RGB

CAUTION: It is possible to simultaneously send video data through MIPI video mode and register commands through MIPI command mode. Video data sent over MIPI command mode is limited to no more than FWVGA (854x480) resolutions.

Figure 1: BX6B2E Architecture



Use Case

Data path input and outputs are:

- Input – MIPI 2-lane
- Output – MIPI 2-lane and RGB

Control path input and outputs are:

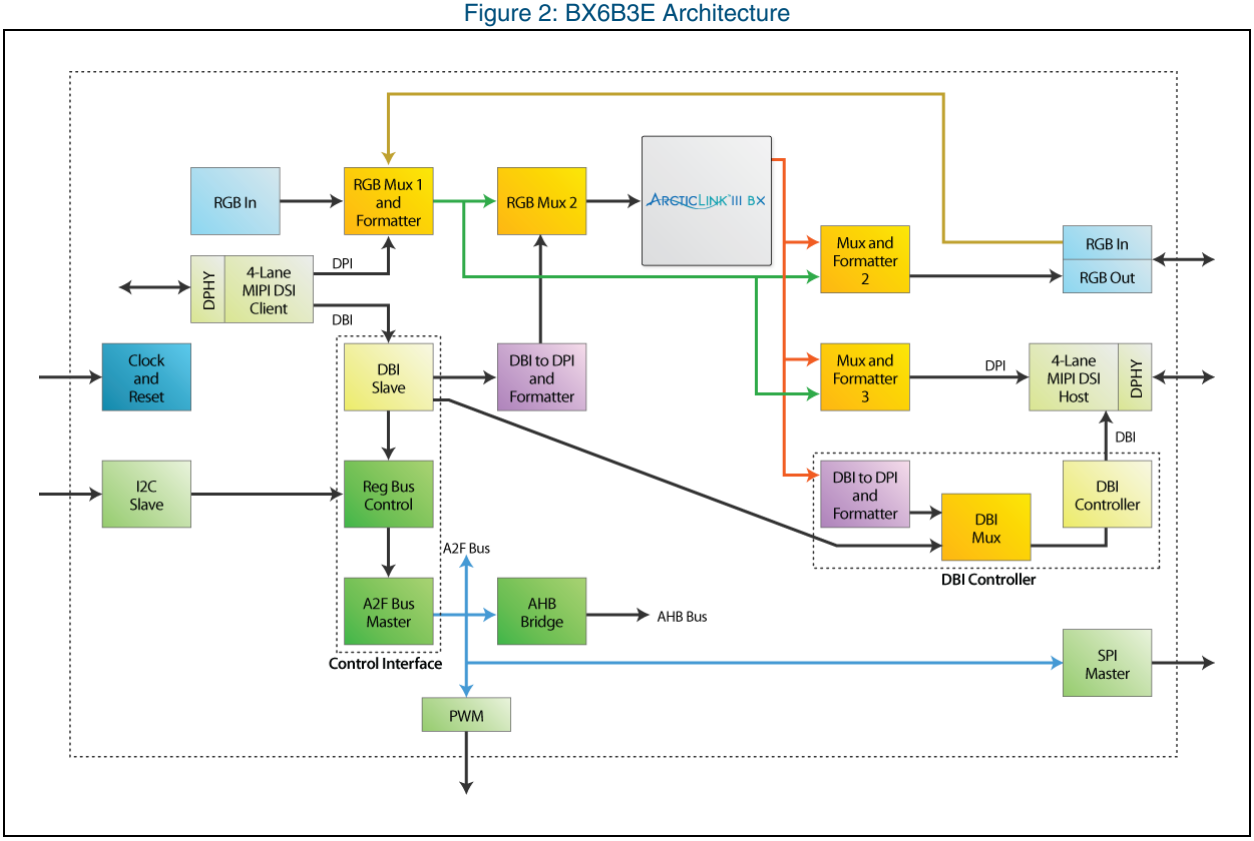
- Input – I^2C and/or MIPI DBI
- Output – SPI and/or MIPI DBI

Maximum resolution is WXGA (1366 x 768)at 24 bpp at 60 fps. The speed is limited by MIPI bandwidth.

BX6B3E — MIPI-4 to MIPI-4 and RGB

CAUTION: It is possible to simultaneously send video data through MIPI video mode and register commands through MIPI command mode. Video data sent over MIPI command mode is limited to no more than FWVGA (854x480) resolutions.

Figure 2: BX6B3E Architecture



Use Case

Data path input and outputs are:

- Input – MIPI 4-lane
- Output – MIPI 4-lane and RGB

Control path input and outputs are:

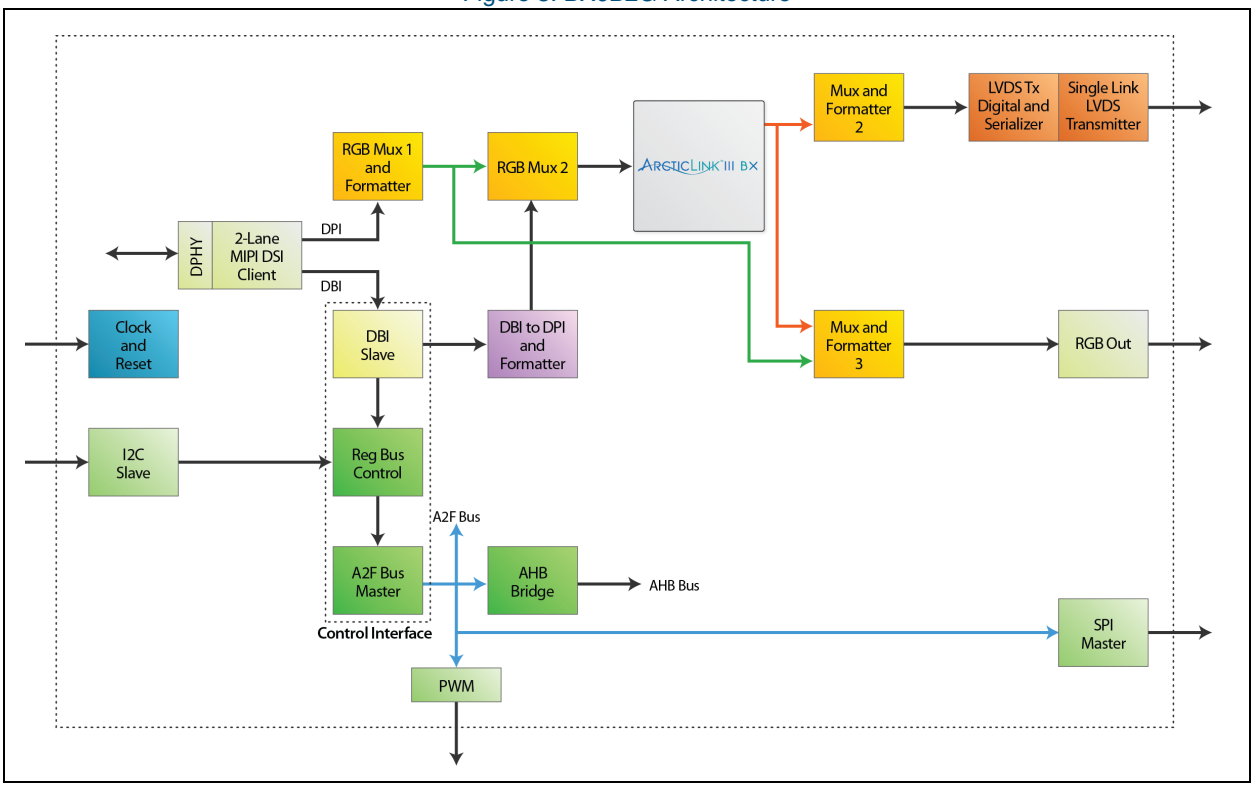
- Input – I^2C and/or MIPI display bus interface (DBI)
- Output – SPI and/or MIPI DBI

Maximum resolution is WUXGA (1920 x 1200) at 24 bpp at 60 fps. The speed is limited by MIPI bandwidth.

BX6B2G — MIPI-2 to LVDS-1 and RGB

CAUTION: It is possible to simultaneously send video data through MIPI video mode and register commands through MIPI command mode. Video data sent over MIPI command mode is limited to no more than FWVGA (854x480) resolutions.

Figure 3: BX6B2G Architecture



Use Case

Data path input and outputs are:

- Input – MIPI 2-lane
- Output – RGB and LVDS-1

Control path input and outputs are:

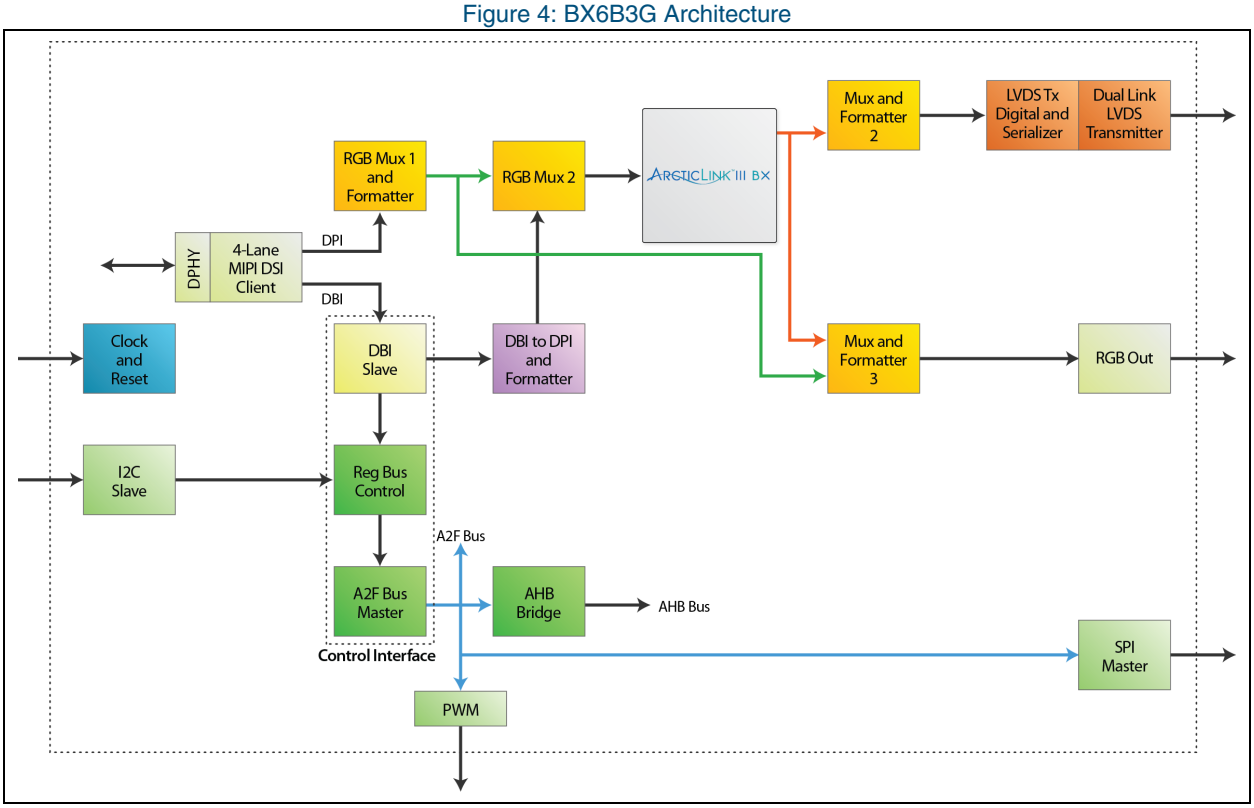
- Input – I^2C and/or MIPI DBI
- Output – SPI

Maximum resolution is 1280 x 800 at 24 bpp at 60 fps. The speed is limited by LVDS bandwidth.

BX6B3G — MIPI-4 to LVDS-2 and RGB

CAUTION: It is possible to simultaneously send video data through MIPI video mode and register commands through MIPI command mode. Video data sent over MIPI command mode is limited to no more than FWVGA (854x480) resolutions.

Figure 4: BX6B3G Architecture



Use Case

Data path input and outputs are:

- Input – MIPI 4-lane
- Output – RGB and LVDS-2

Control path input and outputs are:

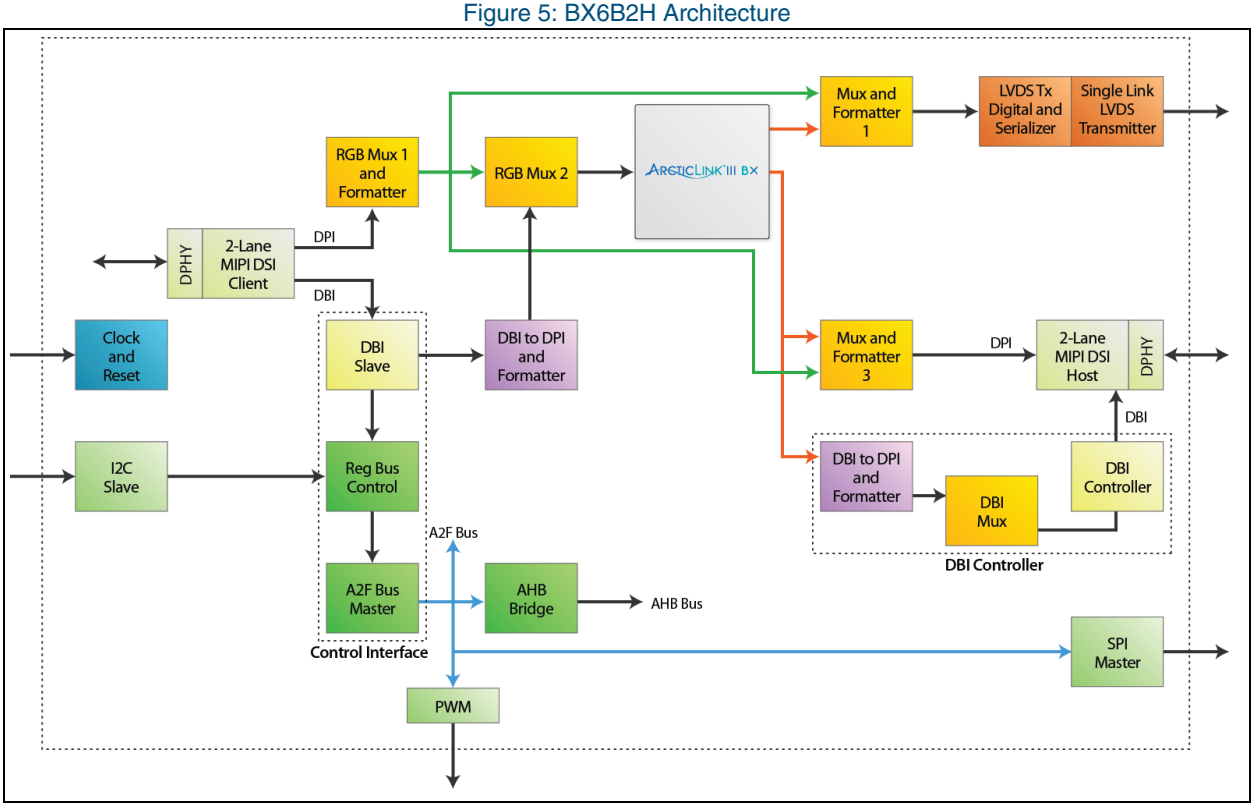
- Input – I^2C and/or MIPI DBI
- Output – SPI

Maximum resolution is 1920 x 1200 at 24 bpp at 60 fps. The speed is limited by MIPI bandwidth.

BX6B2H — MIPI-2 to MIPI-2 and LVDS-1

CAUTION: It is possible to simultaneously send video data through MIPI video mode and register commands through MIPI command mode. Video data sent over MIPI command mode is limited to no more than FWVGA (854x480) resolutions.

Figure 5: BX6B2H Architecture



Use Case

Data path input and outputs are:

- Input – MIPI 2-lane
- Output – MIPI 2-lane and LVDS-1

Control path input and outputs are:

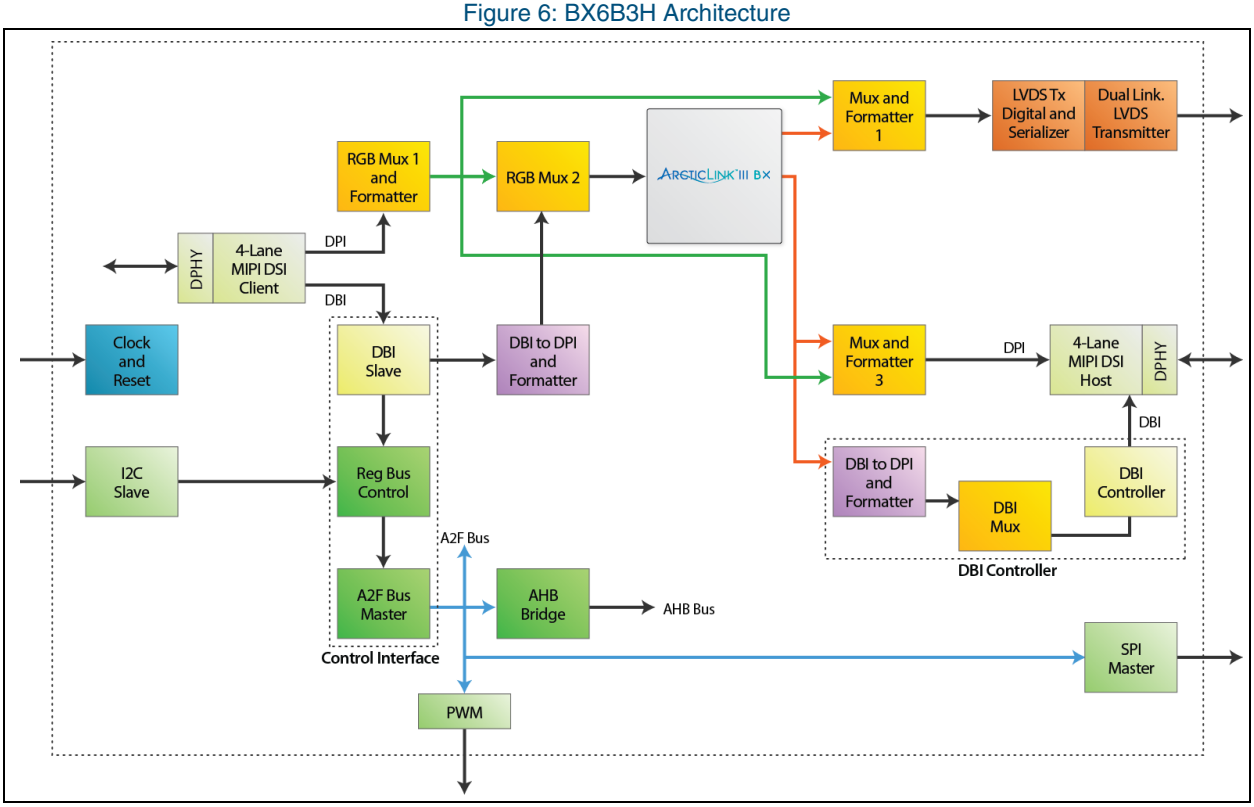
- Input – I^2C and/or MIPI DBI
- Output – SPI

Maximum resolution is 1280 x 800 at 24 bpp at 60 fps. The speed is limited by LVDS bandwidth.

BX6B3H — MIPI-4 to MIPI-4 and LVDS-2

CAUTION: It is possible to simultaneously send video data through MIPI video mode and register commands through MIPI command mode. Video data sent over MIPI command mode is limited to no more than FWVGA (854x480) resolutions.

Figure 6: BX6B3H Architecture



Use Case

Data path input and outputs are:

- Input – MIPI 4-lane
- Output – MIPI 4-lane and LVDS-2

Control path input and outputs are:

- Input – I^2C and/or MIPI DBI
- Output – SPI

Maximum resolution is 1920 x 1200 at 24 bpp at 60 fps. The speed is limited by MIPI bandwidth.

Power Consumption

Table 2 and **Table 3** shows the power consumption in various operating modes.

Table 2: BX6Bxx Power Consumption (mW) at 60 fps[a]

Resolution	Display Width (pixels)	Display Height (pixels)	BX6B2E		BX6B3E		BX6B2G		BX6B3G	
			18 bpp	24 bpp	18 bpp	24 bpp	18 bpp	24 bpp	18 bpp	24 bpp
QVGA	320	240	45.7	49.4	44.5	47.8	90.8	93.77	146.9	150.0
VGA	640	480	56.6	63.1	54.3	59.1	99.5	103.8	155.6	159.9
WVGA	854	480	62.3	69.6	58.3	63.7	103.1	107.9	159.2	164.0
PAL	768	576	64.9	72.8	60.2	65.8	104.8	109.9	160.9	166.0
SVGA	800	600	66.6	75.1	61.7	67.7	106.1	111.4	162.2	167.5
XGA	1,024	768	84.0	95.2	75.0	83.7	117.3	124.3	173.4	180.4
HD 720	1,280	720	90.3	103.0	80.0	89.6	121.5	128.2	177.6	185.3
WXGA	1,366	768	96.9	110.8	85.3	96.0	-	-	181.9	190.3
SXGA	1,280	960	108.4	-	94.6	106.7	-	-	189.5	199.0
SXGA	1,280	1024	113.0	-	98.2	110.9	-	-	192.6	202.6
SXGA+	1,400	1,050	119.3	-	103.3	116.6	-	-	196.6	207.3
UXGA	1,600	1,200	-	-	123.9	141.1	-	-	213.7	227.0
HD 1080	1,920	1,080	-	-	129.6	147.4	-	-	218.3	232.4
WUXGA	1,920	1,200	-	-	139.7	159.1	-	-	226.6	241.9

a. MIPI DBI command mode is limited to FWVGA (854x480) maximum.

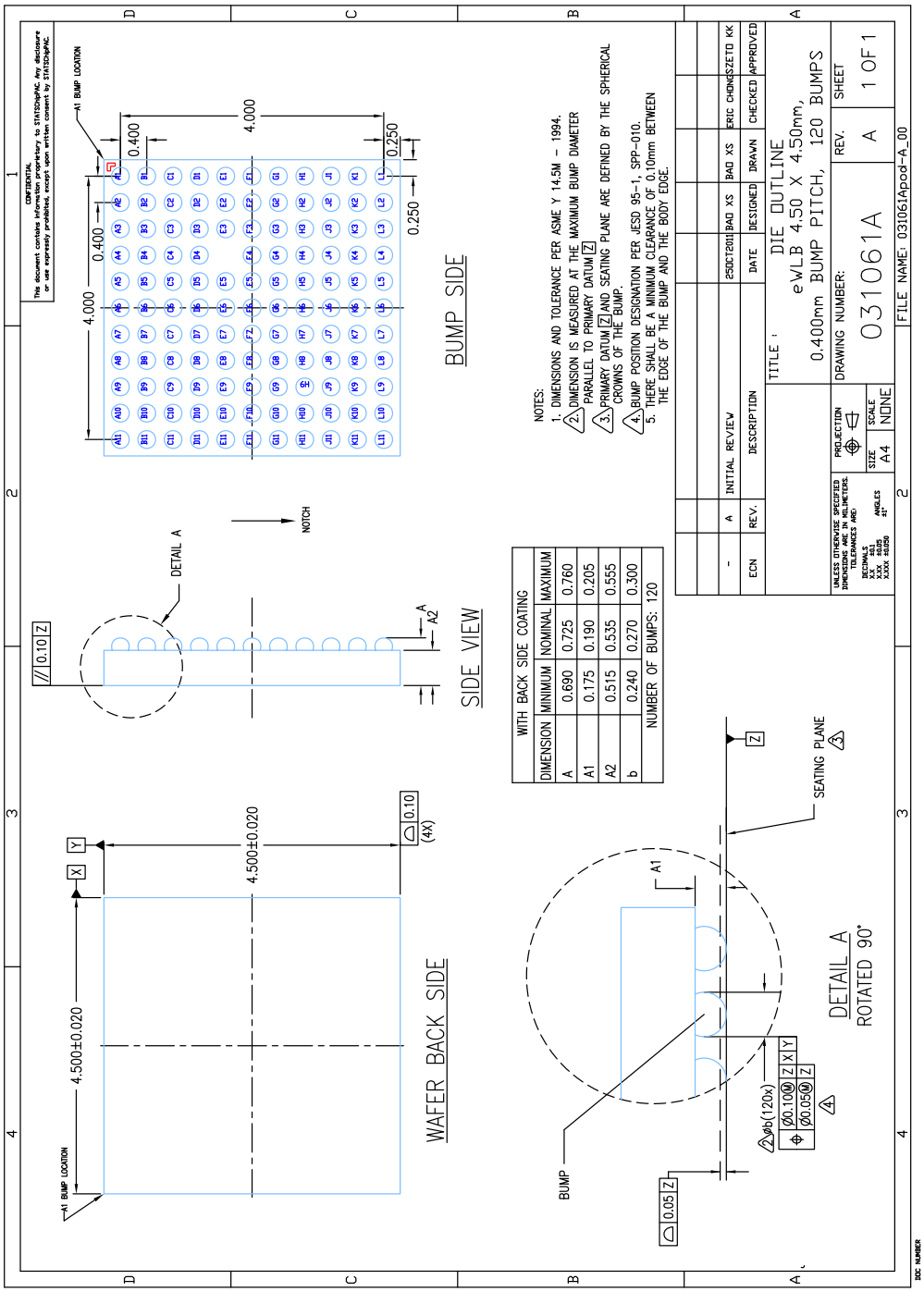
Table 3: BX6Bxx Power Consumption (mW) at 60 fps[a]

Resolution	Display Width (pixels)	Display Height (pixels)	BX6B2H		BX6B3H	
			18 bpp	24 bpp	18 bpp	24 bpp
QVGA	320	240	107.9	108.4	170.9	171.7
VGA	640	480	114.2	115.2	176.5	177.4
WVGA	854	480	117.6	118.9	178.7	179.9
PAL	768	576	119.1	120.5	179.4	180.8
SVGA	800	600	120.1	121.8	180.7	181.9
XGA	1,024	768	130.5	132.7	190.0	191.2
HD 720	1,280	720	134.2	136.8	193.2	194.6
WXGA	1,366	768	-	-	196.7	198.1
SXGA	1,280	960	-	-	202.8	204.7
SXGA	1,280	1,024	-	-	205.0	207.1
SXGA+	1,400	1,050	-	-	231.5	210.3
UXGA	1,600	1,200	-	-	221.6	224.5
HD 1080	1,920	1,080	-	-	225.3	228.2
WUXGA	1,920	1,200	-	-	231.8	234.9

a. MIPI DBI command mode is limited to FWVGA (854x480) maximum.

Mechanical Drawing

Figure 7: BX6 CSSP 120 (0.4 mm) Ball (4.5 mm x 4.5 mm) WLCSP Mechanical Drawing



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Revision History

Revision	Date	Originator and Comments
1.0	October 2012	Initial production release
1.1	March 2013	Paul Karazuba and Kathleen Bylsma Added packages BX6B2G, BX6B3G, BX6B2H and BX6B3H.
1.2	June 2013	Paul Karazuba and Kathleen Bylsma Updated contact information.
1.3	July 2013	Paul Karazuba and Kathleen Bylsma Updated power consumption numbers.
1.4	June 2016	Brian Faith and Kathleen Bylsma Added QuickLogic Part Order Number to Table 1.

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