Pulse Width Modulator (PWM) Pro Controller Data Sheet

Proven System Block (PSB) for QuickLogic Customer Specific Standard Products (CSSPs)

Features

QuickLogic® CSSPs are architected from a unique combination of semiconductor solution platforms and PSBs based on customer requirements. This data sheet represents a specific PSB that is available for inclusion in a CSSP. To discuss options for adding this PSB to an existing CSSP, or architecting a new CSSP, contact your QuickLogic Customer Solution Architect (CSA).

The PWM Pro Controller has the following features:

- 32-bit frequency counter provides lowest PWM frequency of Fsource/2^{32}
- 32-bit duty cycle counter
- PWM frequency counter re-starts on each VSYNC pulse
- Can be disabled to save power

Overview

The QuickLogic PWM Pro Controller enables the system designer to generate PWM pulses at wider ranges of frequencies.

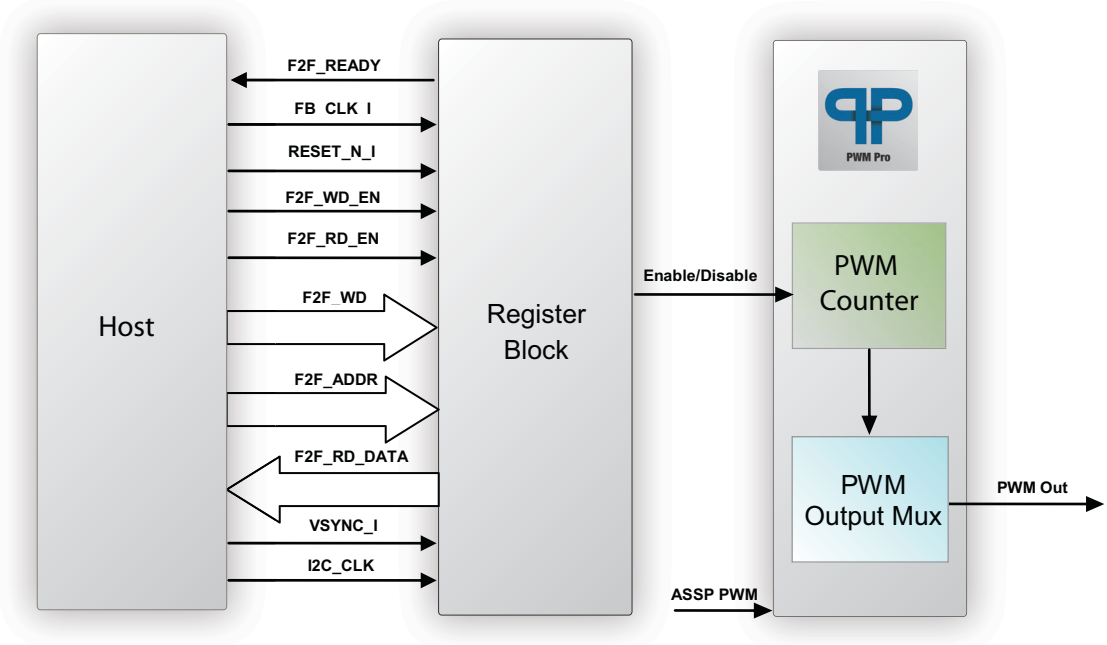
Many embedded PWM controllers are limited in the range of output frequencies that they can provide, limiting their usage and effectiveness in existing systems. The QuickLogic PWM Pro Controller overcomes this limitation, providing a wide range of output frequencies for use in the most demanding applications.

The PWM Pro Controller is available as a PSB within QuickLogic PolarPro® and ArcticLink® II solution platform CSSP families of products. By using CSSPs, system designers are assured of a low-power, small-footprint proven solution.

PSB Architecture

Figure 1 shows a block diagram of the PWM Pro Controller PSB.

Figure 1: PWM Pro Controller Architecture Block Diagram



Functional and Module Description

The PWM Pro Controller PSB consists of the following functional blocks:

- Register — Programmed through a 16-bit data and 4-bit address interface.
- PWM Counter — Loads the frequency division number and the duty cycle values from the register block on each VSYNC pulse.
- PWM Switch — Allows the system designer to select between Fabric PWM/ASSP PWM or keep a continuously high PWM pulse.

Functional Description with Example

If an external oscillator is provided with a source clock of 20 MHz, then FB_CLK_I = 20 MHz and HOST CLK/I2C = 20 MHz (if the Fabric clock is used 'as is' without division).

To achieve a PWM frequency output of 20 kHz with a 60% duty cycle, the following values must be programmed in the registers:

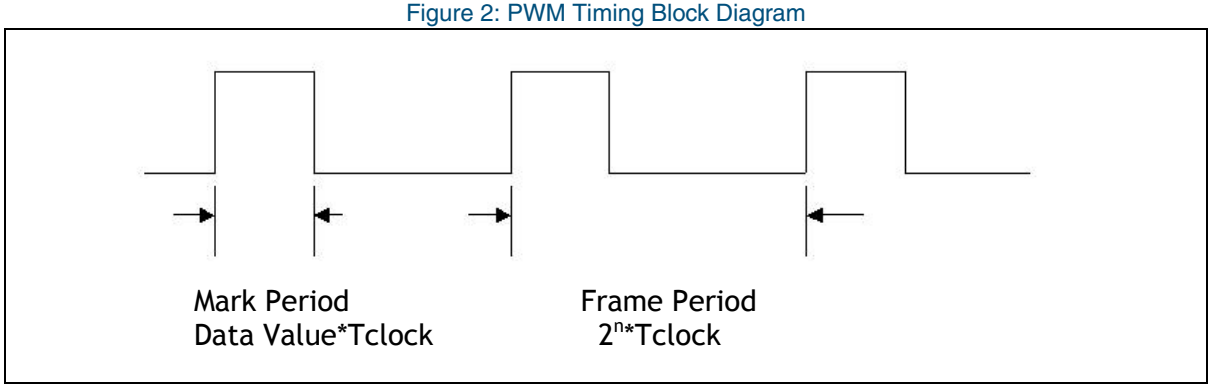
1. Write to the Fabric PWM Control register (lower) = 0x0007. This enables the PWM controller and selects fabric PWM as PWM output source. The PWM Control register (upper) is not used and can be programmed with value = 0x0000.

2. Write to the PWM Frequency register (lower) = 0x03E7 and Frequency register (upper) = 0x0000. Since N = 0x03E7, the divisor is N+1 = 0x03E8 (i.e., 1000 in decimal). So 20 MHz/1000 = 20 kHz. Frame Period = 1/20 kHz.
3. Write to the PWM Duty Cycle register (lower) = 0x012C and PWM Duty Cycle register (upper) = 0x0000. The duty cycle counter increments on each FB_CLK_I pulse. So programming 0x012C (i.e., 600 in decimal) generates a PWM Logic High pulse (Mark Period) for 600 clock cycles and Low for 400 clock cycles.
4. The PWM counters start running as soon as a VSYNC pulse falling edge is detected. These counters are reloaded with new programmed values (if any) from the Frequency/Duty Cycle registers.

PWM Pro Controller Timing

Figure 2 shows the PWM timing block diagram.

Figure 2: PWM Timing Block Diagram



Host – PWM Pro Controller Interface Timing Diagrams

Figure 3 shows the Write timing diagram.

Figure 3: Write to PWM Pro

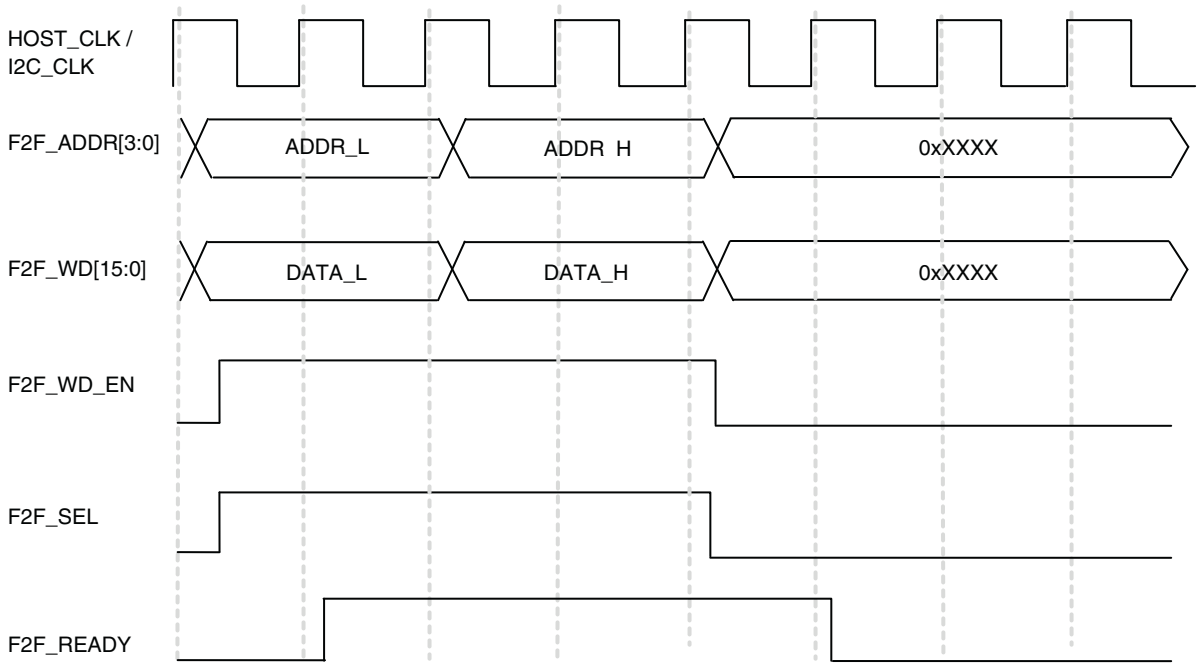
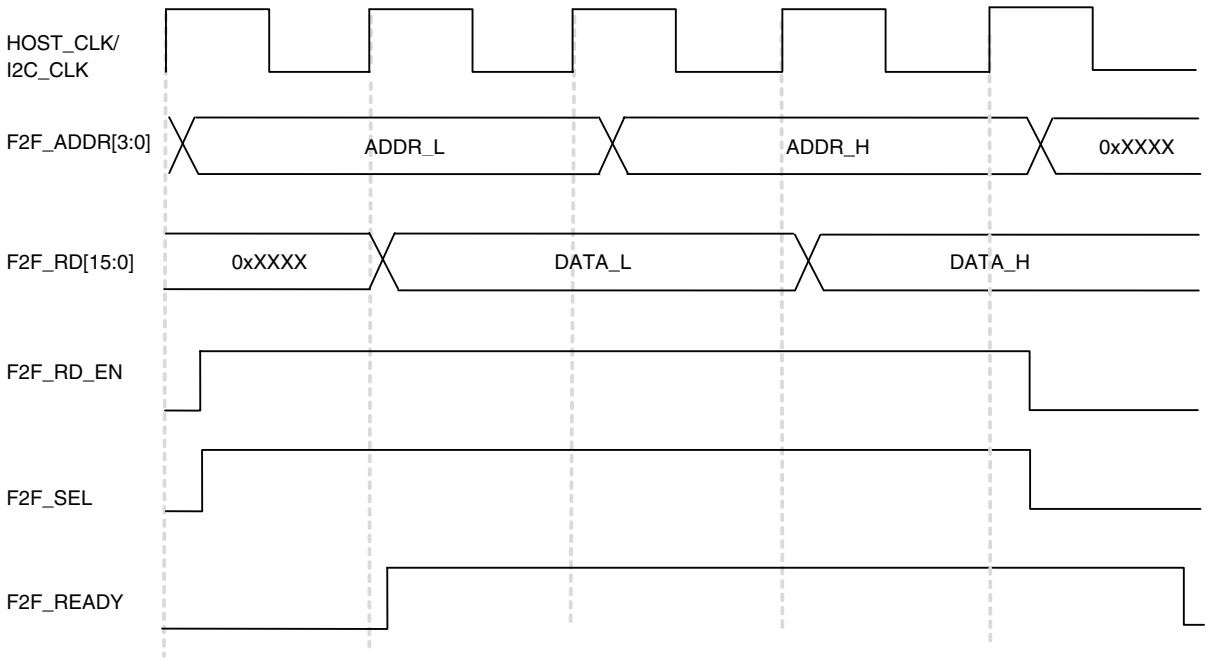


Figure 4 shows the Read timing diagram.

Figure 4: Read from PWM Pro



Interface List and Description

Table 1 summarizes the PWM Pro Controller PSB interface signals.

Table 1: Pin Descriptions

Pin	Direction	Description
FB_CLK_I	Input	CSSP Fabric clock used by PWM Pro Controller for running internal counters.
I2C_CLK_I	Input	Clock signal used by Master I^2C block or reference clock to Write to the PWM registers.
RESET_N_I	Input	PWM block reset. ACTIVE Low signal.
F2F_ADDR_I[3:0]	Input	4-bit address input for accessing the PWM registers.
F2F_WD_I[15:0]	Input	16-bit write data to the PWM registers.
F2F_RD_EN_I	Input	Read enable for reading data from PWM block.
F2F_WD_EN_I	Input	Write enable for writing data to PWM block.
VSYNC_I	Input	Vertical Sync for input video data. Used for loading the new frequency divisor and duty cycle values in the PWM counters.
ASSP_PWM_I	Input	PWM output from the ASSP section.
F2F_RD_O[15:0]	Output	16-bit data Read from PWM registers.
F2F_SEL_I	Input	PWM block chip select. ACTIVE High signal.
F2F_READY_O	Output	PWM Pro block ready for next transfer. ACTIVE High signal.
PWM_O	Output	Muxed PWM output. Select between ASSP PWM/Fabric PWM.

Register Sets

Memory Map

Table 2 shows the memory map of the PSB register set.

Table 2: PSB Memory Map

Register Offset	Register Name	Reset Value	Description
0x0000	Fabric PWM Control Register Lower	0x00000	Master control registers (lower) for Fabric PWM block.
0x0002	Fabric PWM Control Register Upper	0x00000	Master control registers (upper) for Fabric PWM block.
0x0004	Fabric Frequency Register Lower	0x00000	Input frequency clock divider (lower) for Fabric PWM block.
0x0006	Fabric Frequency Register Upper	0x00000	Input frequency clock divider (upper) for Fabric PWM block.
0x0008	Fabric Duty Cycle Register Lower	0x00000	PWM pulse duty (lower) for Fabric PWM block.
0x000A	Fabric Duty Cycle Register Upper	0x00000	PWM pulse duty (upper) for Fabric PWM block.

Register Descriptions

Configuration and Status Registers

Fabric PWM Control Register (Lower)

Register Offset: 0x0000
Reset Value: 0x0000

Name	Bit(s)	Type	Description
Reserved	15:3	R/W	Reserved.
PWM ENABLE	2	R/W	0 - Disable Fabric PWM 1 - Enable Fabric PWM
PWM SOURCE SELECT	1:0	R/W	Selects the driver for the PWM output pin of the CSSP. 10 - ASSP PWM 11 - Fabric PWM 0X - PWM = High

Fabric PWM Control Register (Upper)

Register Offset: 0x0002
Reset Value: 0x0000

Name	Bit(s)	Type	Description
Reserved	15:0	R/W	Reserved.

Fabric PWM Frequency Register (Lower)

Register Offset: 0x0004
Reset Value: 0x0000

Name	Bit(s)	Type	Description
Frequency Lower	15:0	R/W	Lower 16 bits of the Frequency Divide register. If “N’ is the programmed value, the reference clock is divided by N + 1.

Fabric PWM Frequency Register (Upper)

Register Offset: 0x0006
Reset Value: 0x0000

Name	Bit(s)	Type	Description
Frequency Upper	15:0	R/W	Upper 16 bits of the Frequency Divide register. If “N’ is the programmed value, the reference clock is divided by N + 1.

Fabric PWM Duty Cycle Register (Lower)

Register Offset: 0x0008
Reset Value: 0x0000

Name	Bit(s)	Type	Description
Duty Cycle Upper	15:0	R/W	Lower 16 bits of the Duty Cycle register. The value specifies the number of clock cycles the PWM output remains High.

Fabric PWM Duty Cycle Register (Upper)

Register Offset: 0x000A
Size: 16-bits
Type: Read/Write
Reset Value: 0x0000

Name	Bit(s)	Type	Description
Duty Cycle Upper	15:0	R/W	Upper 16 bits of the Duty Cycle register. The value specifies the number of clock cycles the PWM output remains High.

Supported Operating Systems

The PWM Pro Controller PSB supports the following operating systems:

- Windows® CE
- Windows Mobile®
- Linux®
- Android®

Contact Information

Phone: (408) 990-4000 (US)
(647) 367-1014 (Canada)
+(44) 1932-21-3160 (Europe)
+(886) 2-2345-5600 (Taiwan)
+(86) 21-5116-0532 (China)
E-mail: info@quicklogic.com
Sales: America-sales@quicklogic.com
Europe-sales@quicklogic.com
Asia-sales@quicklogic.com
Japan-sales@quicklogic.com
Support: www.quicklogic.com/support
Internet: www.quicklogic.com

Revision History

Revision	Date	Originator and Comments
A	November 2010	Paul Karazuba and Kathleen Bylsma

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