PolarPro® – The Optimal Choice for Low Power Designs

QuickLogic® White Paper

Introduction

In recent history, power consumption has changed from an idle concern to a monumental obstacle. Despite the convenience of designing with programmable logic devices, they have until now, been synonymous with high power consumption. QuickLogic has addressed the requirement for low power designs with its PolarPro family, leveraging its unique ViaLink® anti-fuse technology along with power reducing features to create a device that is low power by design. QuickLogic's PolarPro family is ideally suited for optimizing programmable applications for minimal power consumption.

Summarized throughout this document are details about how the various features of QuickLogic's PolarPro devices can be used to create designs that ensure a low power implementation. Specific features such as internal clock gating, low power mode, and the inherent power savings due to QuickLogic's unique ViaLink technology will be discussed.

Clock Gating Capability

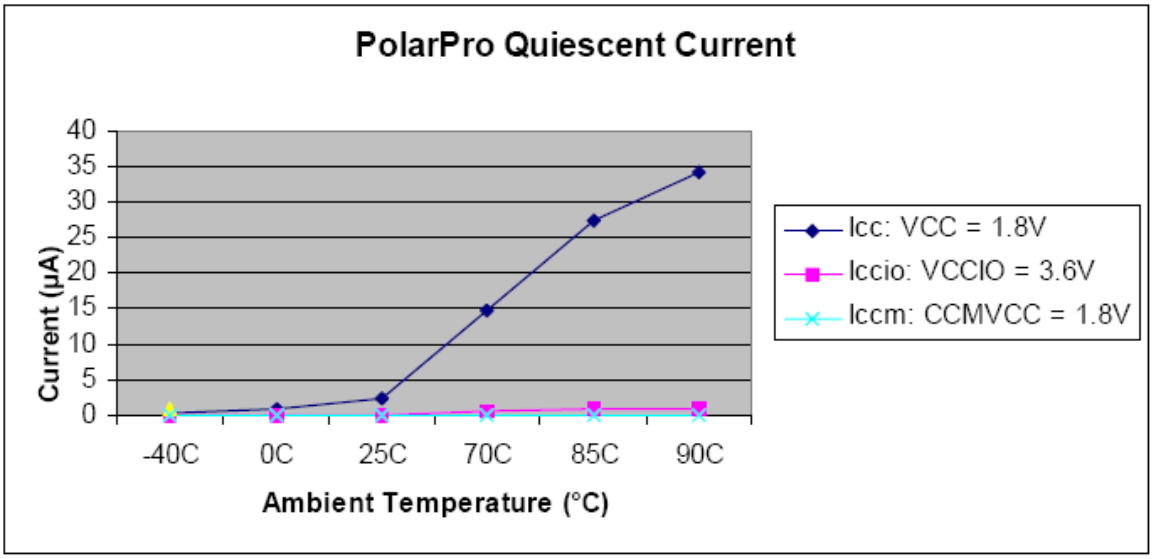
Devices in the QuickLogic PolarPro family, QL1P200 and larger, provide a powerful dynamic clock disable feature that allows designers to dynamically enable and disable clocks routed into the QuickLogic device. Gating a clock contributes to a significant amount of power savings because the amount of toggling on active clock routing resources, flip-flops, and general purpose routing is reduced. Turning off the clocks at the source input pad not only saves power caused by all of the clock routing resources, but also power consumed by all of the corresponding logic associated with the clock.

As an additional feature, PolarPro devices have built-in deglitching circuitry to prevent clock glitching during transitions so that clocks can be enabled or disabled asynchronously without worrying about false edge detection within the internal logic. Without deglitching circuitry, gating clocks generally require extensive planning and partitioning of modules. This valuable feature eases the implementation of designs as well as results in considerable power savings.

Very Low Power (VLP) Mode

QuickLogic PolarPro devices have a unique feature, called VLP mode, which reduces power consumption by placing the device in standby. Specifically, VLP mode can bring the total standby current down to less than 5 µA at room temperature when no incoming signals are toggled. **Figure 1** shows the current response for a PolarPro QL1P100 across a wide range of operating temperatures. Worthy of note is that at room temperature the whole device draws close to only 5 µA of current. Even at 90°C, the PolarPro device consumes less than 35 µA.

Figure 1: Quiescent Current for QL1P100 with VLP = 0 V



VLP mode is controlled by the VLP pin. The VLP pin is active low, so VLP mode is activated by pulling the VLP pin to ground. Conversely, the VLP pin must be pulled to 3.3 V for normal operation. In VLP mode, all General Purpose Input Output (GPIO) ports maintain the status they had before the VLP mode was entered – driving high, low, or hi-impedance. All Double Data Rate Input Outputs (DDRIOs) are pulled low. In addition, all internal memory circuits (logic cell flip-flops, I/O cell flip-flops, RAM blocks, and FIFO controllers) maintain the same logic values after getting out of VLP mode as prior to getting into VLP mode. In VLP mode, all clocks coming into the FPGA will be disabled, regardless of whether they were enabled or disabled using the dynamic clock disable feature.

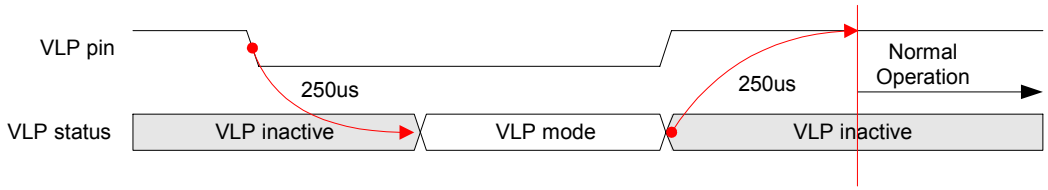
When a PolarPro device goes into VLP mode, the following occurs:

- All logic cell registers and GPIO register values are held
- All RAM cell data is retained
- The output from all GPIO to the internal logic are tied to a weak '1'
- GPIO outputs drive the previous values
- DDRIO levels are pulled down via a weak pull down circuit
- Clock pad inputs are gated
- Configurable Clock Managers (CCMs) are held in the reset state

In QL1P200 and larger devices, the built-in deglitching circuitry prevents glitching in VLP mode the same way as during clock disable and enable transitions. Smaller PolarPro devices such as QL1P075 and QL1P100 do not include this deglitching circuitry, so additional circuitry must be used to prevent glitches.

As mentioned in the VLP behavioral description, the output of the GPIO to the internal logic is a weak '1'. Therefore, to preserve register data, do not use GPIO for a set, reset, or clock signal. As the device exits out of VLP mode, the saved data from the registers, RAM, and GPIO is used to recover the functionality of the device. The entire operation from normal mode to VLP mode requires 250 µs (300 µs maximum). **Figure 2** shows how the timing behavior of VLP mode operates.

Figure 2: Typical VLP Mode Timing



ViaLink Anti-Fuse Technology

QuickLogic's PolarPro devices have an innate advantage over conventional FPGAs, in that PolarPro has a unique anti-fuse technology called ViaLink. Standby power depends heavily on the electrical characteristics of a component. Due to the extensive number of SRAM cells within SRAM FPGA interconnects, they can consume hundreds of milliamps even at standby. Since PolarPro anti-fuse FPGAs have metal-to-metal interconnects, they do not require the additional transistors, and hence power, to retain these interconnects. This results in the perfect combination of low operating voltage and small process geometry with very little leakage current. **Table 1** shows the DC characteristics based on quiescent current when a PolarPro device is powered-up, but has no clocks or I/Os toggling.

Table 1: PolarPro Quiescent Current Consumption

Symbol	Parameter	Conditions	Typical	Units
IVLP	Quiescent Current on VLP pin	VLP = 3.3 V	1	µA
ICCM	Quiescent Current on each CCMVCC	VCC = 1.89 V	1	µA
IVCC	Quiescent Current	VLP = GND	5	µA
		VLP = 3.3 V	40	µA
IVCCIO	Quiescent Current on VCCIO	VCCIO = 3.6 V	2	µA
		VCCIO 2.75 V	2	µA
		VCCIO = 1.89 V	2	µA

Power-Up Sequencing Power Savings

Current associated with the power-up sequence of a device is referred to as in-rush current and is device-specific. For example, Synchronous Random Access Memory (SRAM)-based FPGAs have a high in-rush current because upon power-up these devices are not configured and need to actively download data from external memory chips, such as an EEPROM, to configure their programmable resources. This operation is required to configure their routing connections and look-up tables. However, not only does this require an initial configuration time period, but it also causes a sudden increase in current draw each time the device is powered-up. Conversely, anti-fuse-based FPGAs do not have a high in-rush current since they are already configured and do not require power-on configuration.

Small, Low-Profile Packaging

Low power designs typically require a small form factor and packaging that does not dissipate excessive heat. Most low power applications, especially handhelds and portables, require that packages adhere to compact system dimension specifications and safely remove heat away from the chip. Since QuickLogic devices inherently dissipate static and dynamic low power, the die can be encased in smaller packaging providing greater performance without thermal issues. The PolarPro devices are available in several low profile packages: 132-pin (8mm x 8mm) TFBGA, 196-pin (12mm x 12mm) TFBGA, 144-pin TQFP, 256-pin LFBGA, and 324-pin PBGA.

Conclusion

QuickLogic understands the importance of minimal power consumption, which is why every aspect of PolarPro devices was developed with power conservation in mind. Previously, system designers were more interested in improving speed, but due to the recent development of numerous wireless mobile platforms, and embedded portable applications, power consumption has become an increasingly important design concern. For systems where low power is vital, employing power reduction design techniques along with appropriate low power programmable logic technology, to keep system power consumption to a minimum, becomes compulsory.

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Revision History

Revision	Date	Originator and Comments
A	September 2006	Jason Lew and Kathleen Murchek
B	September 2007	Kathleen Murchek
C	July 2008	Jason Lew and Kathleen Murchek

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