



Dual Mode Phone

Inter-processor Communication Using QuickLogic CSSPs

Dual Mode Phone

Subscriber Identity Module (SIM) cards are used in many of today's mobile phones to identify a subscriber, as well as to store personal data such as phone numbers and text messages. Phones containing two SIM cards are increasing in popularity, allowing consumers to use different cellular networks to place and receive calls. According to KPMG Research;

> *"Dual SIM handsets are growing faster than other handsets. Until recently, there were only three companies selling dual SIM phones…now there are about 40 companies in the market."*

A phone that allows two SIM cards to be active at the same time is known as an "active dual SIM phone." There are two types of active dual SIM phones:

- Single call/dual standby: two SIM cards share a baseband processor
- Dual call/dual standby: two SIM cards each use a separate baseband processor

A phone that shares a baseband processor can only use one SIM card at any given time to make or receive a call. A phone with two processors can use two SIM cards simultaneously. A phone that uses two processors requires an inter-processor communication scheme (see Figure 1).

Figure 1. Inter-processor Communication

Inter-processor Communication

For baseband processors to work together simultaneously, they need to communicate with each other. However, these processors were not designed to communicate with one another. Many processors have a SPI port, but are only configured as SPI master. In addition, many processors have different interface voltage levels adding to the communication mismatch. This makes communication impossible.

Inter-processor Communication Solutions

There are several ways to facilitate inter-processor communication.

- Indirect communication through a mailbox (Figure 3)
- Direct communication through a common interface port (Figure 4)

Both of these methods can be implemented using a Customer Specific Standard Product (CSSP) from QuickLogic as a bridge device between the two processors. The CSSP uses programmable fabric that is customized to support different mailbox configurations, as well as additional internal functions. The hardware can be customized to support the software implementation, shortening development time. Figure 2 illustrates some of the different interfaces that can be used to communicate with a baseband processor.

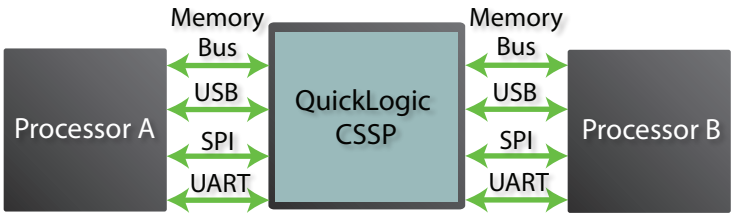

Figure 2. Inter-processor Communication Solutions

QuickLogic offers wide range of inter-processor communication solutions covering all bandwidth requirements. Designers can select different architectures depending on the performance (data exchange between two processors). For example, for low-end/low bandwidth, UART is sufficient. For medium or moderate bandwidth, SPI is sufficient. For high-end/high bandwidth, USB or memory bus SDIO is required.

Low Bandwidth Implementation

Figure 3 demonstrates how to bridge a Qualcomm QSC6085 processor with a NXP 4902 processor. As shown, the QSC6085 has used all its UARTs and cannot directly connect to the NXP processor. Utilizing the local bus on the QSC6085, a local bus-to-UART bridging function, along with a voltage level shifter, is implemented inside the CSSP to facilitate inter-processor communication. Furthermore, additional functions such as GPIO expansion, I2C, and SPI can be integrated.

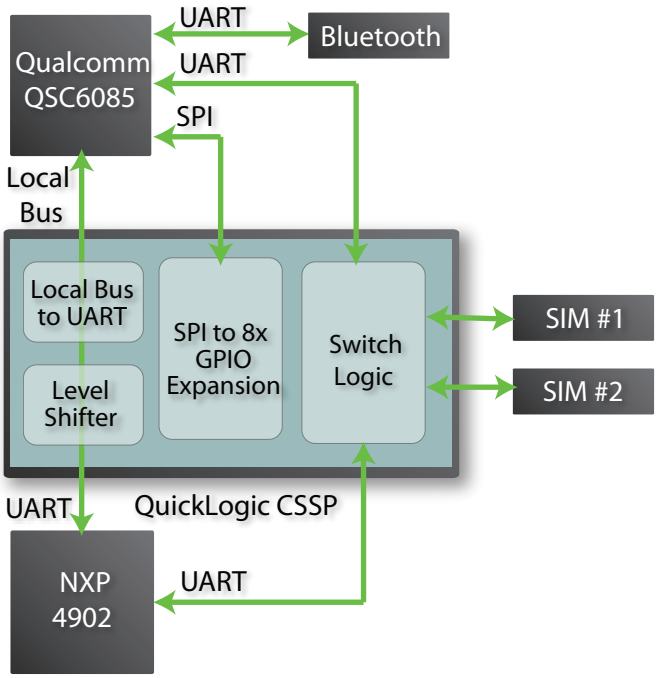

Figure 3. Low Bandwidth Implementation

Medium Bandwidth Implementation

Figure 4 is implemented with SPI slaves, along with a mailbox storage, utilizing the built-in RAM block. This implementation is a better alternative than dual-port RAM structure, as less signals are used, simplifying the PCB layout. The CSSP can also be customized to assist in software implementation.

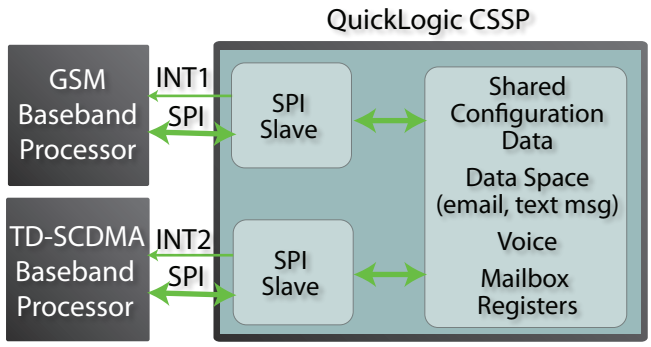

Figure 4. Medium Bandwidth Implementation

High Bandwidth Implementation

Figure 5 is implemented with an SDIO client and Qualcomm memory external bus interface (EBI2) that is ideal for high-end application. In addition, the previous mailbox design can be implemented. Alternatively, interfaces such as USB or other memory buses can be used.

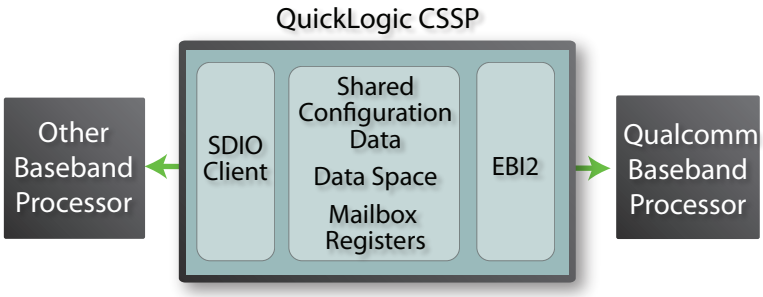

Figure 5. High Bandwidth Implementation

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