Introduction

The QuickLogic ArcticLink III family of devices all have GPIO pins that are multi-functional. Some GPIO can be changed to different functions. Other GPIO are used to set internal configuration registers based on the input values during the power-up sequence. After powering up, these GPIO switch to the corresponding normal operation settings.

ArcticLink III GPIO Functions

The following gives a brief summary of the various GPIO that are available in all ArcticLink III devices. As shown in Table 1, some GPIO have different functions during the power-up sequence. These GPIO values are latched to the ArcticLink III device during reset. At that time, the external host can drive the desired values, and then tri-states these lines after coming out of the reset state as these GPIO switch to their normal operation functions. Alternatively, the GPIO that have power-up configuration functions can be terminated externally with either a pull-up or pull-down resistor.

Table 1: ArcticLink III GPIO Configuration Summary

<table>
<thead>
<tr>
<th>GPIO Number</th>
<th>Data Sheet Reference</th>
<th>Power-Up Configuration Function</th>
<th>Normal Operation Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPIO(0)</td>
<td>PWM_1/GPIO&lt;0&gt;</td>
<td>SYS_CLK input frequency range</td>
<td>PWM 1 output</td>
</tr>
<tr>
<td>GPIO(1)</td>
<td>PWM_2/GPIO&lt;1&gt;</td>
<td>MIPI LP clock divider value</td>
<td>PWM 2 output</td>
</tr>
<tr>
<td>GPIO(2)</td>
<td>SCLK/GPIO&lt;2&gt;</td>
<td>I²C Slave Address bit 0</td>
<td>SPI SCLK</td>
</tr>
<tr>
<td>GPIO(3)</td>
<td>SDO/GPIO&lt;3&gt;</td>
<td>I²C Slave Address bit 1</td>
<td>SPI SDO</td>
</tr>
<tr>
<td>GPIO(4)</td>
<td>I2C_SDA/GPIO&lt;4&gt;</td>
<td>unused</td>
<td>I²C SDA</td>
</tr>
<tr>
<td>GPIO(5)</td>
<td>I2C_SCL/GPIO&lt;5&gt;</td>
<td>unused</td>
<td>I²C SCL</td>
</tr>
<tr>
<td>GPIO(6)</td>
<td>SDI/GPIO&lt;6&gt;</td>
<td>unused</td>
<td>SPI SDI</td>
</tr>
<tr>
<td>GPIO(7)</td>
<td>SS/GPIO&lt;7&gt;</td>
<td>unused</td>
<td>SPI SS</td>
</tr>
<tr>
<td>GPIO(8)</td>
<td>GPIO&lt;8&gt;</td>
<td>unused</td>
<td>unused</td>
</tr>
</tbody>
</table>
GPIO Power-Up Configuration Functions

The ArcticLink III GPIOs 0, 1, 2, and 3 are used as configuration pins during power-up. Depending upon whether there is an external pull-up or pull-down resistor, the corresponding setting is assigned. The following are more in-depth details about the functional behavior of these ArcticLink III GPIO and how to configure them.

- **GPIO(0):**
  - When GPIO(0) has an external pull-down to ground, it indicates that the SYS_CLK input frequency is between 9 MHz and 20 MHz.

- **GPIO(1):**
  - GPIO(1) configures the MIPI Low Power (LP) Clock settings of the MIPI Client interface to the ArcticLink III. As per the MIPI specification, the host processor is responsible for controlling its own clock frequency to match the MIPI client peripheral. The host processor LP clock frequency must be in the range of 67% to 150% of the client LP clock frequency. By default, the MIPI LP clock of the ArcticLink III is the same frequency as the SYS_CLK input. If the SYS_CLK needs to be divided by two to be within 67% to 150% of the processor LP clock, then GPIO(1) should have an external pull-up resistor populated. In summary:
    - When GPIO(1) has an external pull-down to ground, it indicates that the SYS_CLK input frequency is within 67% to 150% of the host MIPI LP clock.
    - When GPIO(1) has an external pull-up to DVDD_0, it indicates that the SYS_CLK input frequency divided by two is within 67% to 150% of the host MIPI LP clock.

- **GPIO(2):**
  - When GPIO(2) has an external pull-down to ground, it sets the I2C Slave Address bit 0 to '0'.
  - When GPIO(2) has an external pull-up to DVDD_1, it sets the I2C Slave Address bit 0 to '1'.

- **GPIO(3):**
  - When GPIO(3) has an external pull-down to ground, it sets the I2C Slave Address bit 1 to '0'.
  - When GPIO(3) has an external pull-up to DVDD_1, it sets the I2C Slave Address bit 1 to '1'.

As an example, if GPIO(2) is pulled down, and GPIO(3) is pulled up, the resulting 7-bit I2C Slave Address would be "1100110", which is 0x66 in hexadecimal.
External Terminations

The following Figure 2, shows an example schematic of how to configure the various external termination resistors to the GPIO. If the input frequency of the SYS_CLK signal and LP clock of the MIPI Host is unknown, optional pull-up resistor locations can be designed for the board. It is important to note, that if an ArcticLink III device has either a MIPI Host or MIPI Client, GPIO(0) must be pulled-down since SYS_CLK must be between 9 MHz to 20 MHz. Conversely, if there is no MIPI Host or MIPI Client, GPIO(1) can be either a pull-up or a pull-down.

If the 7-bit \(^{2}\mathrm{C}\) Slave Address of the ArcticLink III can be set to 0x64, GPIO(2), GPIO(3), GPIO(6), GPIO(7), and GPIO(8) can be pulled down using the same termination resistor. This can help to decrease the number of resistors required for the design.

Generally speaking, unused inputs should always be either pulled up or pulled down. This is because the output of the I/O buffers can couple with the input of the same buffer and result in a high speed oscillation. This produces noise and, potentially, higher current draw than is wanted. Therefore, even though GPIO(4) through GPIO(8) do not have a power-up setting, it is still good engineering practice to terminate them. Figure 2, below shows a more optimized configuration for a board that has a SYS_CLK frequency between 9 MHz and 20 MHz, a MIPI LP clock equal to the SYS_CLK, and with a 7-bit \(^{2}\mathrm{C}\) Slave Address of 0x64.
Contact Information

Phone:  
(408) 990-4000 (US)  
+(44) 1932-21-3160 (Europe)  
+(886) 26-603-8948 (Taiwan)  
+(86) 21-2116-0532 (China)  
+(81) 3-5875-0547 (Japan)  
+(82) 31-601-4225 (Korea)

E-mail:  info@quicklogic.com
Sales:  
America-sales@quicklogic.com  
Europe-sales@quicklogic.com  
Asia-sales@quicklogic.com  
Japan-sales@quicklogic.com  
Korea-sales@quicklogic.com

Support: www.quicklogic.com/support
Internet:  www.quicklogic.com

Revision History

<table>
<thead>
<tr>
<th>Revision</th>
<th>Date</th>
<th>Originator and Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>June 2013</td>
<td>Jason Lew and Kathleen Bylsma</td>
</tr>
</tbody>
</table>
Notice of Disclaimer

QuickLogic is providing this design, product or intellectual property “as is.” By providing the design, product or intellectual property as one possible implementation of your desired system-level feature, application, or standard, QuickLogic makes no representation that this implementation is free from any claims of infringement and any implied warranties of merchantability or fitness for a particular purpose. You are responsible for obtaining any rights you may require for your system implementation. QuickLogic shall not be liable for any damages arising out of or in connection with the use of the design, product or intellectual property including liability for lost profit, business interruption, or any other damages whatsoever. QuickLogic products are not designed for use in life-support equipment or applications that would cause a life-threatening situation if any such products failed. Do not use QuickLogic products in these types of equipment or applications.

QuickLogic does not assume any liability for errors which may appear in this document. However, QuickLogic attempts to notify customers of such errors. QuickLogic retains the right to make changes to either the documentation, specification, or product without notice. Verify with QuickLogic that you have the latest specifications before finalizing a product design.

Copyright and Trademark Information

Copyright © 2013 QuickLogic Corporation. All Rights Reserved.
The information contained in this document is protected by copyright. All rights are reserved by QuickLogic Corporation. QuickLogic Corporation reserves the right to modify this document without any obligation to notify any person or entity of such revision. Copying, duplicating, selling, or otherwise distributing any part of this product without the prior written consent of an authorized representative of QuickLogic is prohibited.

QuickLogic and ArcticLink are registered trademarks, and the QuickLogic logo is a trademark of QuickLogic. Other trademarks are the property of their respective companies.