ArcticLink® III BX5 Solution Platform Data Sheet

Platform Highlights

Serial Peripheral Interface (SPI) Master

- Serial interface to control sensors, peripherals, and/or displays.

Onboard Clock Generation

- Integrated, very low power phase-locked loop (PLL) for generating the clocks.

I²C Client

- CPU interface for configuring and controlling internal registers and look-up tables (LUT).

Small Form Factor Packaging

- 120-ball, 4.5 mm x 4.5 mm WLCSP, 0.4 mm ball pitch.

Applications Overview

The ArcticLink III BX5 solution platform is a display interface bridge device enabling the connection of a RGB, MIPI 2-lane, or MIPI 4-lane processor with a RGB, MIPI 2-lane, MIPI 4-lane, LVDS 1-lane, or LVDS 2-lane display, with up to a maximum resolution of 1920x1200 (60 fps). Featuring a small 4.5 mm x 4.5 mm package, the ArcticLink III BX5 solution platform is a low power solution designed for smartphones and tablets.

ArcticLink III BX5 Solution Platform Variants

The ArcticLink III BX5 solution platform features eight distinct variants as described in **Table 1**.

Table 1: ArcticLink III BX5 Solution Platform Variants

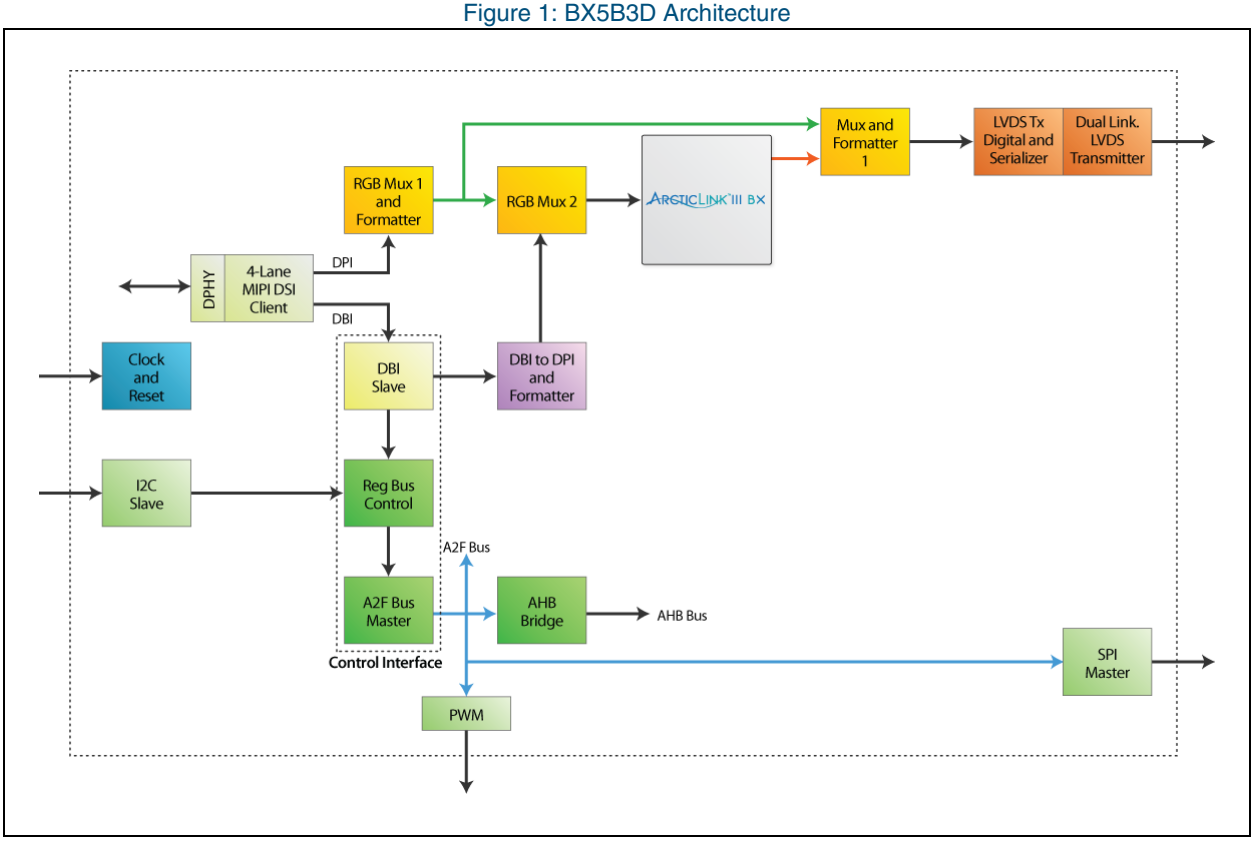
QuickLogic Part Order Number	CSSP Name	Device Input	Device Output	Max Resolution (60 FPS)	Primary Application
CSSP-BMFDN120	BX5B3D	MIPI-4[a]	LVDS-2[b]	1920 x 1200	Smartphones and tablet computers
CSSP-BPFDN120	BX5A1D	RGB	LVDS-1[c]	1280 x 800	Smartphones and tablet computers
CSSP-BQFDN120	BX5A3D	RGB	LVDS-2	1920 x 1200	Smartphones and tablet computers
CSSP-BLFDN120	BX5B1D	MIPI-2[d]	LVDS-1	1280 x 800	Smartphones and tablet computers
CSSP-BGFDN120	BX5B3A	MIPI-4	RGB	1920 x 1200	Smartphones and tablet computers
CSSP-BEFDN120	BX5B2A	MIPI-2	RGB	1366 x 768	Smartphones and tablet computers
CSSP-BJFDN120	BX5A3B	RGB	MIPI-4	1920 x 1200	Smartphones and tablet computers
CSSP-BHFDN120	BX5A2B	RGB	MIPI-2	1366 x 768	Smartphones and tablet computers

a. MIPI-4: Four lane MIPI interface.
b. LVDS-2: Dual link LVDS interface (eight data differential pairs and two clock differential pairs).
c. LVDS-1: Single link LVDS interface (four data differential pairs and one clock differential pair).
d. MIPI-2: Two lane MIPI interface.

Data Paths

BX5B3D — MIPI-4 to LVDS-2

Figure 1: BX5B3D Architecture



Use Case

Data path input and outputs are:

- Input – MIPI 4-lane
- Output – LVDS dual link (four data differential pairs and one clock differential pair)

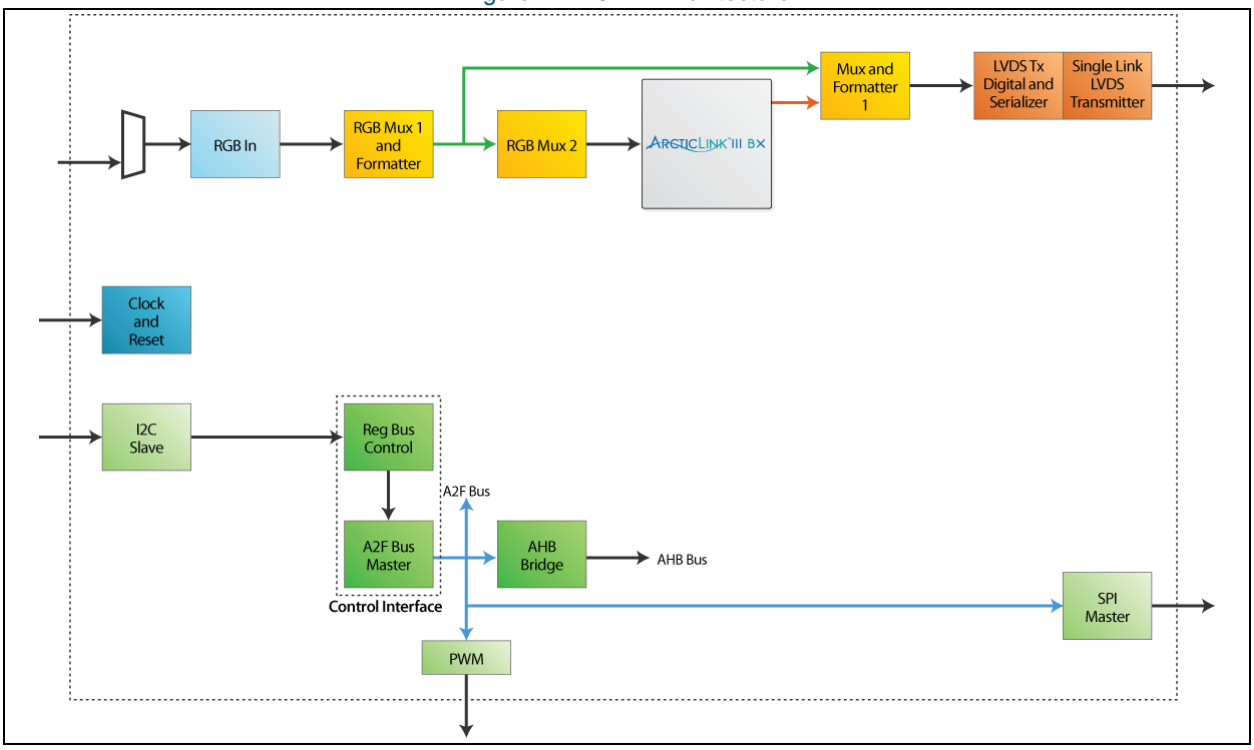
Control path input and outputs are:

- Input – I^2C
- Output – SPI

Maximum resolution is WUXGA (1920 x 1200) at 24 bpp at 60 fps. The speed is limited by LVDS bandwidth.

BX5A1D — RGB to LVDS-1

Figure 2: BX5A1D Architecture



Use Case

Data path input and outputs are:

- Input – RGB
- Output – LVDS single link (four data differential pairs and one clock differential pair)

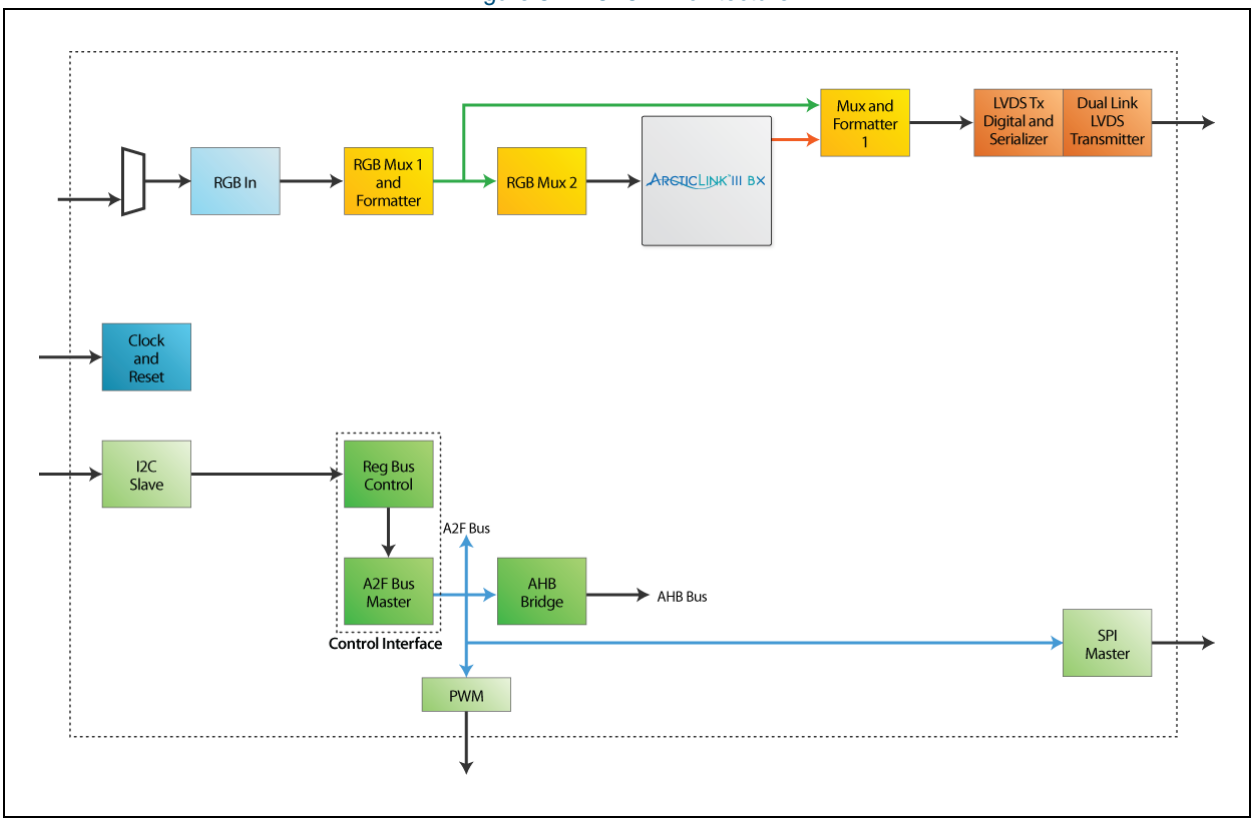
Control path input and outputs are:

- Input – I^2C
- Output – SPI

Maximum resolution is 1280 x 800 at 24 bpp at 60 fps. The speed is limited by LVDS bandwidth, and resolution is dependent on display blanking and pixel clock.

BX5A3D — RGB to LVDS-2

Figure 3: BX5A3D Architecture



Use Case

Data path input and outputs are:

- Input – RGB
- Output – LVDS dual link (eight data differential pairs and two clock differential pairs)

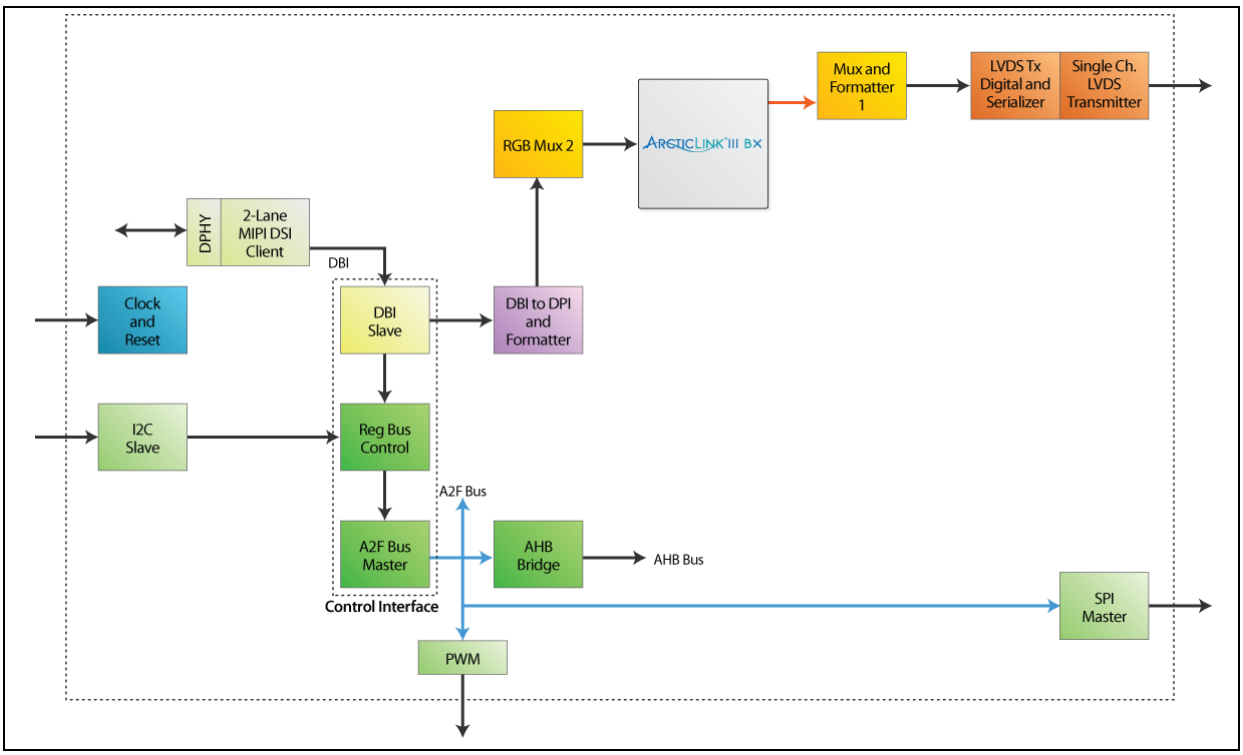
Control path input and outputs are:

- Input – I^2C
- Output – SPI

Maximum resolution is 1920 x 1200 at 24 bpp at 60 fps. The speed is limited by LVDS bandwidth.

BX5B1D — MIPI-2 to LVDS-1

Figure 4: BX5B1D Architecture



Use Case

Data path input and outputs are:

- Input – MIPI 2-lane
- Output – LVDS single link (four data differential pairs and one clock differential pair)

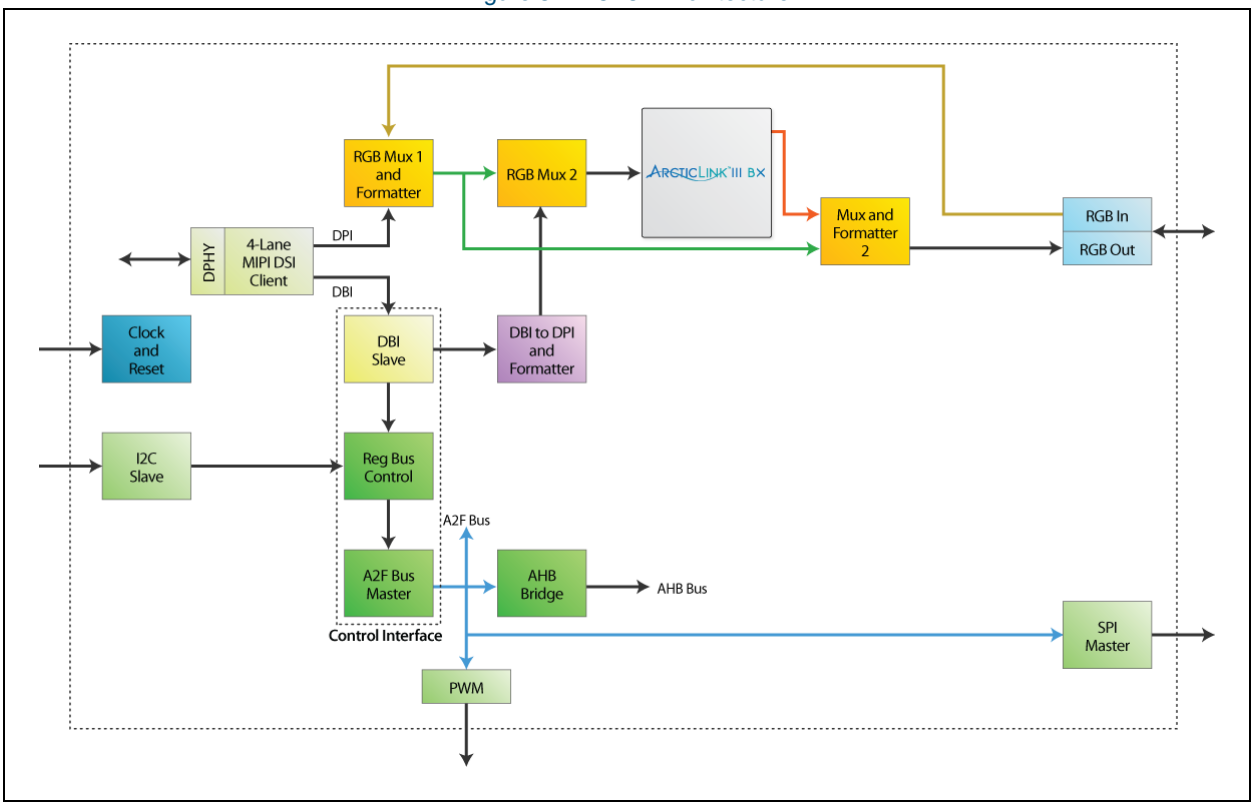
Control path input and outputs are:

- Input – I^2C and/or MIPI display bus interface (DBI)
- Output – SPI

Maximum resolution is 1280 x 800 at 24 bpp at 60 fps. The speed is limited by LVDS bandwidth, and resolution is dependent on display blanking and pixel clock.

BX5B3A — MIPI-4 to RGB

Figure 5: BX5B3A Architecture



Use Case

Data path input and outputs are:

- Input – MIPI 4-lane
- Output – RGB

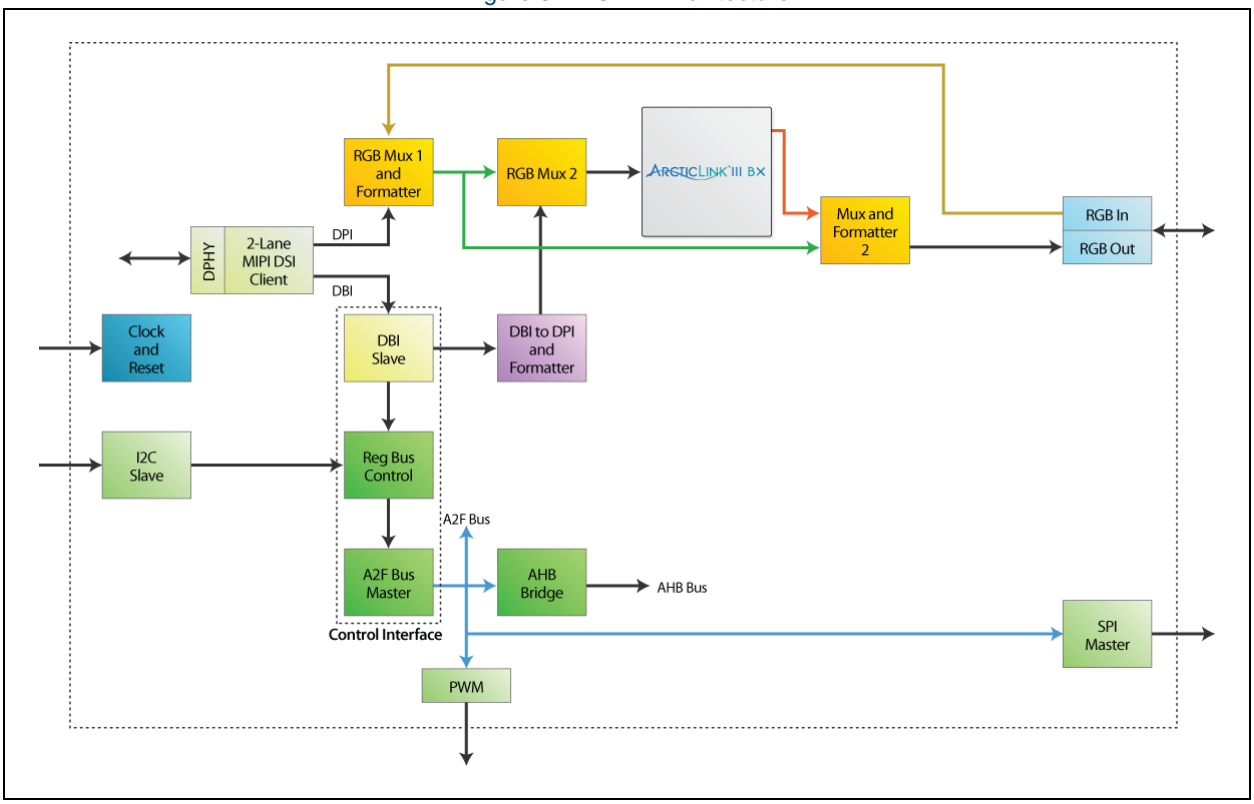
Control path input and outputs are:

- Input – I^2C and/or MIPI display bus interface (DBI)
- Output – SPI

Maximum resolution is 1920 x 1200 at 24 bpp at 60 fps. The speed is limited by MIPI bandwidth.

BX5B2A — MIPI-2 to RGB

Figure 6: BX5B2A Architecture



Use Case

Data path input and outputs are:

- Input – MIPI 2-lane
- Output – RGB

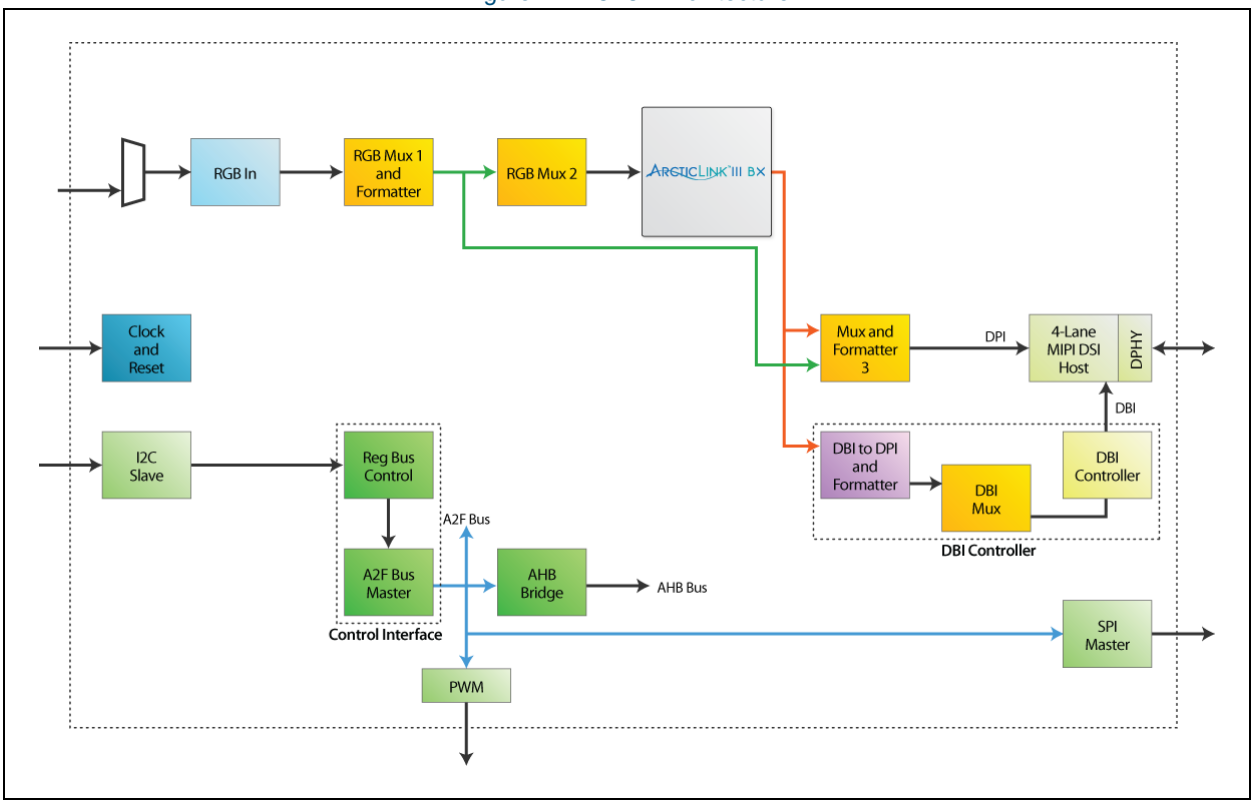
Control path input and outputs are:

- Input – I^2C and/or MIPI DBI)
- Output – SPI

Maximum resolution is 1366 x 768 at 24 bpp at 60 fps. The speed is limited by MIPI bandwidth.

BX5A3B — RGB to MIPI-4

Figure 7: BX5A3B Architecture



Use Case

Data path input and outputs are:

- Input – RGB
- Output – MIPI 4-lane

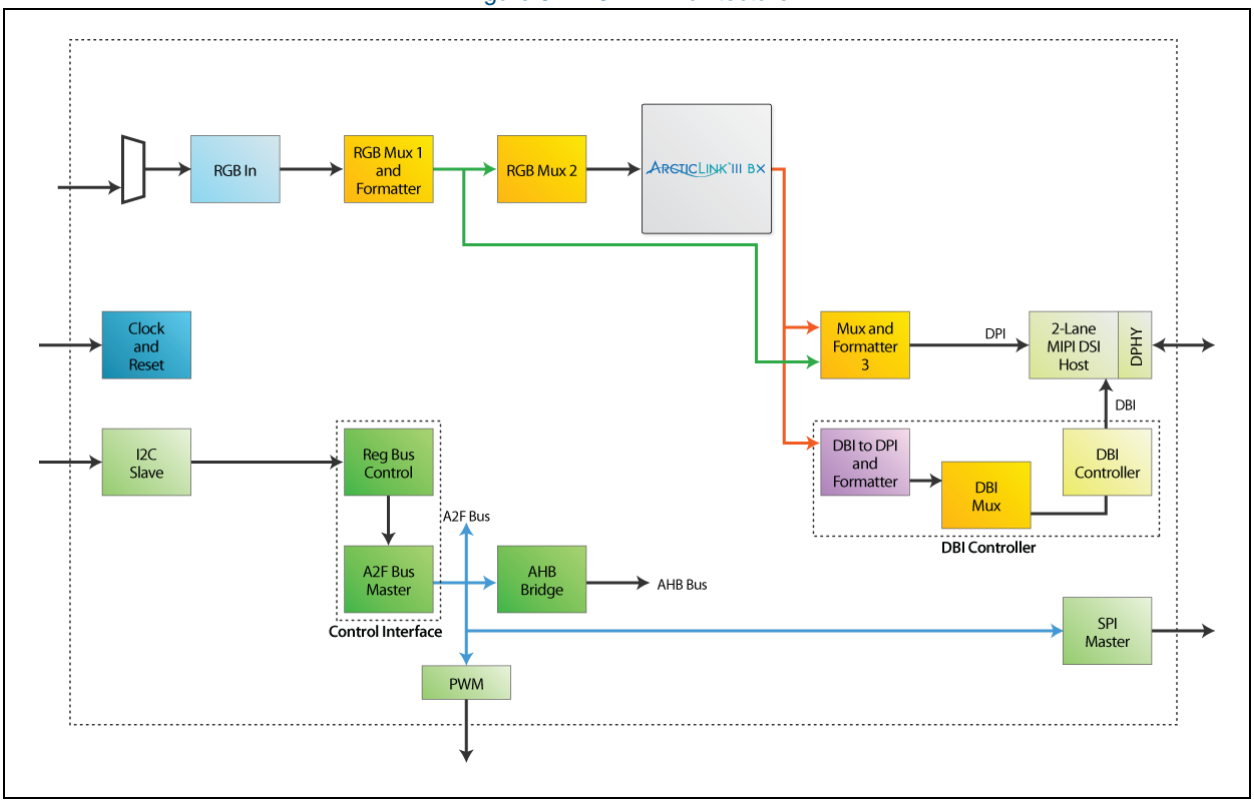
Control path input and outputs are:

- Input – I^2C
- Output – SPI and/or MIPI DBI

Maximum resolution is 1920 x 1200 at 24 bpp at 60 fps. The speed is limited by MIPI bandwidth.

BX5A2B — RGB to MIPI-2

Figure 8: BX5A2B Architecture



Use Case

Data path input and outputs are:

- Input – RGB
- Output – MIPI 2-lane

Control path input and outputs are:

- Input – I^2C
- Output – SPI and/or MIPI DBI

Maximum resolution is 1366 x 768 at 24 bpp at 60 fps. The speed is limited by MIPI bandwidth.

Power Consumption

Table 2 and **Table 3** shows the power consumption in various operating modes. The minimum PCLK possible is assumed for these measurements.

Table 2: BX5Axx Power Consumption (mW) at 60 fps[a]

Resolution	Display Width (pixels)	Display Height (pixels)	BX5A2B		BX5A3B[b]		BX5A1D		BX5A3D	
			18 bpp	24 bpp	18 bpp	24 bpp	18 bpp	24 bpp	18 bpp	24 bpp
QVGA	320	240	22.5	22.5	26.2	26.3	64.3	64.3	133.6	134.0
VGA	640	480	25.8	26.5	29.5	29.6	65.4	65.4	135.8	136.2
WVGA	854	480	27.7	28.6	30.8	30.9	65.8	65.8	136.7	137.1
PAL	768	576	28.7	29.6	31.3	31.4	66.0	66.0	137.1	137.5
SVGA	800	600	29.1	30.4	31.8	32.1	66.1	66.1	137.4	137.9
XGA	1,024	768	34.3	37.0	36.5	37.5	67.5	67.5	140.3	140.8
HD 720p	1,280	720	36.4	39.5	38.4	39.4	68.0	68.0	141.3	141.8
WXGA	1,366	768	38.7	42.1	40.5	41.6	-	-	142.5	142.9
SXGA	1,280	960	42.2	-	43.8	45.3	-	-	144.8	145.2
SXGA	1,280	1,024	43.9	-	44.9	46.6	-	-	145.5	146.0
SXGA+	1,400	1,050	46.0	-	46.9	48.5	-	-	146.6	147.1
UXGA	1,600	1,200	-	-	59.1	61.5	-	-	163.2	163.7
HD 1080	1,920	1,080	-	-	61.5	63.6	-	-	164.3	164.8
WUXGA	1,920	1,200	-	-	65.6	67.8	-	-	166.9	167.4

a. MIPI DBI command mode is limited to FWVGA (854x480) maximum.
b. Power measurement is shown with a 3.3 V RGB I/O. If a 1.8 V RGB I/O is used, power consumption drops approximately 5 mW at 1080P (1920x1080) resolution.

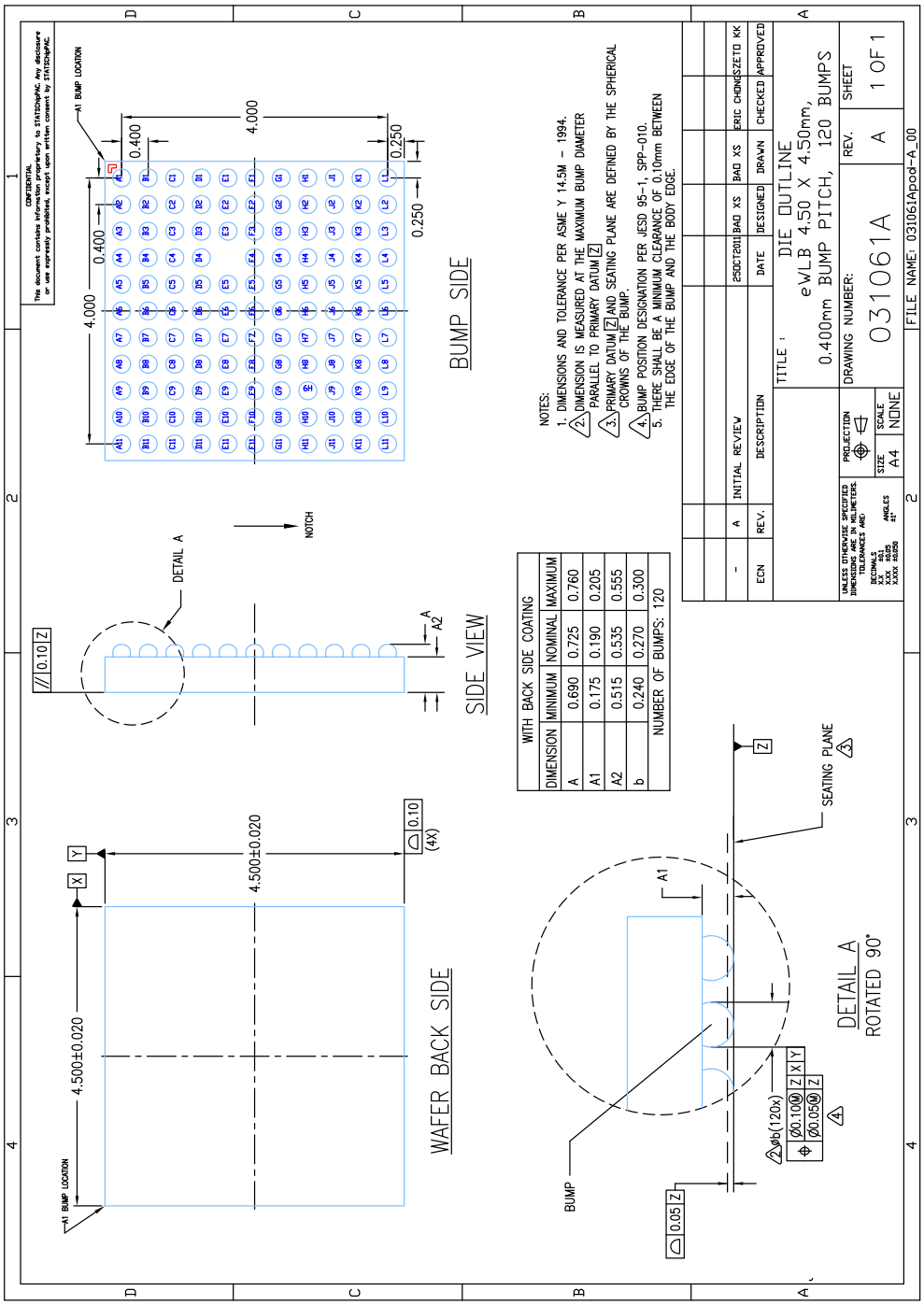
Table 3: BX5Bxx Power Consumption (mW) at 60 fps[a]

Resolution	Display Width (pixels)	Display Height (pixels)	BX5B2A		BX5B3A		BX5B1D		BX5B3D	
			18 bpp	24 bpp	18 bpp	24 bpp	18 bpp	24 bpp	18 bpp	24 bpp
QVGA	320	240	18.7	19.9	17.1	19.7	71.6	71.9	130.1	131.6
VGA	640	480	26.5	30.7	24.2	28.1	74.1	74.5	133.6	135.1
WVGA	854	480	29.7	34.4	27.1	31.4	75.1	75.6	136.5	138.6
PAL	768	576	31.3	36.2	28.6	33.1	75.6	76.1	135.9	137.4
SVGA	800	600	32.4	37.7	29.6	34.4	76.0	76.5	136.4	138.0
XGA	1,024	768	42.5	49.4	38.8	45.1	79.4	79.9	141.1	142.7
HD 720	1,280	720	46.3	53.9	42.3	49.2	80.5	81.2	142.8	144.4
WXGA	1,366	768	50.1	58.4	45.8	53.3	-	-	144.5	146.2
SXGA	1,280	960	57.1	-	52.1	60.7	-	-	148.0	149.6
SXGA	1,280	1,024	59.8	-	54.6	63.6	-	-	149.2	150.9
SXGA+	1,400	1,050	63.4	-	57.9	67.5	-	-	150.9	152.6
UXGA	1,600	1,200	-	-	70.4	82.1	-	-	157.9	175.7
HD 1080	1,920	1,080	-	-	74.1	86.5	-	-	174.2	177.8
WUXGA	1,920	1,200	-	-	80.8	94.2	-	-	177.9	181.5

a. MIPI DBI command mode is limited to FWVGA (854x480) maximum.

Mechanical Drawing

Figure 9: BX5 Solution Platform – CSSP 120 0.4 mm Ball (4.5 mm x 4.5 mm) WLCSP Mechanical Drawing



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Revision History

Revision	Date	Originator and Comments
1.0	October 2012	Initial production release.
1.1	July 2013	Paul Karazuba and Kathleen Bylsma – Updated Contact Information section. – Removed Thermal Characteristics page. – Updated maximum resolution for BX5A1D and BX5B1D to 1280 x 800.
1.2	July 2013	Paul Karazuba and Kathleen Bylsma Updated power consumption table for BX5A1D and BX5B1D.
1.3	June 2016	Brian Faith and Kathleen Bylsma Added QuickLogic Part Order Number to

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