Applications Overview

The ArcticLink III BX5 solution platform is a display interface bridge device enabling the connection of a RGB, MIPI 2-lane, or MIPI 4-lane processor with a RGB, MIPI 2-lane, MIPI 4-lane, LVDS 1-lane, or LVDS 2-lane display, with up to a maximum resolution of 1920x1200 (60 fps). Featuring a small 4.5 mm x 4.5 mm package, the ArcticLink III BX5 solution platform is a low power solution designed for smartphones and tablets.

Platform Highlights

Serial Peripheral Interface (SPI) Master
• Serial interface to control sensors, peripherals, and/or displays.

Onboard Clock Generation
• Integrated, very low power phase-locked loop (PLL) for generating the clocks.

I2C Client
• CPU interface for configuring and controlling internal registers and look-up tables (LUT).

Small Form Factor Packaging
• 120-ball, 4.5 mm x 4.5 mm WLCSP, 0.4 mm ball pitch.
ArcticLink III BX5 Solution Platform Variants

The ArcticLink III BX5 solution platform features eight distinct variants as described in Table 1.

Table 1: ArcticLink III BX5 Solution Platform Variants

<table>
<thead>
<tr>
<th>QuickLogic Part Order Number</th>
<th>CSSP Name</th>
<th>Device Input</th>
<th>Device Output</th>
<th>Max Resolution (60 FPS)</th>
<th>Primary Application</th>
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<tbody>
<tr>
<td>CSSP-BMFDN120</td>
<td>BX5B3D</td>
<td>MIPI-4\textsuperscript{a}</td>
<td>LVDS-2\textsuperscript{b}</td>
<td>1920 x 1200</td>
<td>Smartphones and tablet computers</td>
</tr>
<tr>
<td>CSSP-BPFDN120</td>
<td>BX5A1D</td>
<td>RGB</td>
<td>LVDS-1\textsuperscript{c}</td>
<td>1280 x 800</td>
<td>Smartphones and tablet computers</td>
</tr>
<tr>
<td>CSSP-BQFDN120</td>
<td>BX5A3D</td>
<td>RGB</td>
<td>LVDS-2</td>
<td>1920 x 1200</td>
<td>Smartphones and tablet computers</td>
</tr>
<tr>
<td>CSSP-BLFDN120</td>
<td>BX5B1D</td>
<td>MIPI-2\textsuperscript{d}</td>
<td>LVDS-1</td>
<td>1280 x 800</td>
<td>Smartphones and tablet computers</td>
</tr>
<tr>
<td>CSSP-BGFDN120</td>
<td>BX5B3A</td>
<td>MIPI-4</td>
<td>RGB</td>
<td>1920 x 1200</td>
<td>Smartphones and tablet computers</td>
</tr>
<tr>
<td>CSSP-BEFDN120</td>
<td>BX5B2A</td>
<td>MIPI-2</td>
<td>RGB</td>
<td>1366 x 768</td>
<td>Smartphones and tablet computers</td>
</tr>
<tr>
<td>CSSP-BJFDN120</td>
<td>BX5A3B</td>
<td>RGB</td>
<td>MIPI-4</td>
<td>1920 x 1200</td>
<td>Smartphones and tablet computers</td>
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<td>CSSP-BHFDN120</td>
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<td>RGB</td>
<td>MIPI-2</td>
<td>1366 x 768</td>
<td>Smartphones and tablet computers</td>
</tr>
</tbody>
</table>

\textsuperscript{a} MIPI-4: Four lane MIPI interface.
\textsuperscript{b} LVDS-2: Dual link LVDS interface (eight data differential pairs and two clock differential pairs).
\textsuperscript{c} LVDS-1: Single link LVDS interface (four data differential pairs and one clock differential pair).
\textsuperscript{d} MIPI-2: Two lane MIPI interface.
Data Paths

BX5B3D — MIPI-4 to LVDS-2

Use Case

Data path input and outputs are:
- Input – MIPI 4-lane
- Output – LVDS dual link (four data differential pairs and one clock differential pair)

Control path input and outputs are:
- Input – I²C
- Output – SPI

Maximum resolution is WUXGA (1920 x 1200) at 24 bpp at 60 fps. The speed is limited by LVDS bandwidth.
Use Case

Data path input and outputs are:

- Input – RGB
- Output – LVDS single link (four data differential pairs and one clock differential pair)

Control path input and outputs are:

- Input – I2C
- Output – SPI

Maximum resolution is 1280 x 800 at 24 bpp at 60 fps. The speed is limited by LVDS bandwidth, and resolution is dependent on display blanking and pixel clock.
BX5A3D — RGB to LVDS-2

Use Case

Data path input and outputs are:
- Input – RGB
- Output – LVDS dual link (eight data differential pairs and two clock differential pairs)

Control path input and outputs are:
- Input – I2C
- Output – SPI

Maximum resolution is 1920 x 1200 at 24 bpp at 60 fps. The speed is limited by LVDS bandwidth.
Use Case

Data path input and outputs are:

- Input – MIPI 2-lane
- Output – LVDS single link (four data differential pairs and one clock differential pair)

Control path input and outputs are:

- Input – I2C and/or MIPI display bus interface (DBI)
- Output – SPI

Maximum resolution is 1280 x 800 at 24 bpp at 60 fps. The speed is limited by LVDS bandwidth, and resolution is dependent on display blanking and pixel clock.
BX5B3A — MIPI-4 to RGB

Use Case

Data path input and outputs are:

- Input – MIPI 4-lane
- Output – RGB

Control path input and outputs are:

- Input – I²C and/or MIPI display bus interface (DBI)
- Output – SPI

Maximum resolution is 1920 x 1200 at 24 bpp at 60 fps. The speed is limited by MIPI bandwidth.
**Use Case**

Data path input and outputs are:

- **Input** – MIPI 2-lane
- **Output** – RGB

Control path input and outputs are:

- **Input** – I²C and/or MIPI DBI)
- **Output** – SPI

Maximum resolution is 1366 x 768 at 24 bpp at 60 fps. The speed is limited by MIPI bandwidth.
**Use Case**

Data path input and outputs are:

- Input – RGB
- Output – MIPI 4-lane

Control path input and outputs are:

- Input – I²C
- Output – SPI and/or MIPI DBI

Maximum resolution is 1920 x 1200 at 24 bpp at 60 fps. The speed is limited by MIPI bandwidth.
**Use Case**

Data path input and outputs are:

- **Input** – RGB
- **Output** – MIPI 2-lane

Control path input and outputs are:

- **Input** – I²C
- **Output** – SPI and/or MIPI DBI

Maximum resolution is 1366 x 768 at 24 bpp at 60 fps. The speed is limited by MIPI bandwidth.
Power Consumption

Table 2 and Table 3 shows the power consumption in various operating modes. The minimum PCLK possible is assumed for these measurements.

Table 2: BX5Axx Power Consumption (mW) at 60 fps

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<th></th>
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<td>320</td>
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</table>

a. MIPI DBI command mode is limited to FWVGA (854x480) maximum.

b. Power measurement is shown with a 3.3 V RGB I/O. If a 1.8 V RGB I/O is used, power consumption drops approximately 5 mW at 1080P (1920x1080) resolution.
### Table 3: BX5Bxx Power Consumption (mW) at 60 fps\(^a\)

<table>
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<tr>
<th>Resolution</th>
<th>Display Width (pixels)</th>
<th>Display Height (pixels)</th>
<th>BX5B2A 18 bpp</th>
<th>BX5B2A 24 bpp</th>
<th>BX5B3A 18 bpp</th>
<th>BX5B3A 24 bpp</th>
<th>BX5B1D 18 bpp</th>
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<td>75.6</td>
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<td>177.9</td>
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</table>

\(^a\) MIPI DBI command mode is limited to FWVGA (854x480) maximum.
Figure 9: BX5 Solution Platform – CSSP 120 0.4 mm Ball (4.5 mm x 4.5 mm) WLCSP Mechanical Drawing
Contact Information

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Japan-sales@quicklogic.com
Korea-sales@quicklogic.com

Support: www.quicklogic.com/support
Internet: www.quicklogic.com

Revision History

<table>
<thead>
<tr>
<th>Revision</th>
<th>Date</th>
<th>Originator and Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0</td>
<td>October 2012</td>
<td>Initial production release.</td>
</tr>
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</table>
| 1.1      | July 2013  | Paul Karazuba and Kathleen Bylsma
– Updated Contact Information section.
– Removed Thermal Characteristics page.
– Updated maximum resolution for BX5A1D and BX5B1D to 1280 x 800. |
| 1.2      | July 2013  | Paul Karazuba and Kathleen Bylsma
Updated power consumption table for BX5A1D and BX5B1D.                                |
| 1.3      | June 2016  | Brian Faith and Kathleen Bylsma
Updated QuickLogic Part Order Number to                                                  |

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