

ArcticPro

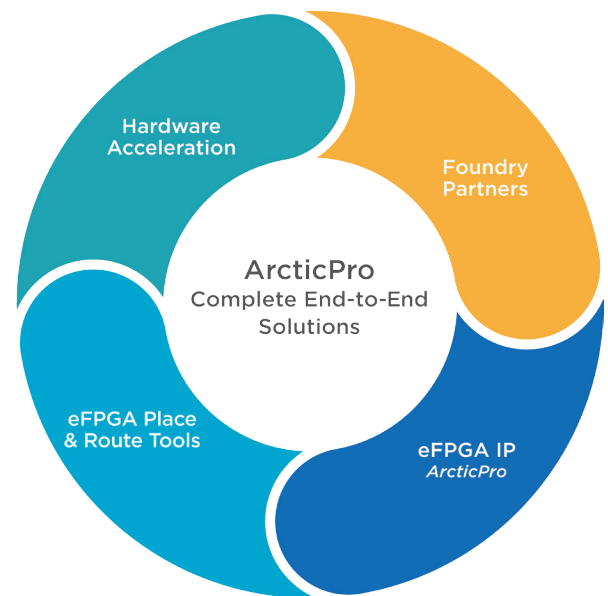
Build Flexibility and Differentiation Into Your Next Low Power SoC

With over 30 years of programmable logic device, software and IP experience, QuickLogic is the world's leading developer of low-cost, ultra-low power, high-performance embedded FPGA (eFPGA) solutions. The company's ArcticPro eFPGA technology enables SoC designs to be customized post-production without expensive and time-consuming redesign - allowing developers to easily address rapidly evolving market requirements, support emerging standards, and address multiple applications with a single mask set.

The QuickLogic Solution

ArcticPro™ 3 eFPGA IP on Samsung Foundry 28FDS® (FD-SOI) Process

The ArcticPro 3 embedded FPGA (eFPGA) technology is the industry's first on the Samsung Foundry 28FDS® (FD-SOI) process. ArcticPro is already supported in 65nm and 40nm CMOS manufacturing processes. QuickLogic's ultra-low power eFPGA architecture and mature software offer SoC designers an easy-to-integrate, highly reliable and extremely low power eFPGA IP. Designers can now create multiple chip variants from a single mask set post-manufacturing, enabling their device to address fragmented or rapidly evolving markets and/or emerging standards.



eFPGA Design Tools

- **Aurora: IP Creation Tool**

- During the SoC integration phase, we provide an intuitive way to define your eFPGA array and port mappings

- **SymbiFlow: Open Source Development Software**

- Including Synthesis, Place & Route and bitstream generation
- Compatible with industry-standard simulators
- Back annotated timing data for performance analysis
- Power calculator

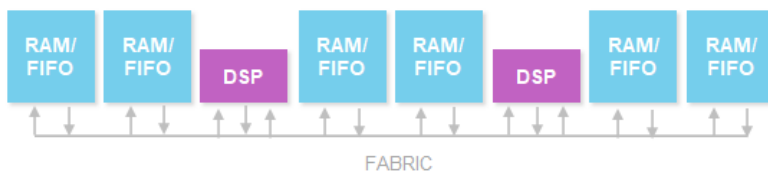
- **Benefits:**

- Easy to use and with a large community of users and developers
- Access to the source code for fast customizations and feature improvements
- Ability to integrate into your own tool suite

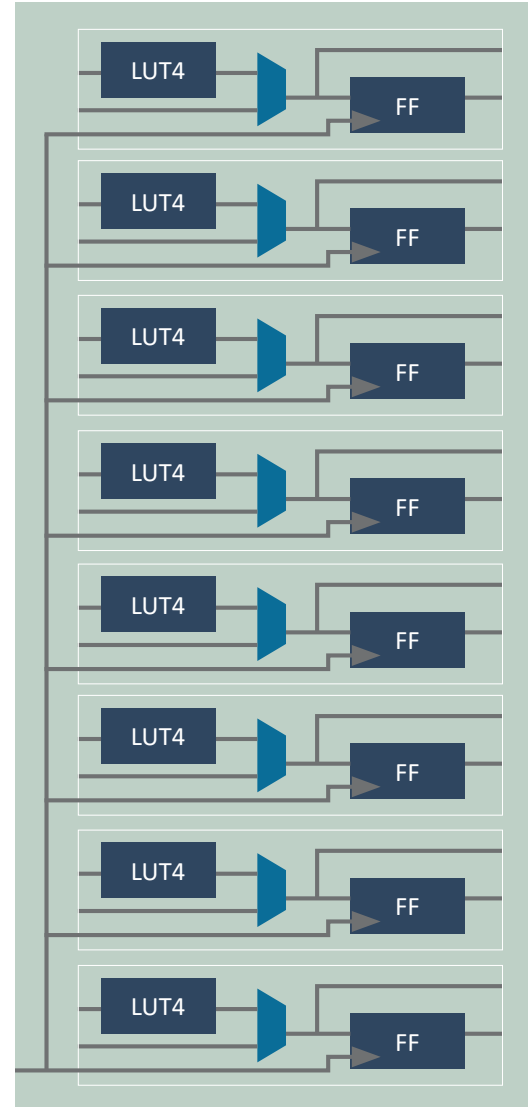
ArcticPro 3 eFPGA Technology

High-performance architecture for low power applications

- **Homogenous fabric architecture**
 - Super Logic Cell (SLC) consists of 8 LUT4
 - 8 registers
- **Hierarchical routing networks for optimum performance and power consumption**
 - Multiple outputs per logic cell are strategically selected to either feedback within the same SLC or to travel out to another SLC. A shared register clock, and set/reset signal for all four logic cells helps reduce routing congestion
 - Two carry-in muxes per logic cell allow each logic cell to function as a 2-bit adder, which results in an 8-bit adder per SLC
- **Flexible flip flop**
 - Flip flop can be driven by combinatorial logic in the cell
 - Flip flop can be used independently of the combinatorial logic in the cell
- **Array sizes ranging from 8x8 SLC up to 64x64 SLC**
- **Built-in block RAM and Multiplier-Accumulates (MACs)**



Integrated RAM, FIFO, and DSP capability for improved performance of computationally intensive applications (Example: ML & AI)



Super Logic cell (SLC) Architecture



For more information about QuickLogic, please visit www.quicklogic.com

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