QuickLogic® ArcticLink® III VX and BX CSSPs – Passive Components Reduction Guide

QuickLogic Application Note 98

Introduction

The use of discrete passive components in electronic systems continues to increase, due to a high degree of system integration, as well as the demand for high-speed operation. With limited printed circuit board (PCB) real-estate available for complex system functionality, reduction in passive component count is required.

This document describes the QuickLogic ArcticLink III VX and/or BX Customer Specific Standard Products (CSSPs) requirements and technical challenges to consider when removing components.

This document is divided into two sections:

- Capacitor functions (such as decoupling, bypassing and bulk) and using ferrite components in the power isolation.
- Consideration for components that can be removed from ArcticLink III VX/BX CSSP designs.

Passive Components in ArcticLink III VX/BX CSSP Systems

Capacitors

Decoupling

Decoupling capacitors are used throughout the board design. These capacitors assist in preventing the ArcticLink III VX/BX CSSP from injecting RF frequency into the power distribution network during high-speed switching. Capacitors also provide a localized source of DC power for the ArcticLink III VX/BX CSSP, which reduces peak current surges propagated across the printed circuit board. These capacitors match with fast edge transition during switching operations. The provision of these devices is a necessity due to EMI analysis. During EMC testing, the number of capacitors can be reduced, but cannot be added.

NOTE: Analysis of optimum placement for these components is not within the scope of this document.

Bypassing

Bypassing capacitors are provided to divert unwanted common-mode RF noise from the ArcticLink III VX/BX CSSP coupling to other nearby logics. The bypass capacitor is essential in creating an AC shunt to remove undesired energy from entering the susceptible areas, in addition to providing other functions of filtering.

Bulk

Bulk capacitors are provided to maintain constant DC voltage and current levels to the ArcticLink III VX/BX CSSP when a high number of signal pins switch simultaneously under maximum capacitive load. These capacitors also prevent power drop-out due to high current demand in a short time (dI/dT) by the ArcticLink III VX/BX CSSP.

Ferrite

Ferrite devices attenuate RF energy. Often, the ferrite is used to prevent parasitic oscillations or unwanted signal coupling travelling along component leads or inter-connect traces. In an EMI application, the ferrite core is used to eliminate or reduce high-frequency RF currents from EMI sources to contaminate neighboring circuitries. In the ArcticLink III VX/BX CSSP, ferrite is used to:

- Suppress device switching frequency from escaping into the board power plane.
- Isolate the source of high frequency energy.
- Work together with a capacitor to provide a low-pass filter that is inductive-capacitive at desirable low frequencies and dissipative at high frequencies.

Considerations for Removal of Required Passive Components

Removing Capacitors

The current recommended capacitors for the ArcticLink III VX/BX CSSP are proven and successfully implemented in several designs. While it is possible to reduce the number of required capacitors, the system designer must consider the following:

- Isolating various ArcticLink III VX/BX CSSP power planes from the rest of the system to prevent noise coupling to neighboring circuits. Noise from power supplies will affect the performance of various PLL circuits.
- Maintaining a minimum of one 2.2 µF, one 0.1 µF and one 0.001 µF for the ArcticLink III VX/BX CSSP core power supplies.
- Using the plane or very thick power traces to prevent a significant voltage drop on I/Os and functional blocks resulting in a fault-trigger. See **Power and Ground Plane** on page 3 to replace capacitors for noise filtering between 30 MHz to 400 MHz.

Power and Ground Plane

A benefit of using multi-layer assemblies is the ability to have a power and ground plane distributed network to enhance the overall performance of system operations. The performance is achieved by having a low-impedance path between the power source and component. A low-impedance path allows for a minimal amount of voltage drop to be present for the overall assembly, power supply to components, and component to component. The physical relationship between the two planes creates one large capacitor, two parallel plates separated by a dielectric. This capacitor provides adequate decoupling for most low-speed (slow edge rate) designs. However, additional layers add cost to the overall PCB assembly.

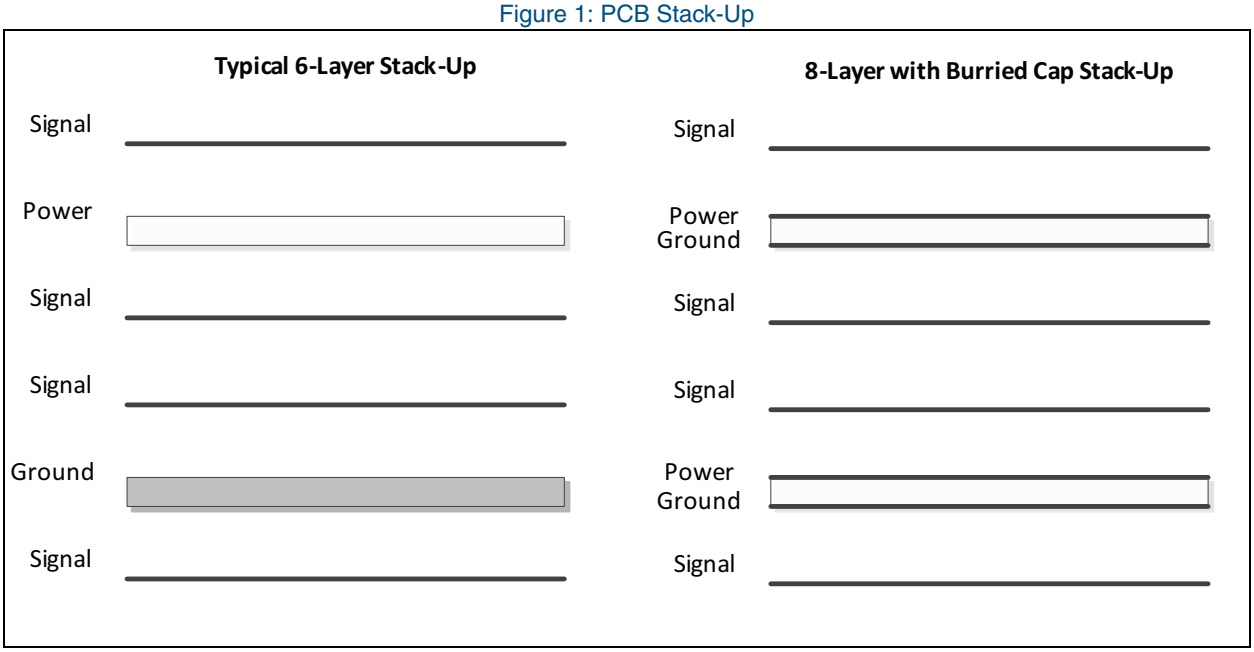
Depending on the thickness of the core material, the dielectric constant value, and the placement of the planes within a board stack-up, various values of capacitance can exist. Network analysis, mathematical calculations or modeling will reveal the actual capacitance of the power and ground plane structure. Proper analysis is required to determine the total impedance of the complete PCB, including the effects of these planes and all of the discreet decoupling capacitors.

NOTE: In-depth analysis of PCB implementation and calculation of these planes is not within the scope of this document.

For a highly dense system, buried capacitance technology must be considered. Buried capacitance is special manufacturing process that has a 0.001-inch dielectric. With this small dielectric, decoupling is effective up to ~300 MHz. The use of discrete capacitors may not be necessary when buried capacitance is used. With fewer discrete devices, less inrush surge current is required, which is beneficial to minimizing board-induced noise voltage, ground bounce, and development of common-mode energy. One draw-back of a buried capacitance technology board is the low dielectric break-down voltage, which is not ideal in a high voltage application.

Figure 1 illustrates the stack-up of these planes.

Figure 1: PCB Stack-Up



Removing Ferrites

Ferrites are used throughout the design to isolate various PLL circuitries from injecting noise into the system supplies, as well as a way to control RF energy. This is critical for EMC testing. During design and debug, the benefits of using ferrites are not obvious. However, during EMI/EMC testing, this can be a determining failure factor that can result in spinning a new PCB. Considerations for removing ferrites are as follows:

- EMC design and testing; the system designer must review the system design to ensure product shielding and design layout minimize emission.

  NOTE: Methods of EMC design are not within the scope of this document.

- Power supplies must have very low noise ripples that are within specifications for proper PLL operation.

See **Specific Use-Case Listings for Removal** on page 4 for more detail.

Removing Resistors

Resistors provide flexibility in system design. The stuff option allows the designer to configure the ArcticLink III VX/BX CSSP differently for different test modes. These are extremely useful during prototype system debug. Once the design is proven, the stuff options can be removed. Some configuration resistors are mandatory and must be included. See **Specific Use-Case Listings for Removal** on page 4 for removal options for a specific use-case.

Specific Use-Case Listings for Removal

The listings in **Table 1** through **Table 5** are based on the ArcticLink III VX/BX CSSP schematic revision 1.2.

While it is possible to perform parts reduction, QuickLogic recommends that the designer implement the full schematic as is. Removal of parts can be executed during EMC testing to achieve final parts count. Without proper parts in place, adjustment/fine-tuning for EMC testing is very difficult.

NOTE: All components listed in each table are candidates for removal. It is up to the designer's discretion to determine which components will be removed. All other passive components in the schematic are required.

MIPI → MIPI (VX3BxB, BX3BxB, VX6BxE and BX6BxE Only)

Table 1: MIPI → MIPI Reduction

Component	Pin	Function	Note
L1, C1, C2, C3	F9	MIPI RX PLL filter	Required low noise on P1V2 supply (±5%); EMC consideration required. QuickLogic recommends using planes.
C4, C5, C6, C7	F8, C7, C8	MIPI RX IO supply	Required low noise on P1V2 supply (±5%). QuickLogic recommends using planes.
L2, C10, C9, C8	J7	MIPI TX PLL filter	Required low noise on P1V2 supply (±5%); EMC consideration required. QuickLogic recommends using planes.
C14, C13, C12, C11	G8, G6, H9	MIPI TX IO supply	Required low noise on P1V2 supply (±5%). QuickLogic recommends using planes.
R1	L1	SYS_CLK pull-down	This resistor provides stable clock at low level to ensure proper VX/BX operation. This signal must be stable during the power-on/reset condition. If system design can ensure stability of signal during power-on/reset; it can be removed.
R2	K1	RESET pull-down	This resistor provides stable reset at low level to ensure proper VX/BX operation. This signal must be stable during the power-on/reset condition. If system design can ensure stability of signal during power-on /reset; it can be removed.
C15	G5	L1 and K1 IO supply	Required low noise on IO supply. QuickLogic recommends using thick-trace or planes.
C17, C18	J4	VX/BX PLL supply	Required low noise on P1V2 supply (±5%). QuickLogic recommends using planes.
R9, R10	B11	LP Clock divider	During prototype initialization, the designer can adjust the default LP clock to ensure proper operation between MIPI Host and MIPI Client. Once a configuration is selected, the resistors can be removed.
R4, R5, R11, R12, R13	D11, D10, E11, E10, E9	GPIO	While the IO is unused, the resistors allow debugging software to toggle the pins. Do not leave these pins open (default are inputs). Tie the pins to GND. Note: the software cannot configure these pins to output.
C32, C34	D9	GPIO4/5/0/1 supply	Requires stable low noise P1V8.
C35, C41	E8	GPIO2/3/6/7/8 supply	Requires stable low noise P1V8/P2V5/P3V3.
C20, C21, C23, C24	VX/BX Core	VDD	Requires plane to provide stable and low-drop supplies.

RGB → LVDS (VX5AxD and BX5AxD Only)

Table 2: RGB → LVDS Reduction

Component	Pin	Function	Note
R1	L1	SYS_CLK pull-down	This resistor provides a stable clock at low level to ensure proper VX/BX operation. This signal must be stable during the power-on/ reset condition. If the system design can ensure stability of signal during power-on/reset, it can be removed.
R2	K1	RESET pull-down	This resistor provides stable reset at low level to ensure proper VX/BX operation. This signal must be stable during the power-on/ reset condition. If the system design can ensure stability of signal during power-on/reset, it can be removed.
C15	G5	L1 and K1 IO supply	Required low noise on IO supply. QuickLogic recommend using thick-trace or planes.
C17, C18	J4	VX/BX PLL supply	Required low noise on P1V2 supply (±5%). QuickLogic recommends using planes.
R7, R8	A11	Sys Clk selection	Use during debug; the designer can remove the resistor and hardwire the IO using final configuration.
R9, R10	B11	LP Clock Divider	Signal can be tied high or low.
R4, R5, R11, R12, R13	D11, D10, E11, E10, E9	GPIO	While the IO is unused, the resistors allow debug software to toggle the pins. Do not leave these pins open (default are inputs). Tie the pins to GND. Note: The software cannot configure these pins to output.
C32, C34	D9	GPIO4/5/0/1 supply	Requires stable low noise P1V8.
C35, C41	E8	GPIO2/3/6/7/8 supply	Requires stable low noise P1V8/P2V5/P3V3.
C20, C21, C23, C24	VX/BX Core	VDD	Requires plane to provide stable and low-drop supplies.
C29, C30, C31	H7, D4	RGB IO supply	Required low noise on this supply. QuickLogic recommends using planes.
C26, C27, C28	D3, F3, G4	LVDS IO supply	Required low noise on this supply. QuickLogic recommends using planes.

RGB → MIPI (VX5AxB and BX5AxB Only)

Table 3: RGB → MIPI Reduction

Component	Pin	Function	Note
L2, C10, C9, C8	J7	MIPI TX PLL filter	Required low noise on P1V2 supply (±5%); EMC consideration required. Recommend to use planes
C14, C13, C12, C11	G8, G6, H9	MIPI TX IO supply	Required low noise on P1V2 supply (±5%). QuickLogic recommends using planes.
R1, R2	L1, K1	SYS_CLK pull-down RESET pull-down	This resistor provides stable clock and reset at low level to ensure proper VX/BX operation. This signal must be stable during the power-on/reset condition. If the system design can ensure stability of signal during power-on/reset, it can be removed.
C15	G5	L1 and K1 IO supply	Required low noise on IO supply. QuickLogic recommends using thick-trace or planes.
C17, C18	J4	VX/BX PLL supply	Required low noise on P1V2 supply (±5%). QuickLogic recommends using planes.
R9, R10	B11	LP Clock Divider	During prototype initialization, the designer can adjust the default LP clock to ensure proper operation between the MIPI Host and MIPI Client. Once a configuration is selected, the resistors can be removed.
R4, R5, R11, R12, R13	D11, D10, E11, E10, E9	GPIO	While the IO is unused, the resistors allow the debug software to toggle the pins. Do not leave these pins open (default are inputs). Tie the pins to GND. Note: The software cannot configure these pins to output.
C32, C34	D9	GPIO4/5/0/1 supply	Requires stable low noise P1V8.
C35, C41	E8	GPIO2/3/6/7/8 supply	Requires stable low noise P1V8/P2V5/P3V3.
C29, C30, C31	H7, D4	RGB IO supply	Required low noise on this supply. QuickLogic recommends using planes.
C20, C21, C23, C24	VX/BX Core	VDD	Requires plane to provide stable and low-drop supplies.

MIPI → LVDS (VX5BxD and BX5BxD Only)

Table 4: MIPI → LVDS Reduction

Component	Pin	Function	Note
L1, C1, C2, C3	F9	MIPI RX PLL filter	Required low noise on P1V2 supply (±5%); EMC consideration required. QuickLogic recommends using planes.
C4, C5, C6, C7	F8, C7, C8	MIPI RX IO supply	Required low noise on P1V2 supply (±5%). QuickLogic recommends using planes.
R1, R2	L1, K1	SYS_CLK pull-down RESET pull-down	This resistor provides stable clock and reset at low level to ensure proper VX/BX operation. This signal must be stable during the power-on/reset condition. If the system design can ensure stability of signal during power-on/reset, it can be removed.
C15	G5	L1 and K1 IO supply	Required low noise on IO supply. QuickLogic recommends using thick-trace or planes.
C17, C18	J4	VX/BX PLL supply	Required low noise on P1V2 supply (±5%). QuickLogic recommends using planes.
R9, R10	B11	LP Clock Divider	During prototype initialization, the designer can adjust the default LP clock to ensure proper operation between the MIPI Host and MIPI Client. Once a configuration is selected, the resistors can be removed.
R4, R5, R11, R12, R13	D11, D10, E11, E10, E9	GPIO	While the IO is unused, the resistors allows the debug software to toggle the pins. Do not leave these pins open (default are inputs). Tie the pins to GND. Note: The software cannot configure these pins to output.
C32, C34	D9	GPIO4/5/0/1 supply	Requires stable low noise P1V8.
C36, C45	E8	GPIO2/3/6/7/8 supply	Requires stable low noise P1V8/P2V5/P3V3.
C26, C27, C28	D3, F3, G4	LVDS IO supply	Required low noise on this supply. QuickLogic recommends using planes.
C20, C21, C23, C24	VX/BX Core	VDD	Requires plane to provide stable and low-drop supplies.

MIPI → RGB (VX5BxA and BX5BxA Only)

Table 5: MIPI → RGB Reduction

Component	Pin	Function	Note
L1, C1, C2, C3	F9	MIPI RX PLL filter	Required low noise on P1V2 supply (±5%); EMC consideration required. QuickLogic recommends using planes.
C4, C5, C6, C7	F8, C7, C8	MIPI RX IO supply	Required low noise on P1V2 supply (±5%). QuickLogic recommends using planes.
R1, R2	L1, K1	SYS_CLK pull-down RESET pull-down	This resistor provides stable clock and reset at low level to ensure proper VX/BX operation. This signal must be stable during the power-on/reset condition. If the system design can ensure stability of signal during power-on reset, it can be removed.
C15	G5	L1 and K1 IO supply	Required low noise on IO supply. QuickLogic recommends using thick-trace or planes.
C17, C18	J4	VX/BX PLL supply	Required low noise on P1V2 supply (±5%). QuickLogic recommends using planes.
R9, R10	B11	LP Clock Divider	During prototype initialization, the designer can adjust the default LP clock to ensure proper operation between the MIPI Host and MIPI Client. Once a configuration is selected, the resistors can be removed.
R4, R5, R11, R12, R13	D11, D10, E11, E10, E9	GPIO	While the IO is unused, the resistors allow the debug software to toggle the pins. Do not leave these pins open (default are inputs). Tie the pins to GND. Note: The software cannot configure these pins to output.
C32, C34	D9	GPIO4/5/0/1 supply	Requires stable low noise P1V8.
C41, C42	E8	GPIO2/3/6/7/8 supply	Requires stable low noise P1V8/P2V5/P3V3.
C29, C30, C31	H7, D4	RGB IO supply	Required low noise on this supply. QuickLogic recommends using planes.
C20, C21, C23, C24	VX/BX Core	VDD	Requires plane to provide stable and low-drop supplies.

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Revision History

Revision	Date	Originator and Comments
A	September 2012	Anthony Le and Kathleen Bylsma

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