CSSP Specification for Customer Name

ArcticLink® III BX5B3D Device Data Sheet

Revision 1.7

Ordering Information

Package	Part Number
120-ball FOWLCSP	CSSP-BMFDN120-xxxx

CONFIDENTIAL

ArcticLink® III BX5B3D Device Data Sheet

Platform Highlights

Serial Peripheral Interface (SPI) Master

- Serial interface to control sensors, peripherals, and/or displays.

Onboard Clock Generation

- Integrated, very low power phase-locked loop (PLL) for generating the clocks.

I^2C Client

- CPU interface for configuring and controlling internal registers and look-up tables (LUT).

Small Form Factor Packaging

- 120-ball, 4.5 mm x 4.5 mm WLCSP, 0.4 mm ball pitch.

Applications Overview

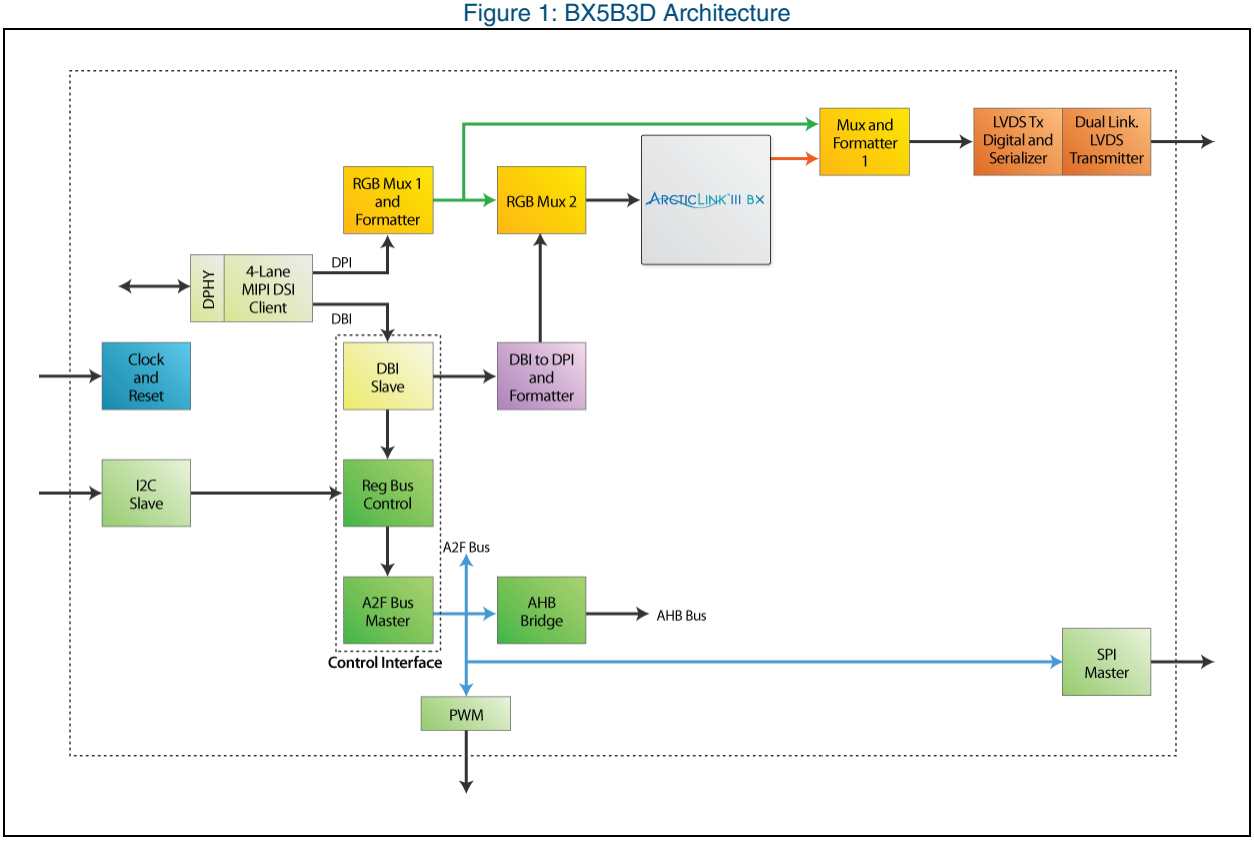
The ArcticLink III BX5B3D device is a display interface bridge device enabling the connection of a MIPI 4-lane processor with a LVDS 2-lane display, with up to a maximum resolution of 1920x1200 (60 fps). Featuring a small 4.5 mm x 4.5 mm package, the ArcticLink III BX5B3D device is a low power solution designed for smartphones and tablets.

Data Paths

CAUTION: MIPI video mode must be used for video on the ArcticLink III BX5 device, as MIPI command mode is not supported for video data. However, MIPI command mode can be used to write register settings on the ArcticLink III BX5 device.

BX5B3D — MIPI-4 to LVDS-2

Figure 1: BX5B3D Architecture



Use Case

Data path input and outputs are:

- Input – MIPI 4-lane
- Output – LVDS dual link (four data differential pairs and one clock differential pair)

Control path input and outputs are:

- Input – I^2C
- Output – SPI

Maximum resolution is WUXGA (1920 x 1200) at 24 bpp at 60 fps. The speed is limited by LVDS bandwidth.

ArcticLink III BX5B3D Device Modules

Control Interface Module

Figure 2 shows the Control Interface Module.

Figure 2: Control Interface Module

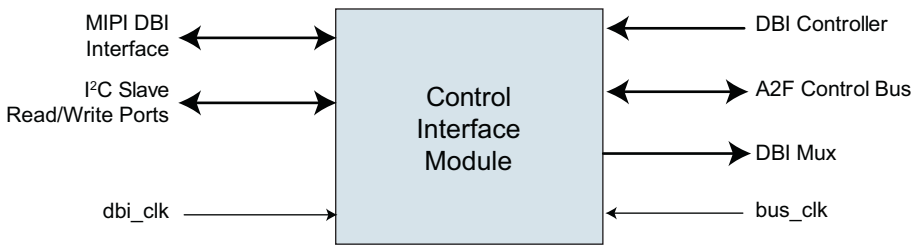


Table 1 shows the A2F bus address map of the ArcticLink III BX5 device.

Table 1: A2F Bus Address Map

Module	Start Address [11:0]	End Address [11:0]
MIPI DSI Client (through A2F to AHB bridge)	0x200	0x2FF
SPI Master	0x000	0x0FF
Common Registers in the Control Interface Module (for I²C Slave, PWM, Use Case selection, Clock and Reset Controller and Error handling)	0x100	0x1FF
Clock and Reset (see **Clock and Reset Registers** on page 32)	0x700	0xFFF

The Control Interface Module allows the external host to access the internal Vx registers through I²C or the MIPI Client interface. MIPI command packets are passed on the Control Interface Module through an internal DBI bus. MIPI generic commands can be used to access internal Vx registers using a programmable command format.

The following are DCS commands:

- *set_address_mode*
- *set_pixel_format*
- *set_column_address*
- *set_page_address*
- *write_memory_start*
- *write_memory_continue*

Note that *set_column_address* and *set_page_address* indicate a full frame when the secondary video input MIPI Rx DBI is enabled. Also, the *write_memory_start* and *write_memory_continue* commands must carry at least one line of data or any integer number of lines in case secondary video input MIPI Rx DBI is enabled. Avoid decoding the *set_column_address* and *set_page_address* commands if the system host can configure the resolution.

Another special DCS command set that must be handled is:

- *set_tear_on*
- *set_tear_scanline*
- *set_tear_off*
- *enter_sleep_mode* (for shutdown)
- *exit_sleep_mode*
- *enter_idle_mode* (for color mode])
- *exit_idle_mode*

This special DCS command set is treated the same as any other forward commands to an external display device through SPI, the only difference is that the *TE* signal of the client DBI interface is driven with that of the host. Although these are direct connections, the client has the option to configure masks independently. Apart from this, *TE* and *SD-in/out* signals are driven out by multiplexing with the general purpose input/output (GPIO). The *SD-in/out* multiplexed signals, incoming *SD* signal, and outgoing *SD* signal must have the option to invert at configuration.

The registers of I^2C Slave, PWM, Use Case selection, Clock and Reset Controller and Error handling are located in the Control Interface Module and are routed to respective modules. Since there are only a few registers in the blocks and some of the registers are needed in multiple blocks, they are centrally located rather than independent modules decoding from the A2F bus. Only I^2C or MIPI DBI is allowed to access the registers and not both simultaneously.

MIPI Display Serial Interface (DSI) Client

MIPI DSI Rx has up to four data lanes (4 Gbps total) and is in compliance with *MIPI DSI Specification Version 1.02* supporting video mode and command mode with display pixel interface (DPI) (DPI-2 v2.00) and DBI (DBI-2 v2.00). The MIPI D-PHY is in compliance with MIPI D-PHY *Specification Version 1.0.*

MIPI DSI Rx forward DPI traffic includes DPI to RGB. DBI traffic support is included as well as generic write and limited digital command system (DCS) commands to the local ArcticLink III BX5 device registers. MIPI DSI Rx reverse DBI traffic includes generic reads from the local ArcticLink III BX5 device registers and read commands.

The ArcticLink III BX5 device supports the following features:

- Video mode and command mode
- Multiple packets per transmission
- Continuous and noncontinuous clock behavior on clock lanes
- Ultra low power state (ULPS) mode
- Acknowledge packets and trigger messages
- Reverse low power transmission and reception
- All generic read/write, short and long packets
- All DCS commands
- Switching to ultra low power mode
- Bus turn around

- Switching to low power mode
- Programmable Error Injection and Detection
- Data lanes configurable up to four
- End of transmission (EOT), error-correcting code (ECC) and cyclic redundancy checking (CRC) enable/disable mechanisms
- Recovery due to contention
- Generic parallel interface for sending and receiving vendor specific information to display unit
- DPI interface for sending pixel data to display unit
- One virtual channel for video mode
- One virtual channel for command mode

MIPI Client Timing

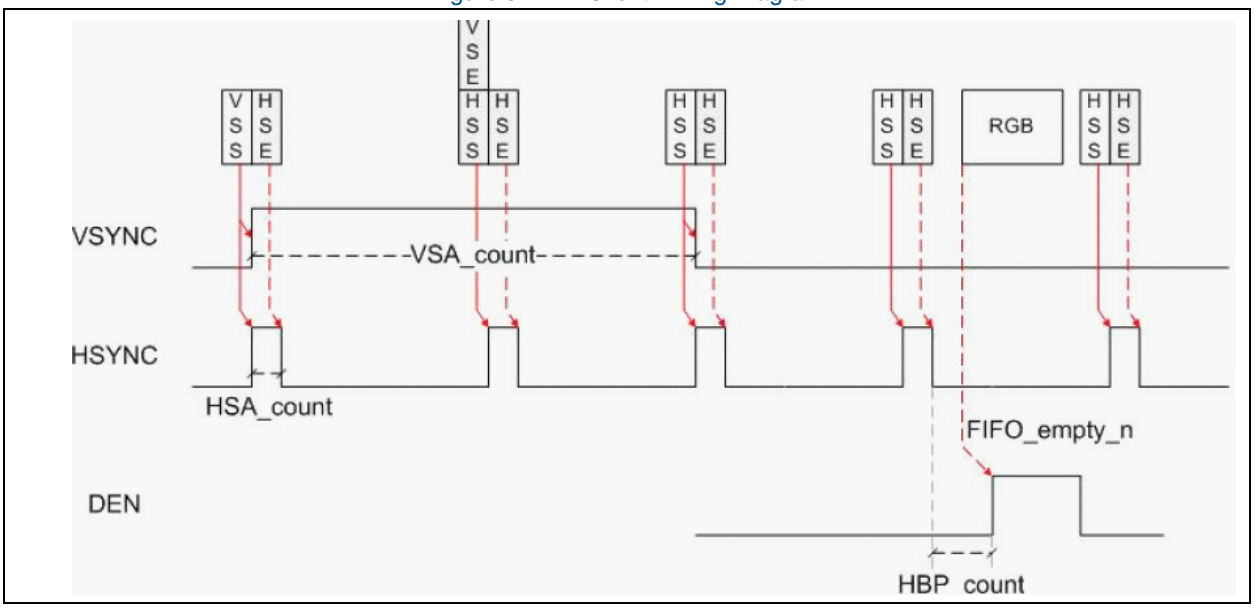
Table 2 describes the MIPI Client timing.

Table 2: MIPI Client IP

Constraint	Description	Value	Unit	Dependencies	Source
MIPI HBP (Client)	Delay MIPI Client DPI RGB by HBP to make it consistent for every line (arbitrarily set to 16 clocks)	16	pclk		MIPI Client (see **Figure 3**)
HFP min	Min HFP	48	pclk		Combined
HSA min	Min HSYNC pulse	1	pclk		Combined
HBP min	Min HBP	16	pclk		Combined
VFP min	Min VFP	1	lines		Combined
VSA min	Min VSYNC pulse	1	lines		Combined
VBP min	Min VBP	1	lines	Width, HFP, HBP, HSA	Combined

Figure 3 shows the MIPI Client timing.

Figure 3: MIPI Client Timing Diagram



MIPI D-PHY

The MIPI D-PHY supports the following features:

- Type 1 display architecture in command mode
- Synchronous transfer at high speed mode with bit rates of 80 Mbps to 1 Gbps
- Asynchronous transfer at low power mode with a bit rate of 10 Mbps
- Spaced one-hot encoding for low power data
- One byte buffer housed inside the core for data-in and data-out path
- Data lanes for transfer of data in high speed as well as in low power modes
- Ultra low power mode, escape mode and high speed mode
- Activation and disconnecting of high speed terminators for reception and transmission
- Type 4 display architecture in video mode
- Video mode and command mode support in dual channel mode

MIPI Bandwidth Calculations

The MIPI bandwidth calculations used to support maximum resolution are:

H (in pixels) x W (in pixels) x FPS x BPP = x

1 Gbps x 4 lane MIPI = 4 Gbps

4 Gbps - x = Maximum allowable total command overhead

WUXGA (1920x1200 60 fps with 24 bpp) calculation:

Total data rate of WUXGA with 24 bpp = 3.317 Gbps

Maximum number of MIPI lanes = 4

Per MIPI lane bandwidth minimum requirement = 829 Mbps

Maximum allowable total command overhead (blanking + overhead, all lanes) = 0.683 Gbps

I²C Slave

NOTE: The bus clock must be 25X the speed of the I²C clocks.

The following features are supported by the I²C Slave:

- All mandatory I²C specifications (Start, Stop, Acknowledge, etc.)
- Repeated starts
- 7-bit slave addressing:
  - LS – Two bits that can be controlled through the pins GPIO[2] and GPIO[3] (the default value is “00”)
  - MS – Five bits that can be controlled through the register (the default value is “11001”)
- MIPI command emulation over an I²C interface
- Bursts for MIPI commands and direct access
- Maximum speed up to 400 kilobits/sec (fast mode)
- Direct register access where the address is followed by:
  - N bytes data to be written for write access
  - number of bytes to be read

The following features are not supported by the I²C Slave:

- Device ID – The Device ID field is an optional 3-byte (24-bit) read-only word providing the following information:
  - Twelve bits that contain the manufacturer name (unique per manufacturer, such as NXP)
  - Nine bits that contain the part identification (assigned by manufacturer, such as PCA9698)
  - Three bits that contain the die revision (assigned by manufacturer, such as RevX)
- 10-bit addressing
- Clock stretching
- Reserved addresses
- High-speed mode (3.4 Mbps)

I²C Data Format

The I²C Slave on the ArcticLink III BX5 device supports two types of accesses, the direct and MIPI-emulated. Direct access allows the I²C Master to read from and write to the ArcticLink III BX5 device internal registers. The MIPI-emulated access allows the I²C Client to initiate MIPI access on the MIPI Client through the internal DBI bus. To enable this feature, the I²C Slave must distinguish which type of access is being initiated on the I²C bus.

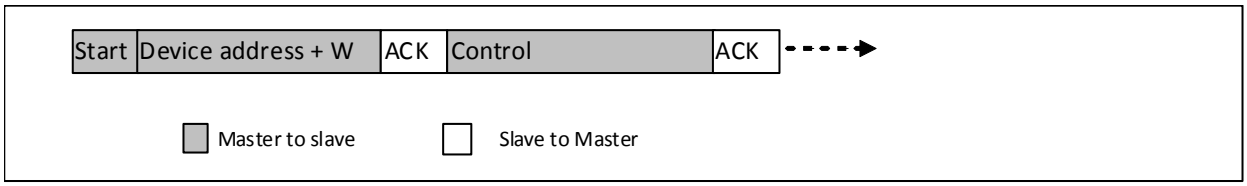


Table 3 defines the I²C data format.

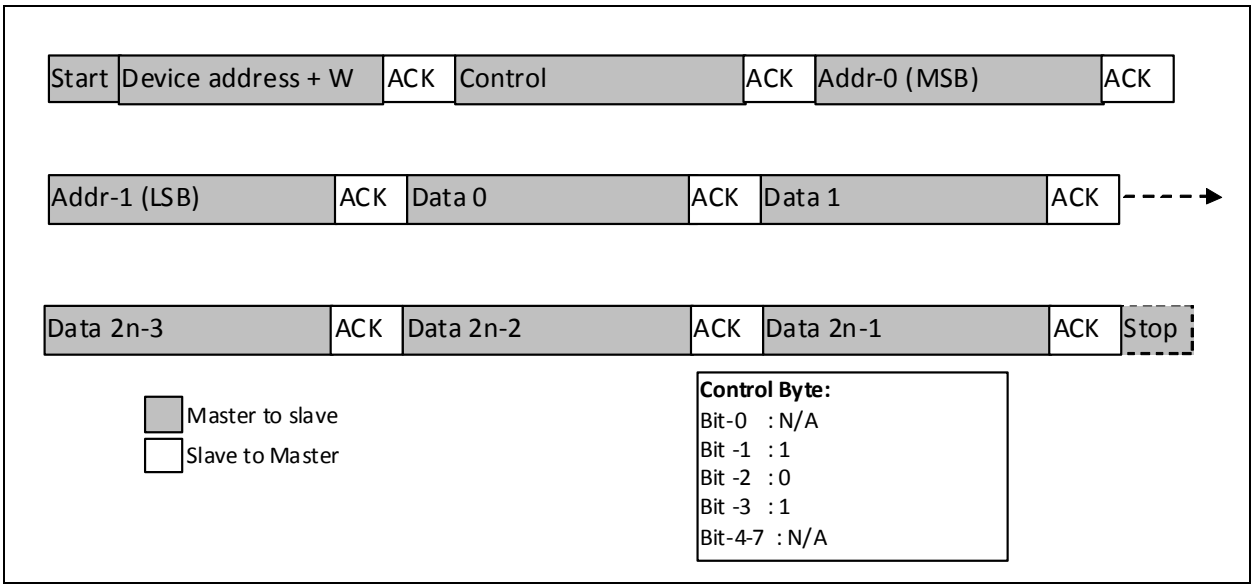
Table 3: I²C Data Format

Control Bit(s)	Description
[0]	MIPI-emulated access only: 1 – Generic command 0 – DCS command
[1]	Access type: 1 – Direct access 0 – MIPI-emulated access
[2]	Direct access type: 1 – Read access 0 – Write access
[3]	Control Interface Module MUX control: 1 – I²C 0 – MIPI[a]
[7:4]	Reserved

a. Upon reset, the Control Interface Module MUX control defaults to '0' – MIPI. The I²C Master can gain control by issuing an I²C access with control bit [3] set to '1' – I²C. To return control back to MIPI, the I²C Master initiates an I²C access with control bit [3] set to '0'.

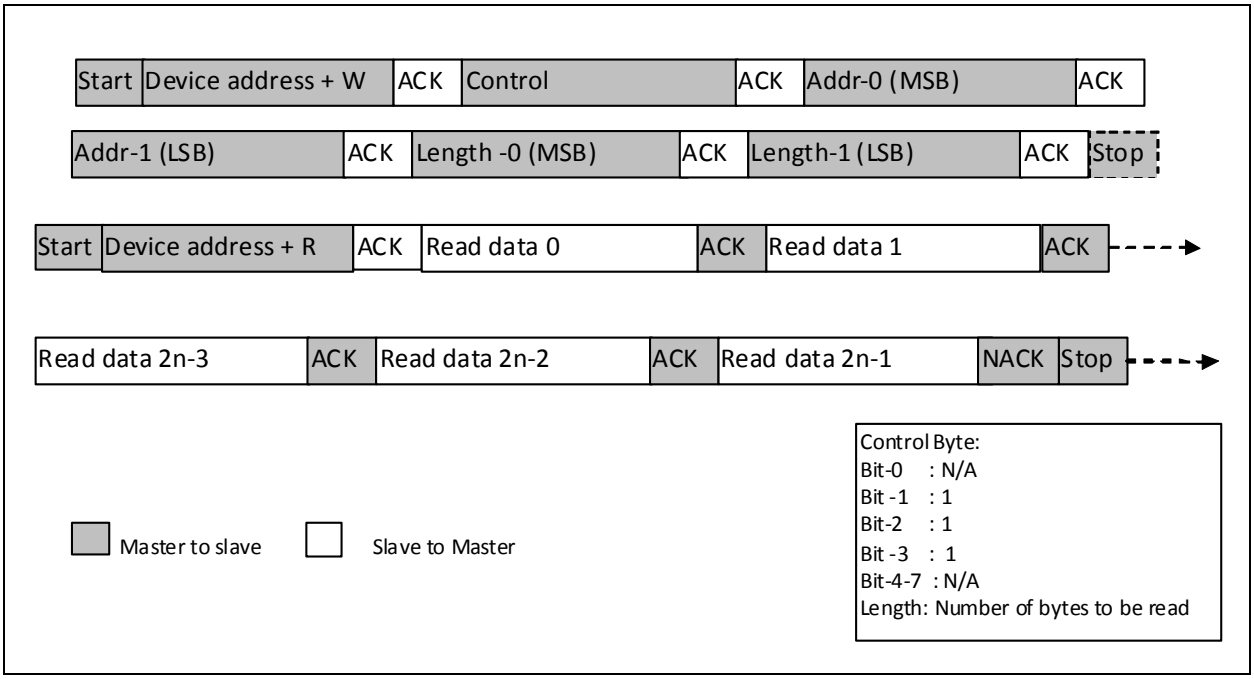
I²C Direct Access Write

The I²C Master can initiate a direct access write to the register offset *Addr* by issuing the following Write command sequence on the I²C bus. The I²C Slave automatically increments *Addr* to support burst access.



I²C Direct Access Read

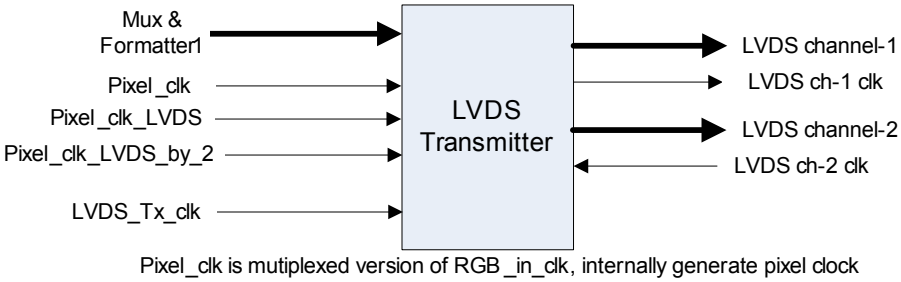
The I²C Master can initiate a direct access read from the register offset *Addr* by issuing the following Read command sequence on the I²C bus. The I²C Slave automatically increments *Addr* to support burst access.



LVDS Transmitter

Figure 4 shows the LVDS Tx interface signals.

Figure 4: LVDS Tx Interface



The LVDS Transmitter block interfaces to the Mux and Formatter 1 module. This block receives 24-bit RGB data (RGB565, RGB666 or RGB888) along with DE, HSync and VSync signals from the Mux and Formatter 1 module. The pixel clock the LVDS Transmitter block receives is up to 173 MHz.

Dual channel LVDS transmissions are 560 Mbps per lane.

LVDS lanes must be driven every cycle irrespective of the state of RGB data, DE and Sync signals. For single channel LVDS mode, data is presented on either channel-1 or channel-2 based on configuration.

LVDS Timing

Figure 5 shows the RGB666 mapping of a single channel LVDS.

Figure 5: RGB666 Mapping of a Single Channel LVDS

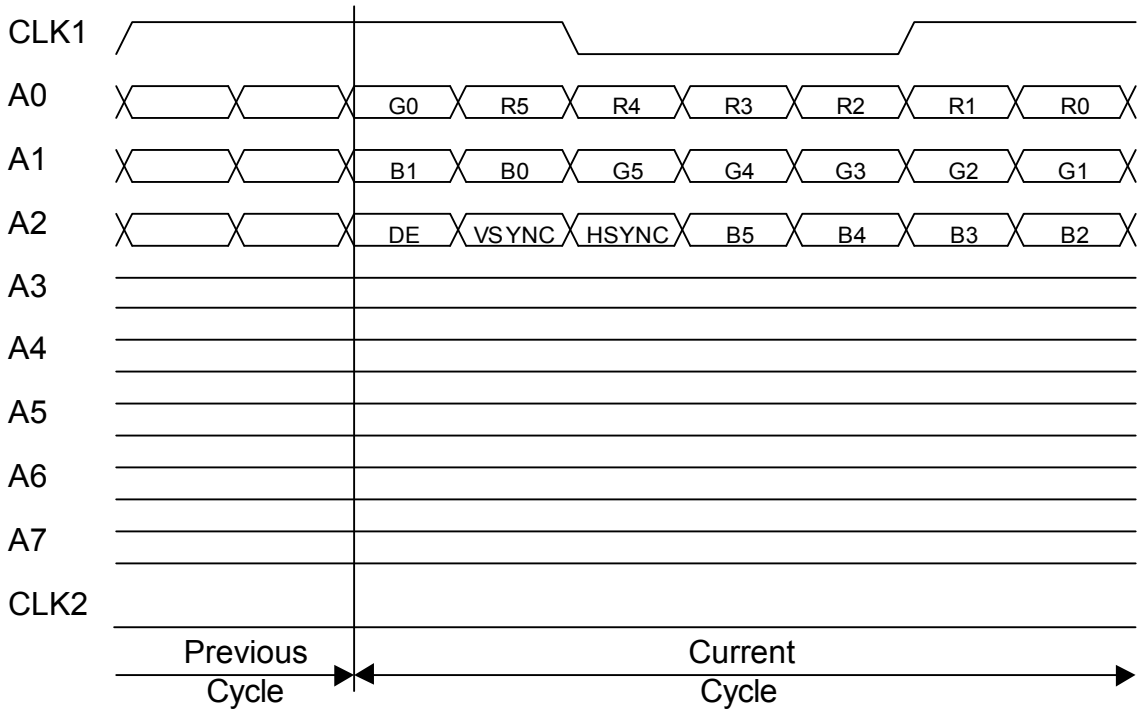


Figure 6 shows the RGB666 mapping of a dual channel LVDS.

Figure 6: RGB666 Mapping of a Dual Channel LVDS

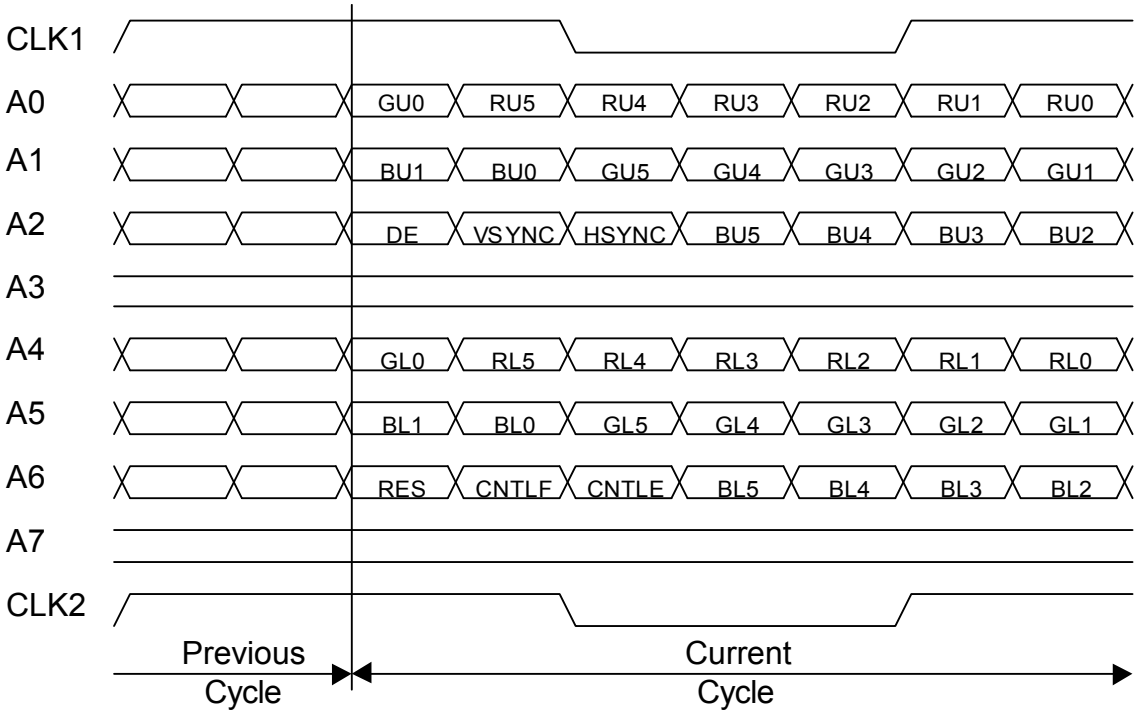
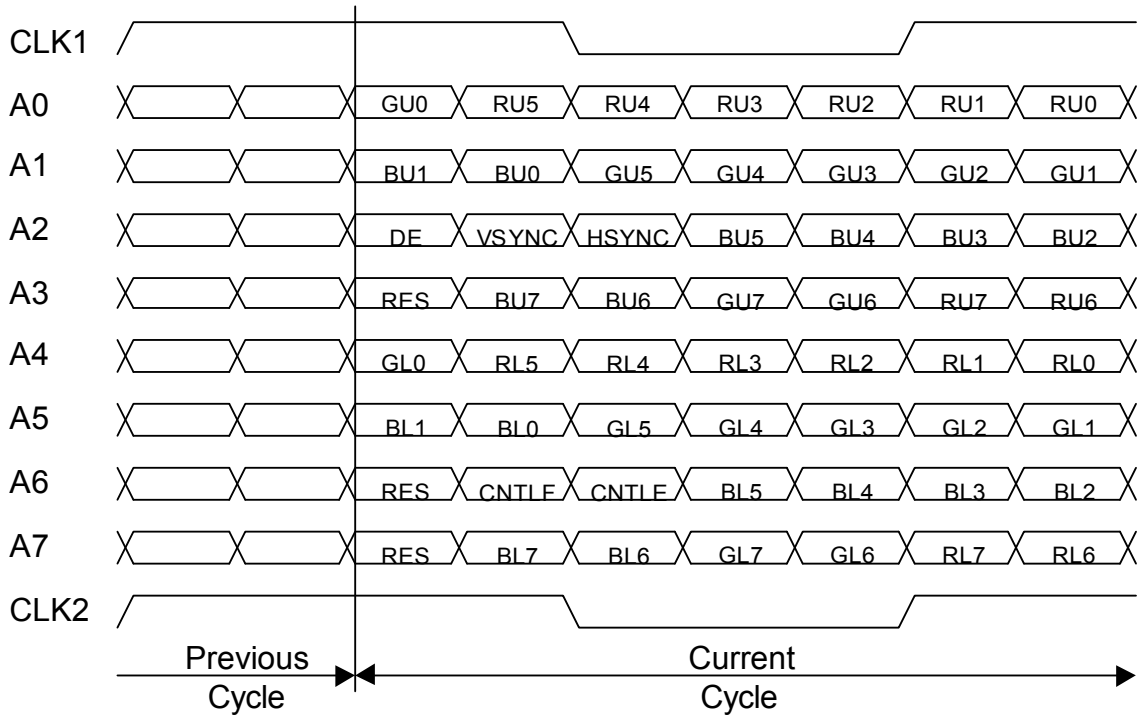


Figure 7 shows the RGB888 mapping of a dual channel LVDS.

Figure 7: RGB888 Mapping of Dual Channel LVDS



Serializer

The LVDS Tx serializer is a 7:1 serializer that runs on pixel clock and 7*pixel clock for single channel LVDS mode, and pixel clock/2 and 7*pixel clock/2 for dual channel LVDS mode. In the serializer, data bits D6 to D0 are loaded to the shift register on the rising edge of *pixel_clk_lvds*. Then the data is shifted for the next six clock cycles of *lvds_tx_ck*.

Figure 8 shows the serializer.

Figure 8: Serializer Diagram

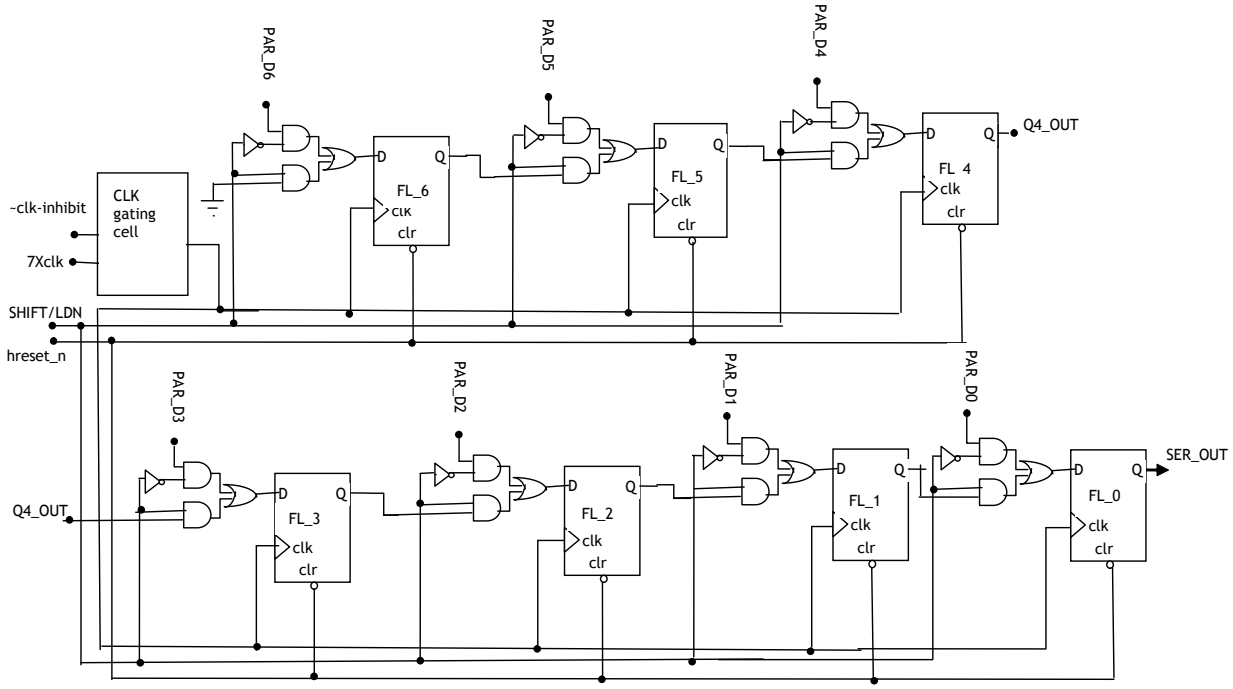


Figure 9 shows the shift/load pulse generation.

Figure 9: Shift/Load Generation

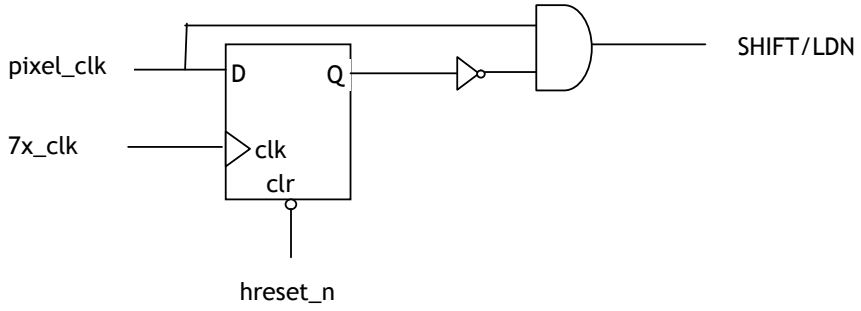


Figure 10 shows the serializer timing diagram.

Figure 10: Serializer Timing Diagram

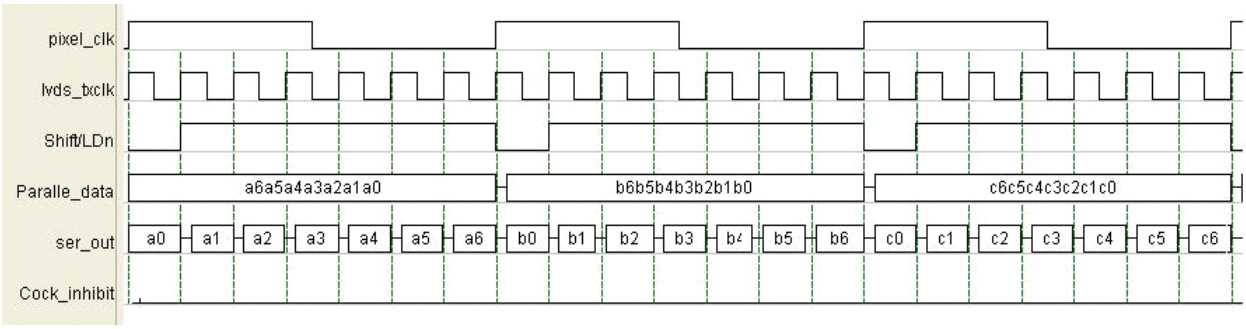


Table 4 describes the LVDS I/O interface signals.

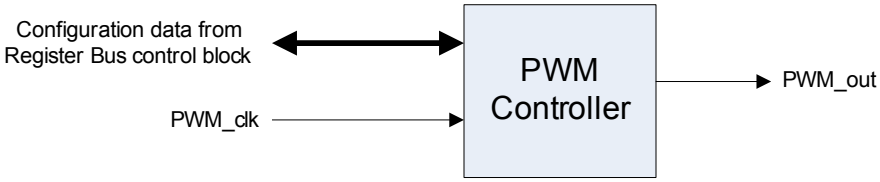
Table 4: LVDS I/O Interface Signals

LVDS-PAD Interface	Description	Driven by in BX5
D	Line driver data input from core	Serializer
ENB	Core active-high power down mode select	Register (LP modes)
OEB	Active-ow output enable	Register bit based on use case
MODE	Current selector pin: 0 = low current 1 = high current	Register
VSEL	Core voltage selector: 0 = VDD is 1.0 V 1= VDD is 1.2 V	Register

Pulse Width Modulator Controller

Figure 11 shows the PWM Controller signal interface.

Figure 11: PWM Controller Interface



The PWM Controller has following features:

- 16-bit register to load count, based on which PWM width is to be generated
- Configurable *PWM_clk* prescale factors of /1 to /1024 of the system clock
- Duty Cycle = Mark Period/Frame Period = Data Value/2^n
- Mark Period = Data Value*Tclock
- Frame Period = Tclock*2^n
- 16-bit PWM Core, n = 16

Clock and Reset Controller

Figure 12 shows the Clock and Reset Controller signal interface.

Figure 12: Clock and Reset Controller Interface

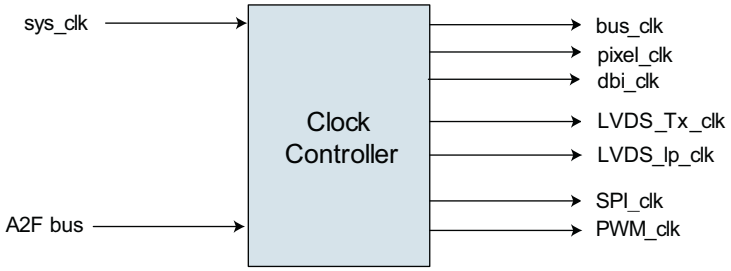


Table 5 describes the ArcticLink III BX5 device clocks.

Table 5: ArcticLink III BX5 Device Clocks

Clock Name	Maximum Frequency	Description	Remarks
sys_clk	9 MHz to 20 MHz	Input clock to the ArcticLink III BX5 solution platform.	
bus_clk	~80 MHz	A2F register access bus, I^2C, SPI, and PWM.	
pixel_clk	~160 MHz	DPI and MIPI DSI Rx Client IP.	
dbi_clk	160 MHz	MIPI DSI Rx client.	Same as *pixel_clk.*
MIPI_lp_clk	~20 MHz	MIPI DSI Rx core and low power clock (to be derived from *sys_clk*).	Same as *sys_clk* or some division needed
pixel_clk_LVDS _by_2	80 MHz	LVDS Tx dual mode.	
SPI_clk	~20 MHz	SPI Master (with necessary divisions from *bus_clk*).	/4 or /8 of *bus_clk*.
PWM_clk		PWM (with necessary divisions from *bus_clk*).	The PWM divider range is 1 to 1024.

Low Power Standby Mode

To enter low power standby mode, set the registers and values as shown in **Table 6**.

Table 6: Standby Mode Register Settings

Address	Value
0x700	0x24000040
0x704	0x9F0009
0x708	0x00000000
0x70C	0x600
0x710	0xC0002
0x714	0x20
0x718	0x309
0x154	0x00000000
0x154	0x80000000
0x248	0x10630009
0x378	0xCA0F3C90
0x37C	0x00000060
0x38C	0x10630009
0x608	0x50F

Register Sets

Table 7 shows the CSSP register set.

Table 7: CSSP Register Set

Offset Address	Description
00h – 58h	MIPI DSI Client Registers
0x04 – 0x74	Common Registers
0x0000 – 0x000a	LVDS Registers
0x00 – 0x18	Clock and Reset Registers
0x00 – 0xff	Reserved

Register Maps

NOTE: QuickLogic will provide the correct register settings/a tool for correctly generating register settings during system design.

MIPI DSI Client Registers

NOTE: The base address for the MIPI DSI Client registers block is 0x200.

Table 8 defines the MIPI DSI Client registers.

Table 8: MIPI DSI Client Registers

Register Offset	Register Name	Default Value
00h	Device ready register	32'h0000_0001
04h	Interrupt status register	32'h0000_0000
08h	Interrupt enable register	32'h03ff_bf7f
0ch	DSI functional programming register	32'h0000_0021
10h	High speed receive timeout counter register	32'h00ff_ffff
14h	Low speed transmit timeout counter register	32'h0001_ffff
18h	Turn around timeout counter register	32'h0000_0014
1ch	Initialization count register	32'h0000_07d0
20h	Max_return_pack_size register	32'h0000_0001
24h	Eot_Ecc_CRC disable register	32'h0000_0000
28h	HBP_count_register	32'h0000_0000
2ch	Data_lane_timing_prarmeter_register	32'h0000_1001
30h	Reset_enable_DFE register	32'h0000_0001
34h	Afe_Trim0_register	32'hca03_3a10
38h	Afe_Trim1_register	32'h0000_1060
3ch	Afe_Trim2_register	32'h82a8_6030
40h	Afe_Trim3_register	32'h8861_4008
44h	Afe_Trim4_register	32'h0010_0285
48h	Afe_Trim5_register	32'h1060_0008
4ch	Reserved	32'h0000_0000
50h	Afe_Trim7_register	32'h4008_82a8
54h	Error_auto_recovery_register	32'h0000_001f
58h	DPI_sync_count_register	32'h0001_0001

Common Registers

After writing to any of these registers, the software sets the Configuration Done register indicating the end of configuration. The hardware then accepts new configuration values.

NOTE: The base address for the Common registers block is 4'h1 (i.e., start address is 0x100 and end address is 0x1ff).

Table 9 defines the Common registers.

Table 9: Common Registers

Register Offset	Register Name	Default Value
0x04	Resolution register	0x0000_0000
0x08	Command control register1	0x0080_8290
0x14	Miscellaneous control register	0x000c_6300
0x30	Mux and formatter 1/2/3	0x0000_0000
0x38	GPIO-in/out register	0x3FFF_XXXX
0x3c	GPIO control register-1	0x0000_0000
0x40	GPIO control register-2	0x0001_0000
0x44	I^2C slave register	0x0000_1943
0x48	Error status register	0x0000_0000
0x4c	Error mask register	0x0000_0000
0x50	Debugging status register	0x0000_0000
0x54	Configuration done register	0x0000_0000
0x58	Device IP configuration register	0x0000_0000
0x5c	PWM 1 control register	0x0000_0000
0x60	PWM 1 frequency register	0x0000_0000
0x64	PWM 1 high time register	0x0000_0000
0x68	PWM 2 control register	0x0000_0000
0x6c	PWM 2 frequency register	0x0000_0000
0x70	PWM 2 high time register	0x0000_0000
0x74	Reserved	0x0000_0000

LVDS Registers

NOTE: The base address for the LVDS register block is 0x600.

Table 10 defines the LVDS registers.

Table 10: LVDS Registers

Register Offset	Register Name
0x0000	LVDS_Tx_ctrl_reg1[15:0]
0x0002	LVDS_Tx_ctrl_reg1[31:16]
0x0004	LVDS_Tx_ctrl_reg2[15:0]
0x0006	LVDS_Tx_ctrl_reg2[31:16]
0x0008	LVDS_Tx_ctrl_reg3[15:0]
0x000a	LVDS_Tx_ctrl_reg3[31:16]

Clock and Reset Registers

NOTE: The base address for the Clock and Reset registers block is 0x700.

Table 11 defines the Clock and Reset registers.

Table 11: Clock and Reset Registers

Register Offset	Register Name
0x00	Clk Rst Register-1
0x04	Clk Rst Register-2
0x08	Soft Reset Register
0x0C	Low Power Register
0x10	Use Case Register
0x14	Mux Select Register
0x18	PLL Power Down Control Register

Register Descriptions

Common Registers

Resolution Register for Secondary Video Path (DBI-DPI-DBI) (Address: 0x104)

Bit(s)	Field	Reset Value	Type	Description
[11:0]	Pixels per line	0x000	R/W	Number of pixels per line. Synchronized as write to from I^2C or DBI. Used only when the next command is read and register bits are stable.
[14:12]	Reserved			
[26:15]	Lines per frame	0x000	R/W	Number of lines per frame. Synchronized as write to from I^2C or DBI. Used only when the next command is read and register bits are stable.
[27]	Command decoded/programmed selection	0x0	R/W	Selection between command decoded value and programmed value. 0 = Command decoded 1 = Programmed
[31:28]	Reserved			

Command Control Register (Address: 0x108)

Bit(s)	Field	Reset Value	Type	Description
[1:0]	Reserved			
[2]	Invert SD polarity	0x0	R/W	Inverts SD polarity going in/out to/of shared SPI SS2 and PWM1 I/O. 0 = Do not invert 1 = Invert
[3]	Reserved			
[6]	DCS command selection	0x0	R/W	Selects between VC given by client or programmed value to use for DCS commands. 0 = VC given by client IP 1 = Programmed value
[14:7]	“Interoperability” vendor identifier-1	0x05	R/W	
[22:15]	“Interoperability” vendor identifier-2	0x01	R/W	
[23]	Inversion bit	0x1	R/W	
[31:24]	Reserved			

Miscellaneous Control Register (Address: 0x114)

Bit(s)	Field	Reset Value	Type	Description
[0]	Bypass RGB/BGR swap detected by set_address_mode command	0x0	R/W	Selects whether to bypass RGB/BGR swap. 0 = Do not bypass 1 = Bypass
[4:1]	Reserved			
[9:5]	Control interface write FIFO almost full	0x18	R/W	Control interface write FIFO almost full threshold.
[14:10]	Control interface read FIFO almost full	0x18	R/W	Control interface read FIFO almost full threshold.
[19:15]	A2F write FIFO almost full threshold	0x18	R/W	A2F write FIFO almost full threshold.
[20]	Control interface async read FIFO flush	0x0	R/W	Flushes the FIFO if the I^2C master stops the transaction before reading all the bytes.
[25:21]	Async read FIFO read threshold value	0x0	R/W	Async read FIFO read threshold value.
[26]	DPItoDBI FIFO flush	0x0	R/W	
[27]	Reserved			
[28]	Host AHB hresp	0x0	R	Set by the hardware and cleared by software.
[29]	Client AHB hresp	0x0	R	Set by the hardware and cleared by software.
[31:30]	Reserved			

Mux and Formatter 1/2/3 (Address: 0x130)

Programming these registers sets the output format.

Bit(s)	Field	Reset Value	Type	Description
[2:0]	Reserved			
[4:3]	Output format	0x0	R/W	00 = Undefined 01 = RGB565 10 = RGB666 11 = RGB888 Mux and formatter 1
[5]	Hsync polarity	0x0	R/W	0 = No change in polarity 1 = Invert polarity Mux and formatter 2
[6]	Vsync polarity	0x0	R/W	0 = No change in polarity 1 = Invert polarity Mux and formatter 2
[7]	DE polarity	0x0	R/W	0 = No change in polarity 1 = Invert polarity Mux and formatter 2
[9:8]	Reserved			
[10]	Hsync polarity	0x0	R/W	0 = Active High polarity 1 = Active low polarity Mux and formatter 3
[11]	Vsync polarity	0x0	R/W	0 = Active High polarity 1 = Active low polarity Mux and formatter 3
[14:12]	Output format	0x0	R/W	000 = Undefined 001 = RGB565 010 = RGB666 011 = RGB888 100 = LRGB666 101, 110, 111 = Undefined
[31:15]	Reserved			

In/Out GPIO and Hardware Configurable Pins

This ArcticLink III device contains eight GPIOs. While each GPIO has a default function as shown, these GPIOs can be configured to perform several functions. For example, GPIO0 can be used as a hardware configurations pin to select the system clock source. During a reset, the device will read the value on this pin to determine the source of system clock. After reset, the pin can be used for other functions, such as PWM0 output. This selection is done by registers. All other GPIO can function in similar ways.

GPIO In/Out Register (Address: 0x138)

Bit(s)	Field	Reset Value	Type	Description
[14:0]	GPIO[14:0]	0xXXXX (Value sampled at I/O pin)	R/W	If GPIO pins are configured as: • Inputs – Both hardware and software can configure the corresponding bits. • Outputs – Only the hardware can configure the corresponding bits.
[29:15]	Dir_sel for GPIO0-14	0x7FFF	R/W	Direction selection for GPIO pins 0 through 14. 1 = Input 0 = 0utput
[31:30]	Reserved		R/W	

GPIO Control Register-1 (Address: 0x13c)

Bit(s)	Field	Reset Value	Type	Description
[3:0]	GPIO0 output mux selection	0x0	R/W	0 = PWM1 1 = PWM1 2 = PWM2 3 = SCLK 4 = MOSI 5 = SS1 6 = SS2 7 = SD_OUT 8 = TE_OUT 9 = Interrupt 10 = GPIO_INOUT_REG[0] Default: PWM1
[7:4]	GPIO1 output mux selection	0x0	R/W	0 = PWM2 1 = PWM1 2 = PWM2 3 = SCLK 4 = MOSI 5 = SS1 6 = SS2 7 = SD_OUT 8 = TE_OUT 9 = Interrupt 10 = GPIO_INOUT_REG[1] Default: PWM2

Bit(s)	Field	Reset Value	Type	Description
[11:8]	GPIO2 output mux selection	0x0	R/W	0 = SCLK 1 = PWM1 2 = PWM2 3 = SCLK 4 = MOSI 5 = SS1 6 = SS2 7 = SD_OUT 8 = TE_OUT 9 = Interrupt 10 = GPIO_INOUT_REG[2] Default: SCLK
[15:12]	GPIO3 output mux selection	0x0	R/W	0 = MOSI 1 = PWM1 2 = PWM2 3 = SCLK 4 = MOSI 5 = SS1 6 = SS2 7 = SD_OUT 8 = TE_OUT 9 = Interrupt 10 = GPIO_INOUT_REG[3] Default: MOSI
[19:16]	GPIO4 output mux selection	0x0	R/W	0 = SDA_OUT 1 = PWM1 2 = PWM2 3 = SDA_OUT 4 = SCLK 5 = MOSI 6 = SS1 7 = SS2 8 = SD_OUT 9 = TE_OUT 10 = Interrupt 11 = GPIO_INOUT_REG[4] Default: SDA_OUT
[23:20]	GPIO5 output mux selection	0x0	R/W	0 = SS1 1 = PWM1 2 = PWM2 3 = SDA_OUT 4 = SCLK 5 = MOSI 6 = SS1 7 = SS2 8 = SD_OUT 9 = TE_OUT 10 = Interrupt 11 = GPIO_INOUT_REG[5] Default: SS1

Bit(s)	Field	Reset Value	Type	Description
[27:24]	GPIO6 output mux selection	0x0	R/W	0 = SS2 1 = PWM1 2 = PWM2 3 = SDA_OUT 4 = SCLK 5 = MOSI 6 = SS1 7 = SS2 8 = SD_OUT 9 = TE_OUT 10 = Interrupt 11 = GPIO_INOUT_REG[6] Default: SS2
[31:28]	GPIO7 output mux selection	0x0	R/W	0 = SD_OUT 1 = PWM1 2 = PWM2 3 = SDA_OUT 4 = SCLK 5 = MOSI 6 = SS1 7 = SS2 8 = SD_OUT 9 = TE_OUT 10 = Interrupt 11 = GPIO_INOUT_REG[7] Default: SD_OUT

GPIO Control Register-2 (Address: 0x140)

Bit(s)	Field	Reset Value	Type	Description
[3:0]	GPIO8 output mux selection	0x0	R/W	0 = GPIO_INOUT_REG[0] 1 = PWM1 2 = PWM2 3 = SDA_OUT 4 = SCLK 5 = MOSI 6 = SS1 7 = SS2 8 = SD_OUT 9 = TE_OUT 10 = Interrupt 11 = GPIO_INOUT_REG[0] Default: GPIO_INOUT_REG[0]
[6:4]	SDA_IN	0x0	R/W	0 = GPIO 4 1 = GPIO 4 2 = GPIO 5 3 = GPIO 6 4 = GPIO 7 5 = GPIO 8 Default: GPIO 4

Bit(s)	Field	Reset Value	Type	Description
[9:7]	SCL	0x0	R/W	0 = GPIO 5 1 = GPIO 4 2 = GPIO 5 3 = GPIO 6 4 = GPIO 7 5 = GPIO 8 Default: GPIO 5
[12:10]	MISO	0x0	R/W	0 = GPIO 6 1 = GPIO 4 2 = GPIO 5 3 = GPIO 6 4 = GPIO 7 5 = GPIO 8 Default: GPIO 6
[15:13]	SD_IN	0x0	R/W	0 = GPIO 7 1 = GPIO 4 2 = GPIO 5 3 = GPIO 6 4 = GPIO 7 5 = GPIO 8 6 = SD from RGB IN/OUT 7 = MIPI Client NOTE: Use this register to define where the SD-input is taken from, irrespective of whether this GPIO pin is used or not.
[20:16]	GPIO_oe_mux_sel	0x01	R/W	OE mux selection for GPIO 4 through GPIO 8. 0 = GPIO_en 1 = SDA_en
[31:21]	Reserved			

I²C Slave Register (Address: 0x144)

Bit(s)	Field	Reset Value	Type	Description
[3:0]	Filt_sel[3:0]	0x3	R/W	Glitch filter configuration input. Can be hard-fixed; depends on the bus_clk frequency and I²C speed. Note: The glitch filter selection can be made configurable by providing a register for the same in the A2F bus.
[7:4]	Sda_del[3:0]	0x4	R/W	To adjust the SDA_IN delay to fix hold violation issues.
[12:8]	Slave_addr_msb[4:0]	0x19	R/W	MS 5 bits of Slave address.
[31:13]	Reserved			

Error Status Register (Address: 0x148)

Bit(s)	Field	Reset Value	Type[a]	Description
[0]	MIPI unrecognized/ undefined generic command	0x0	R	0 = Not detected 1 = Unrecognized/undefined generic command detected
[1]	Control interface sync write FIFO full		R	
[2]	Control interface async read FIFO full		R	
[3]	DBI controller async FIFO full		R	
[4]	DBItoDPI FIFO full		R	
[5]	DPItoDBI FIFO full		R	
[6]	A2F master async FIFO full		R	
[7]	AHB slave error		R	
[8]	SPI Master Tx done		R	
[9]	SPI Master Tx register overwrite		R	
[17:10]	SPI address where overwrite happened		R	
[18]	LVDS Tx Ch-1 async FIFOs full		R	
[19]	LVDS Tx Ch-1 async FIFOs full		R	
[20]	AHB host interrupt	0x0	R	
[21]	AHB client interrupt	0x0	R	
[31:22]	Reserved			

a. Set by the hardware and cleared by software.

Error Mask Register (Address: 0x14c)

Bit(s)	Field	Reset Value	Type	Description
[0]	MIPI unrecognized/undefined generic command	0x0	R/W	0 = Not masked 1 = Masked
[1]	Control interface sync write FIFO full		R/W	
[2]	Control interface async read FIFO full		R/W	
[3]	DBI controller async FIFO full		R/W	
[4]	DBItoDPI FIFO full		R/W	
[5]	DPItoDBI FIFO full		R/W	
[6]	A2F master async FIFO full		R/W	
[7]	AHB slave error		R/W	
[8]	SPI Master TX done		R/W	
[9]	SPI Master Tx register overwrite		R/W	
[17:10]	Reserved			
[18]	LVDS Tx Ch-1 Async FIFOs full		R/W	
[19]	LVDS Tx Ch-1 Async FIFOs full		R/W	

Bit(s)	Field	Reset Value	Type	Description
[20]	Reserved			
[21]	Ahb client interrupt		R/W	
[31:22]	Reserved			

Debugging Status Register (Address: 0x150)

Bit(s)	Field	Reset Value	Type	Description
[11:0]	Number of pixels per line	0x000	R	
[23:12]	Number of lines per frame	0x000	R	
[24]	RGB swap DBI to DPI	0x0	R	
[25]	RGB swap DPI to DBI	0x0	R	
[27:26]	RGB Format DBI	0x0	R	
[31:28]	Reserved			

Configuration Done Register (Address: 0x154)

Bit(s)	Field	Reset Value	Type	Description
[30:0]	Reserved			
[31]	Config done	0x0	R/W	Used for the synchronization of all the dynamic registers. 0 = Configuring registers 1 = Configuration over

Device IP Configuration Register (Address: 0x158)

Bit(s)	Field	Reset Value	Type	Description
[0]	Device ip config done	0x0	R/W	Status of Device IP register configuration. 0 = Configuring registers 1 = Configuration over
[31:1]	Reserved			

PWM 1 Control Register (Address: 0x15c)

Bit(s)	Field	Reset Value	Type	Description
[1:0]	PWM source select	0x0	R/W	Selects the source of vsync for PWM. 00 = Reserved 01 = LVDS 10 = DPI 11 = DBI
[2]	PWM_enable	0x0		0 = Disable PWM output 1 = Enable PWM output
[31:3]	Reserved			

PWM 1 Frequency Register (Address: 0x160)

Bit(s)	Field	Reset Value	Type	Description
[31:0]	Frequency	0x0000_0000		Division factor of reference clock to determine PWM clock frequency. If 'N' is the programmed valued, it is divided by N + 1.

PWM 1 High Time Register (Address: 0x164)

Bit(s)	Field	Reset Value	Type	Description
[31:0]	High Time	0x0000_0000		Number specifies the logic High for number of reference clock cycle

PWM 2 Control Register (Address: 0x168)

Bit(s)	Field	Reset Value	Type	Description
[1:0]	PWM source select	0x0	R/W	Selects the driver for the CSSP PWM output pin 10 = PWM output 11 = PWM output 0X = PWM-High
[2]	PWM_enable	0x0		0 = Disable PWM output 1 = Enable PWM output
[31:3]	Reserved			

PWM 2 Frequency Register (Address: 0x16c)

Bit(s)	Field	Reset Value	Type	Description
[31:0]	Frequency	0x0000_0000		Division factor of reference clock to determine PWM clock frequency. If 'N' is the programmed valued, it is divided by N + 1.

PWM 2 High Time Register (Address: 0x170)

Bit(s)	Field	Reset Value	Type	Description
[31:0]	High Time	0x0000_0000		The number specifies the logic High for the number of reference clock cycle

LVDS Registers

LVDS_Tx_ctrl_reg1 (Address: 0x600)

Bit(s)	Field	Reset Value	Type[a]	Description
[0]	Number of LVDS channels	0x0	R/W	0 = Single channel 1 = Double channel
[1]	LDI/LVDS mode	0x0	R/W	0 = LDI mode 1 = LVDS mode
[8:2]	Clock pattern for channel-1	0x63	R/W	Specifies the clock pattern to be sent to the first LVDS transmitter channel.
[15:9]	Clock pattern for channel-2	0x63	R/W	Specifies the clock pattern to be sent to the second LVDS transmitter channel.
[16]	Channel to be used by single LVDS mode	0x0	R/W	0 = Sent on Channel-1 1 = Sent on Channel-2
[17]	Channel where first pixel appears for dual LVDS mode	0x0	R/W	0 = Sent on Channel-1 1 = Sent on Channel-2
[21:18]	FIFO Write threshold	0xB	R/W	Threshold value for FIFO write operation.
[25:22]	FIFO Read threshold	0x5	R/W	Threshold value for FIFO read operation.
[29:26]	Reserved			
[30]	CNTLE/TESTA	0x0	R/W	CNTLE/TESTA bits defined in LVDS stream
[31]	CNTLF/TESTB	0x0	R/W	CNTLF/TESTB bits defined in LVDS stream

a. R/W = read/write by software
R/WH = read/write by software and hardware

LVDS_Tx_ctrl_reg2 (Address: 0x604)

Bit(s)	Field	Reset Value	Type[a]	Description
[9:0]	LVDS OEB	0	R/W	Active low output enable.
[19:10]	LVDS MODE	1	R/W	0 = select high current 1 = select low current
[29:20]	LVDS VSEL	1	R/W	>VDD = 1.0v >VDD = 1.2v
[30]	RES	0x0	R/W	RES bit defined in LVDS stream.
[31]	Reserved			

a. R/W = read/write by software
R/WH= read/write by software and hardware

LVDS_Tx_ctrl_reg3 (Address: 0x608)

Bit(s)	Field	Reset Value	Type[a]	Description
[3:0]	ENB	4'hf	R/W	Low power select mode. Active low.
[4]	DE polarity	0	R/W	This is the polarity configuration registers for RGB mux and formatter1. It is used as polarity indication for write control logic. 1 = Active low 0 = Active high
[5]	Hsync polarity	0	R/W	This is the polarity configuration registers for RGB mux and formatter1. It is used as polarity indication for write control logic. 1 = Active low 0 = Active high
[6]	Vsync polarity	0	R/W	This is the polarity configuration registers for RGB mux and formatter1. It is used as polarity indication for write control logic. 1 = Active low 0 = Active high
[8:7]	RGB Format	00	R/W	RGB format configuration bits for mux and formatter1. 00 = undefined 01 = RGB565 10 = RGB666 11 = RGB888
[9]	RES bit configuration	0	R/W	0 = RES bit in output 1 = DE in output
[10]	TEST bits configuration	0	R/W	0 = TEST bits in output 1 = Hsync, Vsync in output
[11]	LVDS enable	0	R/W	LVDS enable/disable. 0 = LVDS not enabled 1= LVDS enabled Note: Set only if all LVDS register configuration is done.
[31:12]	Reserved			

a. R/W = read/write by software
R/WH = read/write by software and hardware

Clock and Reset Registers

ClkRst Register-1 (Address: 0x700)

Bit(s)	Field	Reset Value	Type	Description
[0]	Reserved			
[2:1]	MIPI lp clk division (Client DPHY)	0x0	R/W	0 = /1 1 = /2 2 = /4 3 = Undefined
[4:3]	Bus clock division	0x0	R/W	0 = /1 1 = /2 2 = /4 3 = Undefined
[5]	SPI clock division	0x0	R/W	0 = /4 1 = /8
[9:6]	PWM clock division	0x0	R/W	0 = /2 1 = /4 2 = /8 Values 3 through 10 are invalid division factors. (Division is w.r.t bus clock).
[10]	MIPI lp clock selection	0x0	R/W	This decides the LP clock selection based on sys clk. 0 = Clock generated from PLL (sys clk is 10 MHz to 25 MHz) 1 = Reserved
[11]	DBI clock selection	0x0	R/W	Glitch-free clock muxing for selecting the value of the dbi_clk basic clock. 0 = Bus clock 1 = PLL clock
[12]	PLL lock		R	If set, indicates that the MIPI PLL has attained lock.
[13]	PLL lock		R	If set, indicates that the internal clock PLL has attained lock.
[18:14]	PLL cnta		R/W	Not used.
[19]	PLL cntb		R/W	Not used.
[25:20]	PLL ‘P’ value	0x0	R/W	P value of PLL. Valid range is from 1 to 64. (Always program value P-1.)
[31:26]	PLL ‘S2’ value	0x0	R/W	S2 value of PLL. Valid range is from 1 to 64. (Always program value S2-1.)

Clk Rst Register-2 (Address: 0x704)

Bit(s)	Field	Reset Value	Type	Description
[15:0]	PLL 'M' value	0x270	R/W	M value of PLL. Range is from 8 to 65536. (Always program value M-1.)
[20:16]	PLL 'S' value	0x0	R/W	S value of PLL. Valid range is from 1 to 32. (Always program value S-1.)
[22:21]	PLL bypass	0x0	R/W	Bypass input for PLL. This bypasses the input ref clock to PLLOUT1 and PLLOUT2. 01 = Bypass PLLOUT1 10 = Bypass PLLOUT2 11 = Bypass both clocks
[23]	PLL standby	0x0	R/W	Standby input for PLL.
[31:24]	Reserved			

Soft Reset Register (Address: 0x708)

Bit(s)	Field	Reset Value	Type	Description
[0]	Reserved			
[1]	MIPI DSI Client	0x0	R/W	Resets MIPI DSI client module.
[2]	DBItoDPI and DPItoDBI	0x0	R/W	Resets the DBI2DPI formatter and DPI2DBI formatter modules. Also resets the DBItoDPI and formatter register in the control interface module.
[4:3]	Reserved			
[5]	LVDS Tx	0x0	R/W	Resets the LVDS Tx module.
[6]	Reserved			
[7]	I^2C slave	0x0	R/W	Resets the I^2C slave module. Also resets the I^2C slave register in the control interface module.
[8]	Control Interface (including A2F bus master) and AHB bridge, which runs on bus_clk	0x0	R/W	Resets control interface module. Also resets the following registers: • Resolution register for secondary video path (DBI-DPI-DBI) • Command control register-1 • Command control register-2 • Command control register-3
[9]	PWM	0x0	R/W	Resets the PWM module. Also resets the following registers in the control interface module: • PWM 1 Control register • PWM 1 Frequency register • PWM 1 High Time register • PWM 2 Control register • PWM 2 Frequency register • PWM 2 High Time register
[10]	SPI Master	0x0	R/W	Resets the SPI Master module.
[11]	DBI Controller	0x0	R/W	Resets DBI Controller module. Also resets the DBI controller register in the control interface.

Bit(s)	Field	Reset Value	Type	Description
[29:12]	Reserved	0x0		
[30]	Chip reset	0x0	R/W	Resets the whole device.
[31]	Reset trigger	0x0	R/W	

Low Power Register (Address: 0x70C)

Bit(s)	Field	Reset Value	Type	Description
[0]	Reserved			
[1]	Clock enable for MIPI DSI Client DPI	0	R/W	When both are clock gated, DPHY is powered down. PHY has per lane power down.
[2]	Clock enable for MIPI DSI Client DBI, DBI slave which runs on dbi_clk	1	R/W	When both are clock gated, DPHY is powered down. PHY has per lane power down.
[3]	Clock enable for DBItoDPI & DPItoDBI	0	R/W	
[5:4]	Reserved			
[6]	Clock enable for LVDS Tx digital	0	R/W	Separate power down for the each ENB of LVDS I/Os.
[8:7]	Reserved			
[9]	Clock enable for the I^2C slave	1	R/W	
[10]	Control Interface (including A2F bus master) and AHB bridge, which runs on bus_clk	1	R/W	Not used. Never clock gate these blocks.
[11]	Clock enable for PWM	0	R/W	
[12]	Clock enable for SPI Master	0	R/W	
[13]	Enable for PLL	0	R/W	
[14]	Enable for PLL	0	R/W	
[31:15]	Reserved			

Use Case Register (Address: 0x710)

Bit(s)	Field	Reset Value	Type	Description
[1:0]	Primary Video Input source	0x0		00 = Not present 01 = Reserved 10 = Reserved 11 = MIPI Rx DPI
[2]	Reserved			
[3]	Primary Video Output – LVDS Tx	0x0		0 = Disabled 1 = Enabled
[15:4]	Reserved			
[16]	Clock edge to be used for channel1 clk lane	0x0		0 = Posedge 1 = Negedge

Bit(s)	Field	Reset Value	Type	Description
[17]	Clock edge to be used for channel2 clk lane	0x0		0 = Posedge 1 = Negedge
[18]	Clock edge to be used for channel1 data lane	0x0		0 = Posedge 1 = Negedge
[21:20]	Reserved			
[26:22]	Sel18	0x0		Select whether to use 1.8 V for selected power domains. [0] = Power pad domain1 [1] = Power pad domain2 [2] = Power pad domain3 [3] = Power pad domain4 [4] = Reserved
[31:27]	Reserved			

Mux Select Register (Address: 0x714)

WARNING: The fields marked with an "*" are for advanced users only. It is not necessary to program this field in normal use cases of the device. This field is used to override the internal hardware logic to make clock mux selections. Incorrect programming can cause device errors.

Bit(s)	Field	Reset Value	Type	Description
[0]	MIPI_DPhy_clock select	0x0	R/W	Selects the RGB clock as the reference clock to PLL. 0 = Sys clock 1 = Reserved
[2:1]	Bus clock select software override*	0x0	R/W	Software selection for the bus clock. 00 = No software override 01 = Sys clock 10 = RGB clock 11 = PLL clock
[4:3]	Pixel clock select software override*	0x0	R/W	Software selection for pixel clock. 00 = No software override 01 = PLL clock 10 = RGB clock 11 = Sys clock
[5]	LVDS clock select	0x0	R/W	Selection for LVDS clock. 0 = PLL clock (default) 1 = Generated counter-based clock **NOTE**: Do not program this field for normal operation. Added as a fail-safe option.
[7:6]	PLL ref clock select software override*	0x0	R/W	Software selection for PLL reference clock. 00 = No software override 01 = Sys clock 10 = RGB clock 11 = Reserved
[31:8]	Reserved			

PLL Power-Down Control Register (Address: 0x718)

Bit(s)	Field	Reset Value	Type	Description
[7:0]	PLL power-down counter	8'h05	R/W	The counter value must be set based on the system clock frequency. count_value*sys_clk_period = 100 ns (100 ns based on feedback from PLL).
[8]	PLL reconfiguration indicator	1'b0	R/W	Indicates the PLL has been reconfigured. This helps to know if the PLL has been really powered down or has been powered down for the purpose of reconfiguration.
[9]	PLL lock mask	1'b0	R/W	PLL lock mask. By default the mask is off. If set, masks the PLL lock from affecting the reset of internal modules.
[31:10]	Reserved			

Electrical Specifications

Power-On Sequencing

- The ArcticLink III device does not have a required power-on sequence, as long as sys_reset and sys_clk are held either LOW(GND) or tri-stated.
- All voltage rails should power on linearly.
- All voltage rails should reach 90% of their final values within 500 µs of each other.
- All supplies should ramp to full value within 0.20 ms to 50 ms.
- Device initiation should not happen until all voltage rails reach full value.

AC and DC Characteristics

The AC and DC Specifications are provided in **Table 12** through **Table 21**.

Table 12: Typical Values

Parameter	Value	Parameter	Value
Core Voltage	1.2 V	ESD Pad Protection	1.5 kV
Latch-up Immunity	±100 mA	Laminate Package (WLCSP) Storage Temperature	-55° C to + 125° C

Table 13: Absolute Maximum Ratings

Parameter	Value	Unit
DVDD_1,DVDD_2A, DVDD_2B, DVDD_3	-0.5 to 3.6	V
DVDD_0	-0.5 to 3.6	V
MIPI_RX_VDD12_D	-0.5 to 1.32	V
MIPI_RX_VDD12_B	-0.5 to 1.32	V
MIPI_RX_VDD12_P	-0.5 to 1.32	V
VDD	-0.5 to 1.32	V
PLL_VDDA	-0.5 to 1.32	V
LVDS_DVDD	-0.3 to 3.6	V
Voltage range at any output terminal	-0.3 to 1.5	V
Voltage range at any input terminal	-0.5 to (DVDD_x +0.5)	V
Electrostatic discharge human body model (all pins)	±1.5	kV

Table 14: Maximum Operating Current

Supply Rail	Max.	Unit
DVDD[a]	300	mA
MIPI_RX_VDD[a]	200	mA
LVDS_DVDD	300	mA
VDD, PLL_VDDA	200	mA

a. Total for supply rail.

Table 15: Recommended Operating Conditions

Symbol	Description	Min.	Nom.	Max.	Unit
DVDD_1,DVDD_2A, DVDD_2B, DVDD_3	I/O supplies	1.62	1.8/2.5/3.3	3.63	V
DVDD_0	I^2C and PWM input supplies	1.62	1.8	1.98	V
MIPI_RX_VDD12_D	MIPI/DPHY lane I/O power supply	1.08	1.2	1.32	V
MIPI_RX_VDD12_B	MIPI/DPHY lane BIAS power supply	1.08	1.2	1.32	V
MIPI_RX_VDD12_P	MIPI/DPHY lane PLL power supply	1.08	1.2	1.32	V
VDD	Core power supply	1.08	1.2	1.32	V
PLL_VDDA	PLL power supply	1.08	1.2	1.32	V
LVDS_LVDD	LVDS power supply	3.00	3.3	3.63	V
I2C_SDA, I2C_SCL (DVDD_0)					
V_{IH}	High-level input voltage[a]	$0.7*V_{DVDD\_0}$		$V_{DVDD\_0}+0.3$	V
V_{IL}	Low-level input voltage[a]	-0.3		$0.3*V_{DVDD\_0}$	V
V_{OL}	Output low voltage at 6.5 mA[a]			0.4	V
I2C_SCL	Clock frequency	100		400	kHz
PWM_1, PWM_2 (DVDD_0)					
V_{IH}	High-level input voltage[a]	$0.7*V_{DVDD\_0}$		$V_{DVDD\_0}+0.3$	V
V_{IL}	Low-level input voltage[a]	-0.3		$0.3*V_{DVDD\_0}$	V
SPI (DVDD_1)					
V_{IH}	High-level input voltage[a]	$0.7*V_{DVDD\_1}$		$V_{DVDD\_1}+0.3$	V
V_{IL}	Low-level input voltage[a]	-0.3		$0.3*V_{DVDD\_1}$	V
t_{DS}	Data set-up time prior to SPI_SCLK[a]	50% of SPI_SCLK			ns
t_{DH}	Data hold time prior to SPI_SCLK[a]			50% of SPI_SCLK	ns
SYS_CLK, SYS_RST_N (DVDD_3)					
V_{IH}	High-level input voltage[a]	$0.7*V_{DVDD\_3}$		$V_{DVDD\_3}+0.3$	V
V_{IL}	Low-level input voltage[a]	-0.3		$0.3*V_{DVDD\_3}$	V

Figure 13: Input Signal Setup and Hold Time Definition t_{DS} and t_{DH}

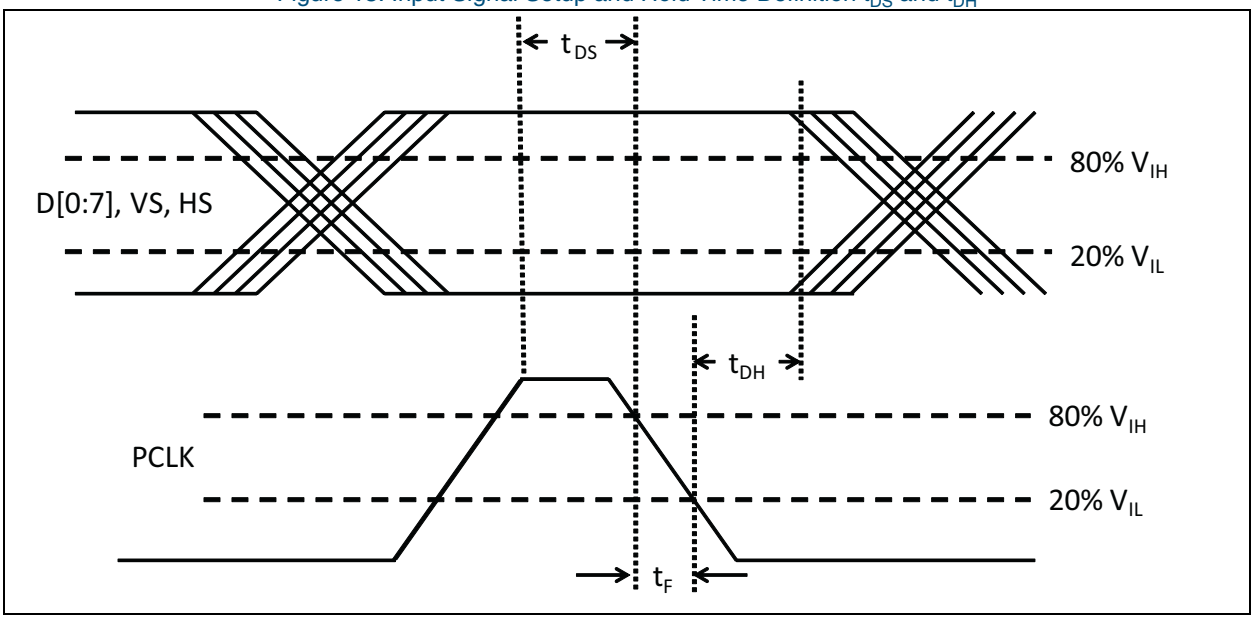


Table 16: Device Electrical Characteristics

Symbol	Description	Parameter	Min.	Typ.	Max.	Unit
I_{DD}	Supply standby current[a]	DVDD_0	-	1	-	µA
		DVDD_1	-	1	-	µA
		DVDD_2A, DVDD_2B	-	8	-	µA
		DVDD_3	-	1	-	µA
		LVDS_VDD	-	10	-	µA
		VDD	-	650	-	µA
	Power-up		-	5	-	mA

a. The device must be configured through the software for standby per **Table 6** on page 17, and Sys_Clk is stopped.

Table 17: RX Input Electrical Characteristics

Symbol	Description	Min.	Typ.	Max.	Unit
HS Receiver DC Specifications					
V_{CMRX}	HS receive static common-mode voltage	70	200	330	mV
V_{IDTh}	Differential input high threshold	-	-	70	mV
V_{IDIL}	Differential input low threshold	-70	-	-	mV
V_{IIHS}	Single-ended input high voltage	-	-	460	mV
V_{ILHS}	Single-ended input low voltage	-40	-	-	mV
$V_{TERM-EN}$	Single-ended threshold for HS termination enable	-	-	450	mV
Z_{ID}	Differential input impedance	80	100	125	ohm
HS Receiver AC Specifications					
$\Delta V_{CMRX(HF)}$	Common-level interference above 450 MHz	-	-	100	mV
$\Delta V_{CMRX(LF)}$	Common-level interference between 50 MHz to 450 MHz	-50	-	50	mV
CMM	Common mode termination	-	-	60	pF
LP Receiver DC Specifications					
V_{IH}	Input high level	880	-	-	mV
V_{IL}	Input low level	-	-	550	mV
$V_{IL-ulps}$		-	-	300	mV
V_{hyst}	Input hysteresis	25	-	-	mV
I_{leak}	Pin leakage current	-10	-	10	µA
LP Receiver AC Specifications					
$e_{(SPICE)}$	Input pulse rejection	-	-	300	ps
T_{MIN-RX}	Minimum pulse width response	20	-	-	ns
V_{INT}	Peak interference amplitude	-	-	200	mV
f_{INT}	Interference frequency	450	-	-	MHz

Table 18: GPIO Input Electrical Characteristics

Symbol	Description	Parameter	Min.	Typ.	Max.	Unit
I2C_SDA, I2C_SCL (DVDD_0)						
$I_{leakage}$	Input leakage	DVDD_0 = 1.62 V and 1.98 V	0	0.2	2	µA
$I_{leakage}$	Input leakage	Power down; Vin = 1.8 V	0	0.1	-	µA
PWM_1, PWM_2 (DVDD_0)						
$I_{leakage}$	Input leakage	DVDD_0 = 1.62 V and 1.98 V	0	0.2	2	µA
$I_{leakage}$	Input leakage	Power down; Vin = 1.8 V	0	0.1	-	µA
SPI (DVDD_1)						
$I_{leakage}$	Input leakage	DVDD_1 = 1.62 V and 3.63 V	0	0.2	2	µA
$I_{leakage}$	Input leakage	Power down; Vin = 3.6 V	0	0.1	-	µA
SYS_CLK, SYS_RST_N (DVDD_3)						
$I_{leakage}$	Input leakage	DVDD_3 = 1.62 V and 3.63 V	0	0.2	2	µA
$I_{leakage}$	Input leakage	Power down; Vin = 0 V[a]	0	0.1	-	µA

a. Do not drive input voltage high while device is powered down, as this can cause high input leakage in excess of 20 mA.

Table 19: GPIO Output Electrical Characteristics

Symbol	Description	Parameter	Min.	Typ.	Max.	Unit
I2C_SDA, I2C_SCL (DVDD_0)						
V_{OL}	Output low voltage	6.5 mA	-	-	0.4	V
I_{OL}	Output low current	V_{OL} = 0.4 V DVDD_0 = 1.8 V	6.5	-	19	mA
PWM_1, PWM_2 (DVDD_0)						
V_{OH}	High-level output voltage		DVDD_0-0.4	-	-	V
V_{OL}	Low-level output voltage		-	-	0.4	V
I_{OH}	Output high current	V_{OH} = DVDD_0-0.4 V	14.8	23.2	35.3	mA
I_{OL}	Output low current	V_{OL} = 0.4 V	15.4	27.3	43.6	mA
SPI (DVDD_1)						
V_{OH}	High-level output voltage	DVDD_1 = 1.62 V I_{OH} = -12 mA	DVDD_1-0.4	-	-	V
V_{OL}	Low-level output voltage	DVDD_1 = 1.62 V I_{OH} = 12 mA	-	-	0.4	V
I_{OH}	Output high current	V_{OH} = DVDD_1-0.4 V DVDD_1 = 1.8 V	14.8	23.2	35.3	mA
I_{OL}	Output low current	V_{OL} = 0.4 V DVDD_1 = 1.8V	15.4	27.3	43.6	mA
V_{OH}	High-level output voltage	DVDD_1 = 2.97 V I_{OH} = -12 mA	DVDD_1-0.4	-	-	V

Table 20: LVDS Output Electrical Characteristics

Symbol	Description	Min.	Typ.	Max.	Unit
LVDS Transmitter DC Specification (RLOAD = 100 ohm)					
V_{OH}	Output high level	-	1365	1485	mV
V_{OL}	Output low level	960	1035	-	mV
V_{OD}	Differential output voltage	250	325	410	mV
V_{OS}	Output offset voltage	1125	1200	1275	mV
$[V_{OD}]$	Change in V_{OD} between "0" and "1"	-	2	25	mV
$[V_{OS}]$	Change in V_{OS} between "0" and "1"	-	10	25	mV
Isa, Isb	Output current (driver shorted to ground)	-40	10	40	mA
Isab	Output current (driver shorted together)	-12	10	12	mA
LVDS Transmitter Supply Current					
I TCCW	Transmitter supply current (@ 550 MHz)	-	12.4	15.3	mA
I TCCS	Transmitter power-down supply current	-	10	-	uA
LVDS Transmitter AC Characteristics					
t_{PHL}	Differential high to low propagation delay		900	1500	ps
t_{PLH}	Differential low to high propagation delay		900	1500	ps
t_{skew}	Differential skew between t_{PHL} and t_{PLH}			100	ps
t_{skew2}	Channel to channel skew	-200	50	300	ps
t_{rise}	Vod Differential rise time	250		350	ps
t_{fall}	Vod differential fall time	250		350	ps
F_{max}	Maximum operating frequency			550	MHz

Figure 14: LVDS Timing Diagram

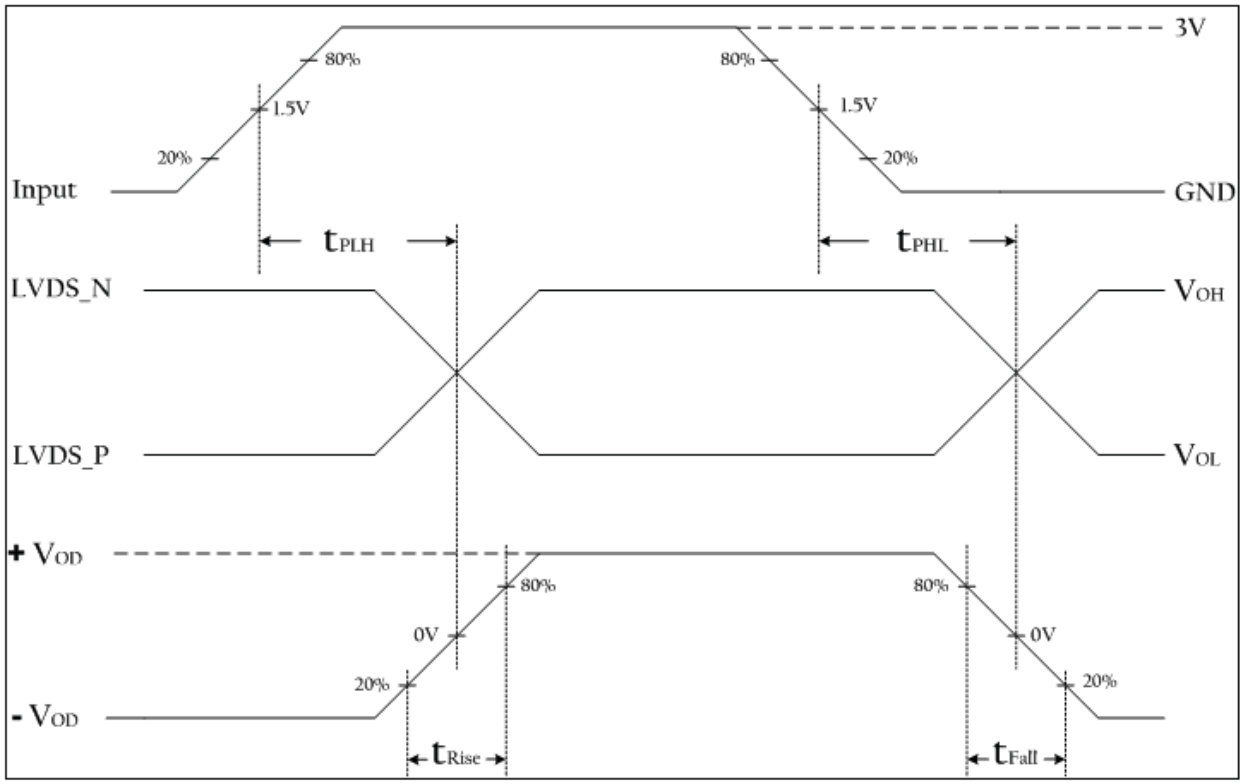


Table 21: System Clock Frequency

Symbol	Description	Min.	Typ.	Max.	Unit
SYS_CLK	System clock frequency	9	-	20	MHz
	Input duty cycle	40	-	60	%
	Input clock rise time	-	-	15	ns
	Input clock fall time	-	-	15	ns
	Input clock period jitter	-	-	100	ps
	PLL output clock jitter			150	ps
	PLL lock time - in power-up	-	150	1000	µs
	System reset time		1.5	50	µs

Package Thermal Characteristics

The ArcticLink III BX5 device is available for the Commercial (-30°C to 85°C Junction) temperature range.

Thermal Resistance Equations:

$\theta_{JC} = (T_J - T_C)/P$
$\theta_{JA} = (T_J - T_A)/P$
$P_{MAX} = (T_{JMAX} - T_{AMAX})/\theta_{JA}$

Parameter Description:

θ_{JC}: Junction-to-case thermal resistance

θ_{JA}: Junction-to-ambient thermal resistance

T_J: Junction temperature

T_A: Ambient temperature

P: Power dissipated by the device while operating

P_{MAX}: The maximum power dissipation for the device

T_{JMAX}: Maximum junction temperature

T_{AMAX}: Maximum ambient temperature

NOTE: Maximum junction temperature (T_{JMAX}) is 100°C. To calculate the maximum power dissipation for a device package look up θ_{JA} from **Table 22**, pick an appropriate T_{AMAX} and use:
$P_{MAX} = (125°C - T_{AMAX})/ \theta_{JA}$

Table 22: Package Thermal Characteristics[a]

Package Description				θ_{JA} (°C/W)			θ_{JC} (°C/W)
Name	Package Code	Package Type	Pin Count	0 LFM	200 LFM	400 LFM	
ArcticLink III BX5	FO	WLCSP (4.5 mm x 4.5 mm)	120	31.8	29.1	28.2	8.0

a. Contact QuickLogic for θ_{JA} values.

Power Consumption

Table 23 shows the power consumption in various operating modes. The minimum PCLK possible is assumed for these measurements.

Table 23: BX5B3D Power Consumption (mW) at 60 fps[a]

Resolution	Display Width (pixels)	Display Height (pixels)	BX5B3D	
			18 bpp	24 bpp
QVGA	320	240	130.1	131.6
VGA	640	480	133.6	135.1
WVGA	854	480	136.5	138.6
PAL	768	576	135.9	137.4
SVGA	800	600	136.4	138.0
XGA	1,024	768	141.1	142.7
HD 720	1,280	720	142.8	144.4
WXGA	1,366	768	144.5	146.2
SXGA	1,280	960	148.0	149.6
SXGA	1,280	1,024	149.2	150.9
SXGA+	1,400	1,050	150.9	152.6
UXGA	1,600	1,200	157.9	175.7
HD 1080	1,920	1,080	174.2	177.8
WUXGA	1,920	1,200	177.9	181.5

a. MIPI DBI command mode is limited to FWVGA (854x480) maximum.

Signal Description

Table 24 provides the signal descriptions for the ArcticLink III BX5B3D device.

Table 24: ArcticLink III BX5B3D Signal Description

Name	Direction	Description	Voltage Bank
MIPI Interface Signals			
MIPI RX			
MIPI_RX_DPCK	IN	MIPI/DSI differential input clock.	1.2V
MIPI_RX_DNCK			
MIPI_RX_DP0	I/O	MIPI/DSI differential input (bidirectional mode support) data lane 0.	1.2V
MIPI_RX_DN0			
MIPI_RX_DP1	IN	MIPI/DSI differential input data lane 1.	1.2V
MIPI_RX_DN1			
MIPI_RX_DP2	IN	MIPI/DSI differential input data lane 2.	1.2V
MIPI_RX_DN2			
MIPI_RX_DP3	IN	MIPI/DSI differential input data lane 3.	1.2V
MIPI_RX_DN3			
MIPI_RX_VDD12_D	PWR	MIPI/DPHY lane I/O power supply (Client).	1.2V
MIPI_RX_VDD12_B	PWR	MIPI/DPHY BIAS power supply (Client).	1.2V
MIPI_RX_VDD12_P	PWR	MIPI/DPHY PLL power supply (Client).	1.2V
LVDS CH1/CH2 TX			
LVDS_CH1_CK_P	OUT	LVDS CH1 differential output clock.	3.3V
LVDS_CH1_CK_N			
LVDS_CH1_L0_P	OUT	LVDS CH1 differential output data lane 0.	3.3V
LVDS_CH1_L0_N			
LVDS_CH1_L1_P	OUT	LVDS CH1 differential output data lane 1.	3.3V
LVDS_CH1_L1_N			
LVDS_CH1_L2_P	OUT	LVDS CH1 differential output data lane 2.	3.3V
LVDS_CH1_L2_N			
LVDS_CH1_L3_P	OUT	LVDS CH1 differential output data lane 3.	3.3V
LVDS_CH1_L3_N			
LVDS_CH2_CK_P	OUT	LVDS CH2 differential output clock.	3.3V
LVDS_CH2_CK_N			
LVDS_CH2_L0_P	OUT	LVDS CH2 differential output data lane 0.	3.3V
LVDS_CH2_L0_N			
LVDS_CH2_L1_P	OUT	LVDS CH2 differential output data lane 1.	3.3V
LVDS_CH2_L1_N			
LVDS_CH2_L2_P	OUT	LVDS CH2 differential output data lane 2.	3.3V
LVDS_CH2_L2_N			

Table 24: ArcticLink III BX5B3D Signal Description *(Continued)*

Name	Direction	Description	Voltage Bank
LVDS_CH2_L3_P	OUT	LVDS CH2 differential output data lane 3.	3.3V
LVDS_CH2_L3_N			
LVDS_DVDD	PWR	LVDS lane I/O power supply (Host).	3.3V
System Control and GPIOs			
GPIO<8>	I/O	Unused.	DVDD_1[a]
SPI_SCLK/GPIO<2>	I/O	SPI clock.	DVDD_1[a]
SPI_SDO/GPIO<3>	I/O	SPI MOSI.	DVDD_1[a]
SPI_SDI/GPIO<6>	I/O	SPI MISO.	DVDD_1[a]
SPI_SS/GPIO<7>	I/O	SPI Slave select.	DVDD_1[a]
I2C_SDA/GPIO<4>	I/O	I^2C interface data input/output signal (OD).	DVDD_0[a]
I2C_SCL/GPIO<5>	I/O	I^2C interface clock signal (OD).	DVDD_0[a]
PWM_1/ GPIO<0>	I/O	Backlight control 1.	DVDD_0[a]
PWM_2/ GPIO<1>	I/O	Backlight control 2.	DVDD_0[a]
SYS_CLK	IN	System clock.	DVDD_3
SYS_RST_N	IN	System reset (active low).	DVDD_3
Power and Ground			
VDD	PWR	Core voltage.	1.2V
VSS	GND	Ground pin.	GND
PLL_VDDA	PWR	PLL supply voltage.	1.2V
PLL_VSSA	GND	PLL supply ground.	GND
DVDD_0	PWR	VDD_0 power supply.	1.8V
DVDD_1	PWR	VDD_1 power supply.	1.8/2.5/3.3V
DVDD_3	PWR	VDD_3 power supply.	1.8/2.5/3.3V

a. Function of the pin is software configurable.

Pinout Table

Definitions:

- Ball – Ball name
- Signal – Signal name
- Voltage – Voltage tolerance for this ball
- Type – Pad characteristics
  - I/O – Input/Output pin
  - IN – Input only pin
  - OUT – Output only pin
  - OD – Open drain
  - PWR – Power supply pin
  - RS – Reserved
- Tie-off – Recommended connection if pin is not used
  - GND – Ground pin, tie this pin to GND
  - NC – No connect, do not connect to this pin (keep floating)

Table 25: BX5B3D – CSSP 120 0.4 mm Ball (4.5 mm x 4.5 mm) WLCSP Pinout Table

Ball	Signal	Voltage	Type	Tie-Off
A1	LVDS_CH1_L3_P	3.3V	OUT	--
A2	LVDS_CH1_L3_N	3.3V	OUT	--
A3	GND(RFU)	--	RFU	--
A4	GND(RFU)	--	RFU	--
A5	GND(RFU)	--	RFU	--
A6	MIPI_RX_DP3	1.2V	IN	--
A7	MIPI_RX_DP2	1.2V	IN	--
A8	MIPI_RX_DNCK	1.2V	IN	--
A9	MIPI_RX_DN1	1.2V	IN	--
A10	MIPI_RX_DN0	1.2V	IO	--
A11	PWM_1/GPIO<0>	1.8V	IO	--
B1	LVDS_CH1_L2_P	3.3V	OUT	--
B2	LVDS_CH1_L2_N	3.3V	OUT	--
B3	GND(RFU)	--	RFU	--
B4	GND(RFU)	--	RFU	--
B5	GND(RFU)	--	RFU	--
B6	MIPI_RX_DN3	1.2V	IN	--
B7	MIPI_RX_DN2	1.2V	IN	--
B8	MIPI_RX_DPCK	1.2V	IN	--

Table 25: BX5B3D – CSSP 120 0.4 mm Ball (4.5 mm x 4.5 mm) WLCSP Pinout Table *(Continued)*

Ball	Signal	Voltage	Type	Tie-Off
B9	MIPI_RX_DP1	1.2V	IN	--
B10	MIPI_RX_DP0	1.2V	IO	--
B11	PWM_2/GPIO<1>	1.8V	IO	--
C1	LVDS_CH1_CK_P	3.3V	OUT	--
C2	LVDS_CH1_CK_N	3.3V	OUT	--
C3	GND	VSS	PWR	--
C4	GND(RFU)	--	RFU	--
C5	GND(RFU)	--	RFU	--
C6	GND(RFU)	--	RFU	--
C7	V1P2 (MIPI_RX_VDD12_D)	1.2V	PWR	--
C8	V1P2 (MIPI_RX_VDD12_D)	1.2V	PWR	--
C9	GND	VSS	PWR	--
C10	I2C_SDA/GPIO<4>	1.8V	OD or IO[a]	--
C11	I2C_SCL/GPIO<5>	1.8V	OD or IO[a]	--
D1	LVDS_CH1_L1_P	3.3V	OUT	--
D2	LVDS_CH1_L1_N	3.3V	OUT	--
D3	V3P3 (LVDS_DVDD)	3.3V	PWR	--
D4	V1P8(RFU)	--	RFU	--
D5	V1P2	VDD	PWR	--
D6	GND(RFU)	--	RFU	--
D7	GND	VSS	PWR	--
D8	V1P2	VDD	PWR	--
D9	V1P8	DVDD_0	PWR	--
D10	SPI_SDO/GPIO<3>	DVDD_1	OUT or IO[a]	--
D11	SPI_SCLK/GPIO<2>	DVDD_1	OUT or IO[a]	--
E1	LVDS_CH1_L0_P	LVDS_DVDD	OUT	--
E2	LVDS_CH1_L0_N	LVDS_DVDD	OUT	--
E3	GND	VSS	PWR	--
E4	BALL NOT PRESENT			
E5	GND	VSS	PWR	--
E6	V1P2	VDD	PWR	--
E7	GND	VSS	PWR	--
E8	V1P8/V2P5/V3P3	DVDD_1	PWR	--
E9	GPIO<8>	DVDD_1	I/O	GND
E10	SPI_SS/GPIO<7>	DVDD_1	OUT or IO[a]	--
E11	SPI_SDI/GPIO<6>	DVDD_1	IN or IO[a]	--
F1	LVDS_CH2_L3_N	3.3V	OUT	--
F2	LVDS_CH2_L3_P	3.3V	OUT	--
F3	V3P3 (LVDS_DVDD)	3.3V	PWR	--
F4	V1P2	VDD	PWR	--

Table 25: BX5B3D – CSSP 120 0.4 mm Ball (4.5 mm x 4.5 mm) WLCSP Pinout Table *(Continued)*

Ball	Signal	Voltage	Type	Tie-Off
F5	GND	VSS	PWR	--
F6	GND	VSS	PWR	--
F7	V1P2	VDD	PWR	--
F8	V1P2 (MIPI_RX_VDD12_B)	1.2V	PWR	--
F9	V1P2 (MIPI_RX_VDD12_P)	1.2V	PWR	--
F10	DNC	--	RFU	--
F11	DNC	--	RFU	--
G1	LVDS_CH2_L2_P	3.3V	OUT	--
G2	LVDS_CH2_L2_N	3.3V	OUT	--
G3	GND	VSS	PWR	--
G4	V3P3 (LVDS_DVDD)	3.3V	PWR	--
G5	V1P8/V2P5/V3P3	DVDD_3	PWR	--
G6	V1P2(RFU)	--	RFU	--
G7	GND	VSS	PWR	--
G8	V1P2(RFU)	--	RFU	--
G9	GND	VSS	PWR	--
G10	DNC	--	RFU	--
G11	DNC	--	RFU	--
H1	LVDS_CH2_CK_N	3.3V	OUT	--
H2	LVDS_CH2_CK_P	3.3V	OUT	--
H3	LVDS_CH2_L0_N	3.3V	OUT	--
H4	GND	VSS	PWR	--
H5	GND	PLL_VSSA	PWR	--
H6	V1P2	VDD	PWR	--
H7	V1P8(RFU)	--	RFU	--
H8	V1P2	VDD	PWR	--
H9	V1P2(RFU)	--	RFU	--
H10	DNC	--	RFU	--
H11	DNC	--	RFU	--
J1	LVDS_CH2_L1_N	3.3V	OUT	--
J2	LVDS_CH2_L1_P	3.3V	OUT	--
J3	LVDS_CH2_L0_P	3.3V	OUT	--
J4	V1P2	PLL_VDDA	PWR	--
J5	GND(RFU)	--	RFU	--
J6	GND	VSS	PWR	--
J7	V1P2(RFU)	--	RFU	--
J8	GND	VSS	PWR	--
J9	GND(RFU)	--	RFU	--
J10	DNC	--	RFU	--
J11	DNC	--	RFU	--

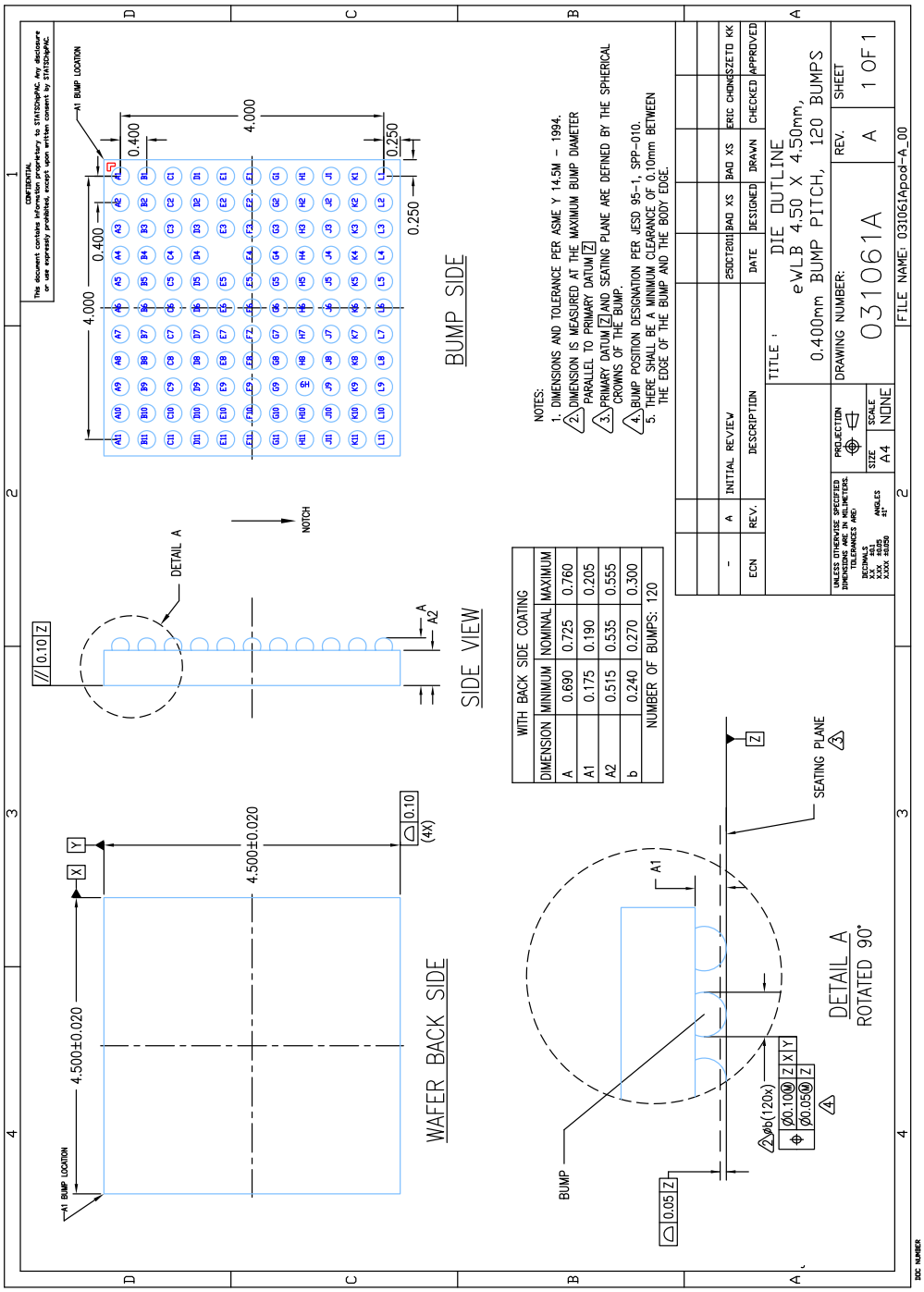
Table 25: BX5B3D – CSSP 120 0.4 mm Ball (4.5 mm x 4.5 mm) WLCSP Pinout Table *(Continued)*

Ball	Signal	Voltage	Type	Tie-Off
K1	SYS_RST_N	DVDD_3	IN	--
K2	GND(RFU)	--	RFU	--
K3	GND(RFU)	--	RFU	--
K4	GND(RFU)	--	RFU	--
K5	GND(RFU)	--	RFU	--
K6	GND(RFU)	--	RFU	--
K7	GND(RFU)	--	RFU	--
K8	GND(RFU)	--	RFU	--
K9	GND(RFU)	--	RFU	--
K10	DNC	--	RFU	--
K11	DNC	--	RFU	--
L1	SYS_CLK	DVDD_3	IN	--
L2	GND(RFU)	--	RFU	--
L3	GND(RFU)	--	RFU	--
L4	GND(RFU)	--	RFU	--
L5	GND(RFU)	--	RFU	--
L6	GND(RFU)	--	RFU	--
L7	GND(RFU)	--	RFU	--
L8	GND(RFU)	--	RFU	--
L9	GND(RFU)	--	RFU	--
L10	GND(RFU)	--	RFU	--
L11	GND(RFU)	--	RFU	--

a. Configuration-dependent.

Mechanical Drawing

Figure 15: BX5B3D Device – CSSP 120 0.4 mm Ball (4.5 mm x 4.5 mm) WLCSP Mechanical Drawing



Reference Schematic

Figure 16: BX5B3D – CSSP 120 0.4 mm Ball (4.5 mm x 4.5 mm) WLCSP Reference Schematic (1 of 2)

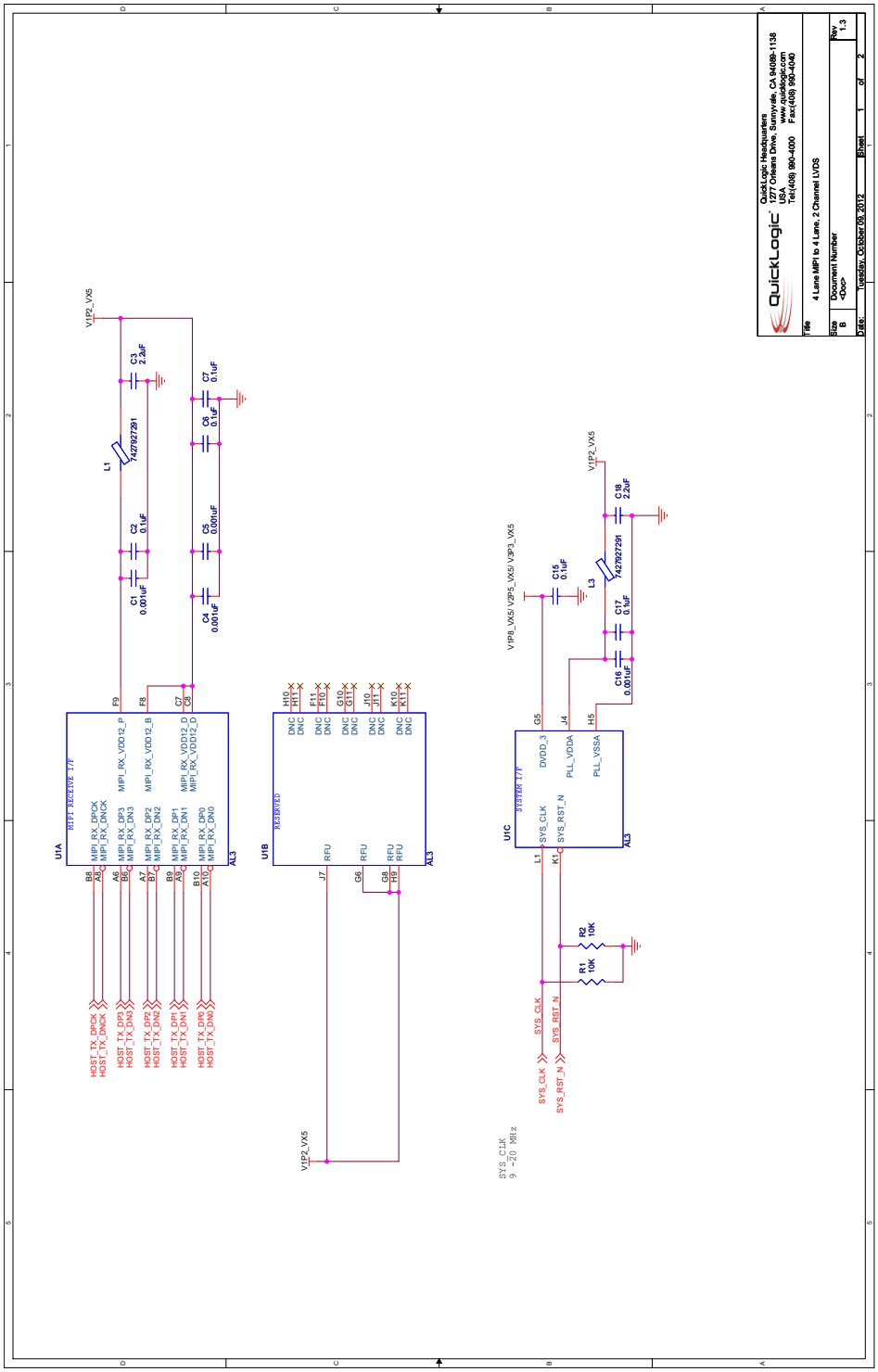
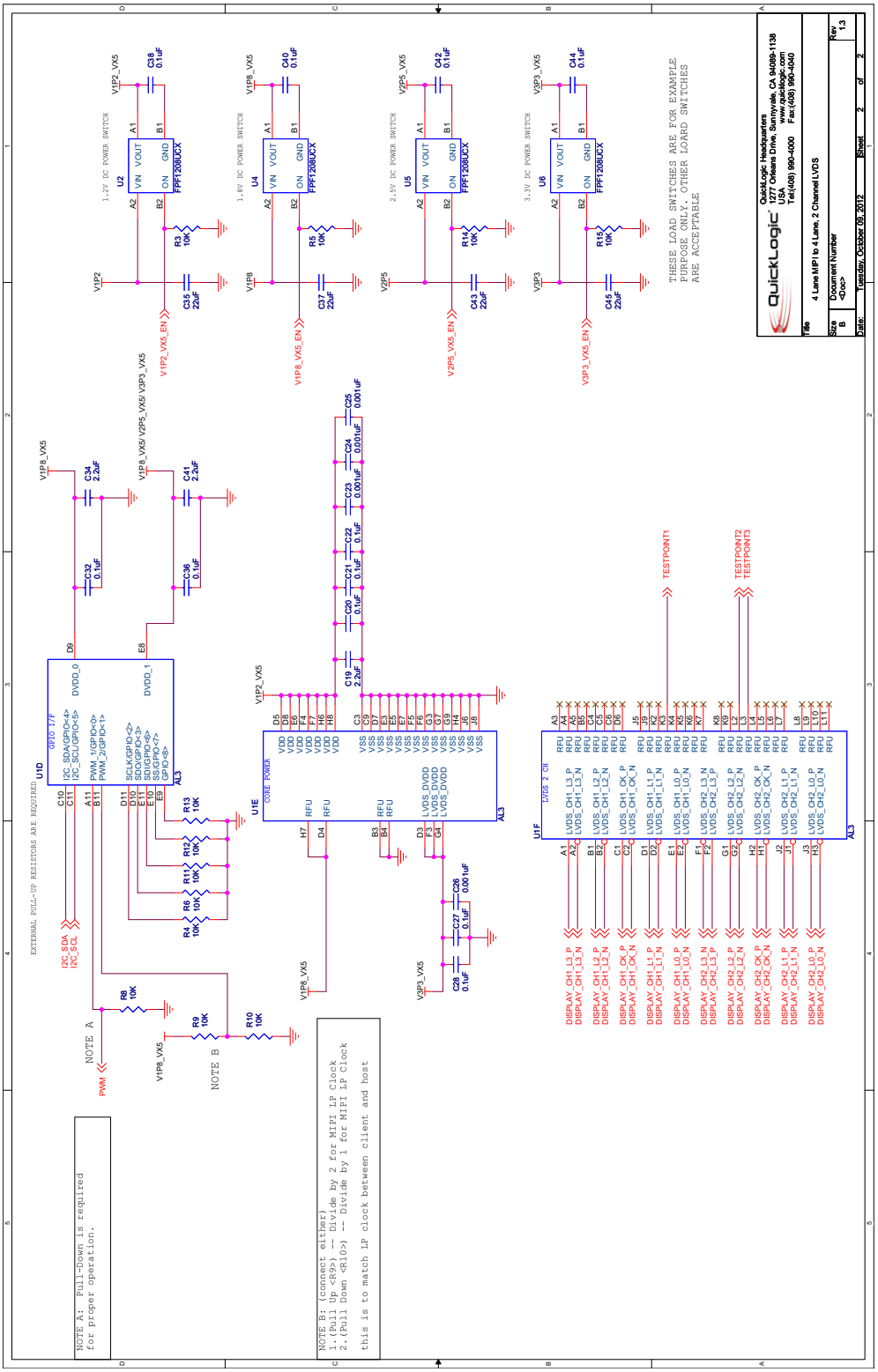


Figure 17: BX5B3D – CSSP 120 0.4 mm Ball (4.5 mm x 4.5 mm) WLCSP Reference Schematic (2 of 2)



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Revision History

Revision	Date	Originator and Comments
1.0	October 2012	Initial production release.
1.1	October 2012	Updated Recommended Operating Conditions table.
1.2	December 2012	Updated Recommended Operating Conditions table, GPIO Input Electrical Characteristics table, and System Clock Frequency table. Added MIPI and LVDS timing information.
1.3	March 2012	Paul Karazuba and Kathleen Bylsma Added part number format to cover page. Updated Power-On Sequencing
1.4	May 2013	Paul Karazuba and Kathleen Bylsma Updated commercial temperature range. Changed E4 in pinout table to BALL NOT PRESENT. Clarification of PWM_clk divider.

Revision	Date	Originator and Comments
1.5	June 2013	Paul Karazuba and Kathleen Bylsma – Changed I2C_SCL Clock Frequency min. and max. values from 400 kHz - 1000 kHz to 100 kHz to 400 kHz. – Clarification of PWM_clk divider. – Updated pin description for A11, B11, C10, C11, D10, D11, E10, and E11. – Added section GPIO and Hardware Configurable Pins. – Updated Contact Information section.
1.6	June 2013	Paul Karazuba and Kathleen Bylsma Updated reference schematic.
1.7	July 2014	Lisa Pham and Kathleen Bylsma – Updated Table 1: A2F Bus Address Map changing *Reserved* to *Clock and Reset* and added a cross reference to the Clock and Reset Registers section. – Added pin numbers to LS description in I2C Slave section. – Added description to Mux and Formatter 1/2/3 in the Register Descriptions section. – Combined bits [14-12] in the Mux and Formatter 1/2/3 table.

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