QuickRAM Datasheet

QuickRAM Antifuse FPGA Combining Performance, Density and Embedded RAM

Device Highlights

High Performance & High Density

- Up to 90,000 usable PLD gates with up to 308 I/Os
- 300 MHz 16-bit counters, 400 MHz datapaths, 160+ MHz FIFOs
- 0.35 µm four-layer metal non-volatile CMOS process

High Speed Embedded SRAM

- Up to 22 dual-port RAM modules, organized in user-configurable 1,152 bit blocks
- 5 ns access times, each port independently accessible
- Fast and efficient for FIFO, RAM, and ROM functions

Easy to Use/Fast Development Cycles

- 100% routable with 100% utilization and complete pin-out stability
- Variable-grain logic cells provide high performance and 100% utilization
- Comprehensive design tools include high-quality Verilog/VHDL synthesis

Advanced I/O Capabilities

- Interfaces with 3.3 V and 5.0 V devices
- PCI compliant with 3.3 V and 5.0 V busses for -1/-2/-3/-4 speed grades
- Full JTAG boundary scan
- I/O cells with individually controlled registered input path and output enables

Up to 308 I/O Pins

- Up to 308 bi-directional input/output pins, PCI-compliant for 5.0 V and 3.3 V buses for -1/-2/-3/-4 speed grades
- Eight high-drive input/distributed network pins

Eight Low-Skew Distributed Networks

- Two array clock/control networks are available to the logic cell flip-flop; clock, set, and reset inputs — each can be driven by an input-only pin
- Six global clock/control networks available to the logic cell; F1, clock, set, and reset inputs and the data input, I/O register clock, reset, and enable inputs as well as the output enable control—each can be driven by an input-only, I/O pin, any logic cell output, or I/O cell feedback

High Performance Silicon

- Input + logic cell + output total delays under 6 ns
- Data path speeds over 400 MHz
- Counter speeds over 300 MHz
- FIFO speeds over 160+ MHz

Figure 1: QuickRAM Block Diagram

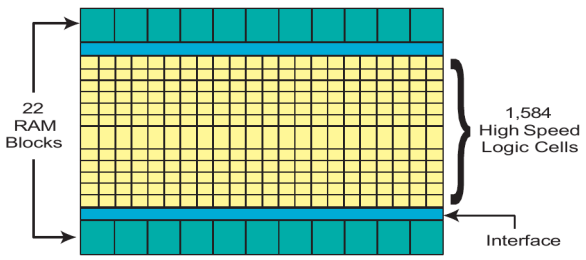

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Table 1: QuickRAM Product Family Members

		QL4009	QL4016	QL4036	QL4058	QL4090
Max Gates		44,964	61,820	97,128	131,328	176,608
Logic Array		16 x 16	20 x 16	28 x 24	36 x 28	44 x 36
Logic Cells		160	320	672	1,008	1,584
Max Flip-Flops		242	438	876	1,260	1,900
Max I/O		74	110	196	244	308
RAM Modules		8	10	14	18	22
RAM Bits		9,216	11,520	16,128	20,736	25,344
Packages	QFN	-	56	-	-	-
	TQFP	100	100/144	144	-	-
	PQFP	-	-	208*	208*	208*
	PBGA	-	-	256	456	456

Table 2: Max I/O per Device/Package Combination

Device	56	100	144	208	256	456
	QFN	TQFP	TQFP	PQFP	PBGA	PBGA
QL4009	-	74	-	-	-	-
QL4016	32	74	110	-	-	-
QL4036	-	-	110	166*	196	-
QL4058	-	-	-	166*	-	244
QL4090	-	-	-	166*	-	308

Note * 208-pin QFP package is in long-term obsolescence and not recommended for new designs.

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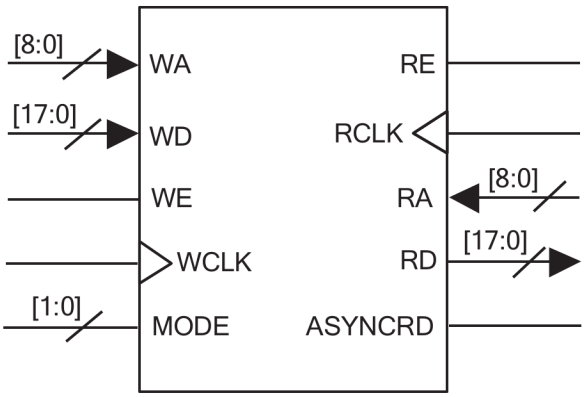
Architecture Overview

The QuickRAM™ family of antifuse FPGAs offers non-volatile programmable logic in combination with Dual-Port SRAM modules. The family offers up to 90,000 usable PLD gates. QuickRAM antifuse FPGAs are fabricated on a 0.35 µm four-layer metal process using QuickLogic's patented ViaLink™ technology to provide a unique combination of high performance, high density, low cost, and extreme ease-of-use.

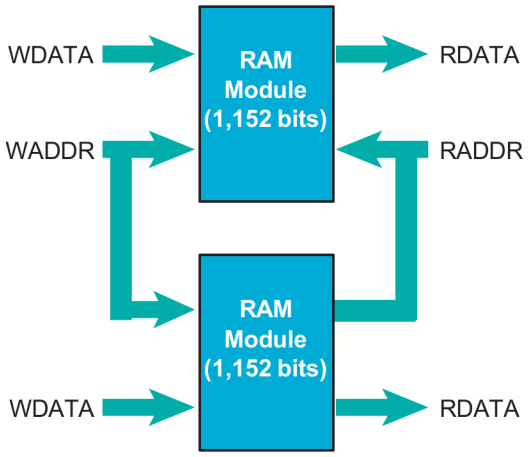
The QuickRAM family contains a range of 160 to 1,584 logic cells and 8 to 22 dual port RAM Modules (see **Figure 1**). Each RAM Module has 1,152 RAM bits, for a total ranging from 9,216 to 25,344 bits (see **Table 1**). RAM Modules are dual port (one read port, one write port) and can be configured into one of four modes: 64 (deep) x18 (wide), 128x9, 256x4, or 512x2 (see **Figure 2**). With a maximum of 308 I/Os, the QuickRAM antifuse FPGAs are available in many device/package combinations (see Table 2).

Figure 2: QuickRAM Module



Designers can cascade multiple RAM Modules to increase the depth or width allowed in single modules by connecting corresponding address lines together and dividing the words between modules (see **Figure 3**). This approach allows up to 512-deep configurations as large as 16 bits wide in the smallest QuickRAM device and 44 bits wide in the largest device.

Figure 3: QuickRAM Module Bits



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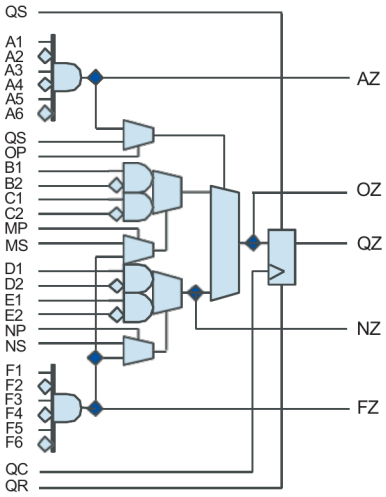
Software support for the complete QuickRAM family is provided through two primary packages:

- **Yosys / YosysHQ** — Offers synthesis support for pASIC3, QuickRAM, and Eclipse devices.
- **QuickWorks™** — Takes the synthesized netlist through place-and-route, static timing analysis (STA), power calculation, and back-annotation, producing the final programming file. Simulation support is available through a range of third-party tools, including **Aldec, Mentor, Cadence**, and others.

The QuickLogic variable grain logic cell features up to 16 simultaneous inputs and 5 outputs within a cell that can be fragmented into 5 independent cells. Each cell has a fan-in of 29 including register and control lines (see **Figure 4**).

Figure 4: QuickRAM Logic Cell



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Electrical Specifications

AC Characteristics at V_{CC} = 3.3 V, T_A = 25° C (K = 1.00)

To calculate delays, multiply the appropriate K factor from **Table 12** by the numbers provided in **Table 3** through **Table 10**.

Table 3: Logic Cell

Symbol	Parameter	Propagation Delays (ns) Fanout				
		1	2	3	4	5
t_{PD}	Combinatorial Delay[a]	1.4	1.7	1.9	2.2	3.2
t_{SU}	Setup Time[a]	1.7	1.7	1.7	1.7	1.7
t_H	Hold Time	0.0	0.0	0.0	0.0	0.0
t_{CLK}	Clock to Q Delay	0.7	1.0	1.2	1.5	2.5
t_{CWHI}	Clock High Time	1.2	1.2	1.2	1.2	1.2
t_{CWLO}	Clock Low Time	1.2	1.2	1.2	1.2	1.2
t_{SET}	Set Delay	1.0	1.3	1.5	1.8	2.8
t_{RESET}	Reset Delay	0.8	1.1	1.3	1.6	2.6
t_{SW}	Set Width	1.9	1.9	1.9	1.9	1.9
t_{RW}	Reset Width	1.8	1.8	1.8	1.8	1.8

a. These limits are derived from a representative selection of the slowest paths through the QuickRAM logic cell including typical net delays. Worst case delay values for specific paths should be determined from timing analysis of your particular design.

Table 4: RAM Cell Synchronous Write Timing

Symbol	Parameter	Propagation Delays (ns) Fanout				
		1	2	3	4	5
t_{SWA}	WA Setup Time to WCLK	1.0	1.0	1.0	1.0	1.0
t_{HWA}	WA Hold Time to WCLK	0.0	0.0	0.0	0.0	0.0
t_{SWD}	WD Setup Time to WCLK	1.0	1.0	1.0	1.0	1.0
t_{HWD}	WD Hold Time to WCLK	0.0	0.0	0.0	0.0	0.0
t_{SWE}	WE Setup Time to WCLK	1.0	1.0	1.0	1.0	1.0
t_{HWE}	WE Hold Time to WCLK	0.0	0.0	0.0	0.0	0.0
t_{WCRD}	WCLK to RD (WA=RA)[a]	5.0	5.3	5.6	5.9	7.1

a. Stated timing for worst case Propagation Delay over process variation at V_{CC} = 3.3 V and T_A = 25°C. Multiply by the appropriate Delay Factor, K, for speed grade, voltage and temperature settings as specified in the Operating Range.

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Table 5: RAM Cell Synchronous Read Timing

Symbol	Parameter	Propagation Delays (ns) Fanout				
		1	2	3	4	5
t_{SRA}	RA Setup Time to RCLK	1.0	1.0	1.0	1.0	1.0
t_{HRA}	RA Hold Time to RCLK	0.0	0.0	0.0	0.0	0.0
t_{SRE}	RE Setup Time to RCLK	1.0	1.0	1.0	1.0	1.0
t_{HRE}	RE Hold Time to RCLK	0.0	0.0	0.0	0.0	0.0
t_{RCRD}	RCLK to RD[a]	4.0	4.3	4.6	4.9	6.1

a. Stated timing for worst case Propagation Delay over process variation at V_{CC} = 3.3 V and T_A = 25°C. Multiply by the appropriate Delay Factor, K, for speed grade, voltage and temperature settings as specified in the Operating Range.

Table 6: RAM Cell Asynchronous Read Timing

Symbol	Parameter	Propagation Delays (ns) Fanout				
		1	2	3	4	5
RPDRD	RA to RD[a]	3.0	3.3	3.6	3.9	5.1

a. Stated timing for worst case Propagation Delay over process variation at V_{CC} = 3.3 V and T_A = 25°C. Multiply by the appropriate Delay Factor, K, for speed grade, voltage and temperature settings as specified in the Operating Range.

Table 7: Input-Only/Clock Cells

Symbol	Parameter	Propagation Delays (ns) Fanout[a]						
		1	2	3	4	8	12	24
t_{IN}	High Drive Input Delay	1.5	1.6	1.8	1.9	2.4	2.9	4.4
t_{INI}	High Drive Input, Inverting Delay	1.6	1.7	1.9	2.0	2.5	3.0	4.5
t_{ISU}	Input Register Set-Up Time	3.1	3.1	3.1	3.1	3.1	3.1	3.1
t_{IH}	Input Register Hold Time	0.0	0.0	0.0	0.0	0.0	0.0	0.0
t_{ICLK}	Input Register Clock To Q	0.7	0.8	1.0	1.1	1.6	2.1	3.6
t_{IRST}	Input Register Reset Delay	0.6	0.7	0.9	1.0	1.5	2.0	3.5
t_{IESU}	Input Register Clock Enable Setup Time	2.3	2.3	2.3	2.3	2.3	2.3	2.3
t_{IEH}	Input Register Clock Enable Hold Time	0.0	0.0	0.0	0.0	0.0	0.0	0.0

a. Stated timing for worst case Propagation Delay over process variation at V_{CC} = 3.3 V and T_A = 25°C. Multiply by the appropriate Delay Factor, K, for speed grade, voltage and temperature settings as specified in **Table 12**.

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Table 8: Clock Cells

Symbol	Parameter	Propagation Delays (ns) Fanout[a]						
		1	2	3	4	8	10	11
t_{ACK}	Array Clock Delay	1.2	1.2	1.3	1.3	1.5	1.6	1.7
t_{GCKP}	Global Clock Pin Delay	0.7	0.7	0.7	0.7	0.7	0.7	0.7
t_{GCKB}	Global Clock Buffer Delay	0.8	0.8	0.9	0.9	1.1	1.2	1.3

a. The array distributed networks consist of 40 half columns and the global distributed networks consist of 44 half columns, each driven by an independent buffer. The number of half columns used does not affect clock buffer delay. The array clock has up to 8 loads per half column. The global clock has up to 11 loads per half column.

Table 9: I/O Cell Input Delays

Symbol	Parameter	Propagation Delays (ns) Fanout[a]					
		1	2	3	4	8	10
$t_{I/O}$	Input Delay (bidirectional pad)	1.3	1.6	1.8	2.1	3.1	3.6
t_{ISU}	Input Register Set-Up Time	3.1	3.1	3.1	3.1	3.1	3.1
t_{IH}	Input Register Hold Time	0.0	0.0	0.0	0.0	0.0	0.0
t_{IOCLK}	Input Register Clock to Q	0.7	1.0	1.2	1.5	2.5	3.0
t_{IORST}	Input Register Reset Delay	0.6	0.9	1.1	1.4	2.4	2.9
t_{IESU}	Input Register Clock Enable Set-Up Time	2.3	2.3	2.3	2.3	2.3	2.3
t_{IEH}	Input Register Clock Enable Hold Time	0.0	0.0	0.0	0.0	0.0	0.0

a. Stated timing for worst case Propagation Delay over process variation at V_{CC} = 3.3 V and T_A = 25°C. Multiply by the appropriate Delay Factor, K, for speed grade, voltage and temperature settings as specified in the Operating Range.

Table 10: I/O Cell Output Delays

Symbol	Parameter	Propagation Delays (ns) Output Load Capacitance (pF)				
		3	50	75	100	150
t_{OUTLH}	Output Delay Low to High	2.1	2.5	3.1	3.6	4.7
t_{OUTHL}	Output Delay High to Low	2.2	2.6	3.2	3.7	4.8
t_{PZH}	Output Delay Tri-state to High	1.2	1.7	2.2	2.8	3.9
t_{PZL}	Output Delay Tri-state to Low	1.6	2.0	2.6	3.1	4.2
t_{PHZ}	Output Delay High to Tri-state[a]	2.0	-	-	-	-
t_{PLZ}	Output Delay High to Tri-state[a]	1.2	-	-	-	-

a. The loads presented in **Figure 5** are used for t_{PXZ}:

Figure 5: Loads used for t_{PXZ}



DC Characteristics

The DC specifications are provided in **Table 11** through **Table 13**.

Table 11: Absolute Maximum Ratings

Parameter	Value	Parameter	Value
V_{CC} Voltage	-0.5 to 4.6 V	DC Input Current	±20 mA
V_{CCIO} Voltage	-0.5 to 7.0 V	ESD Pad Protection	±2000 V
Input Voltage	-0.5 V to V_{CCIO} +0.5 V	Storage Temperature	-65° C to +150° C
Latch-up Immunity	±200 mA	Lead Temperature	300° C

Table 12: Operating Range

Symbol	Parameter		Military		Industrial		Commercial		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V_{CC}	Supply Voltage		3.0	3.6	3.0	3.6	3.0	3.6	V
V_{CCIO}	I/O Input Tolerance Voltage		3.0	5.5	3.0	5.5	3.0	5.25	V
T_A	Ambient Temperature		-55	-	-40	85	0	70	°C
T_C	Case Temperature		-	125	-	-	-	-	°C
K	Delay Factor	-0 Speed Grade	0.42	2.03	0.43	1.90	0.46	1.85	n/a
		-1 Speed Grade	0.42	1.64	0.43	1.54	0.46	1.50	n/a
		-2 Speed Grade	0.42	1.37	0.43	1.28	0.46	1.25	n/a
		-3 Speed Grade			0.43	0.90	0.46	0.88	n/a
		-4 Speed Grade			0.43	0.82	0.46	0.80	n/a

Table 13: DC Characteristics

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{IH}	Input HIGH Voltage		0.5 V_{CC}	V_{CCIO} + 0.5	V
V_{IL}	Input LOW Voltage		-0.5	0.3 V_{CC}	V
V_{OH}	Output HIGH Voltage	I_{OH} = -12 mA	2.4	V_{CC}	V
		I_{OH} = -500 µA	0.9 V_{CC}	V_{CC}	V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA[a]		0.45	V
		I_{OL} = 1.5 mA		0.1 V_{CC}	V
I_I	I or I/O Input Leakage Current	V_I = V_{CCIO} or GND	-10	10	µA
I_{OZ}	3-State Output Leakage Current	V_I = V_{CCIO} or GND	-10	10	µA
C_I	Input Capacitance[b]			10	pF
	Output Short Circuit Current[c]	V_O = GND	-15	-180	mA
I_{OS}		V_O = V_{CC}	40	210	mA
I_{CC}	D.C. Supply Current[d]	V_I, V_{IO} = V_{CCIO} or GND	0.50 (typ)	2	mA
I_{CCIO}	D.C. Supply Current on V_{CCIO}		0	100	µA

a. Applies only to -1/-2/-3/-4 commercial grade devices. These speed grades are also PCI-compliant. All other devices have 8 mA IOL specifications.

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b. Capacitance is sample tested only. Clock pins are 12 pF maximum.

c. Only one output at a time. Duration should not exceed 30 seconds.

d. For -1/-2/-3/-4 commercial grade devices only. Maximum I_{CC} is 3 mA for -0 commercial grade and all industrial grade devices. and 5 mA for all military grade devices. For AC conditions, contact QuickLogic customer applications group.

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Kv and Kt Graphs

Figure 6: Voltage Factor vs. Supply Voltage

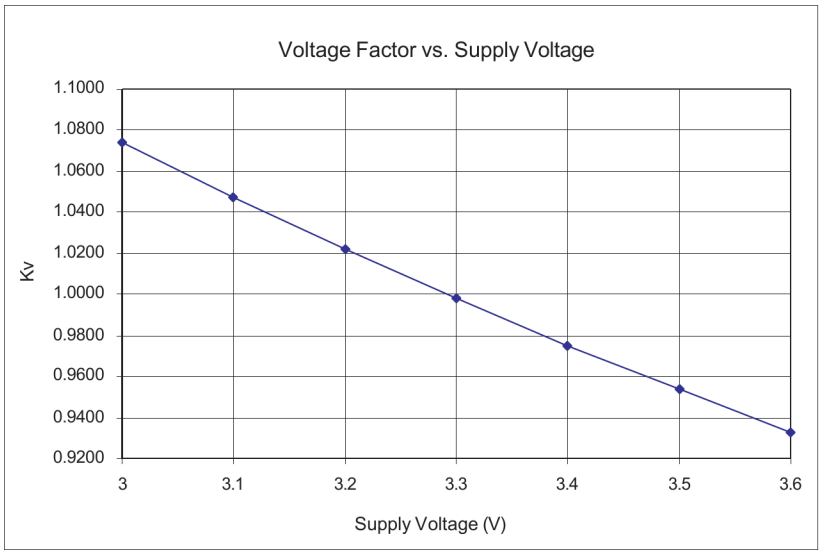
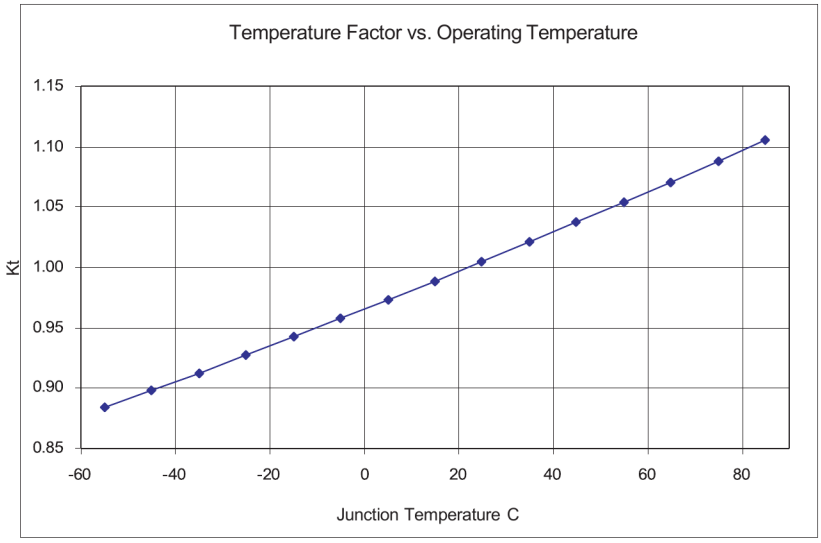


Figure 7: Temperature Factor vs. Operating Temperature



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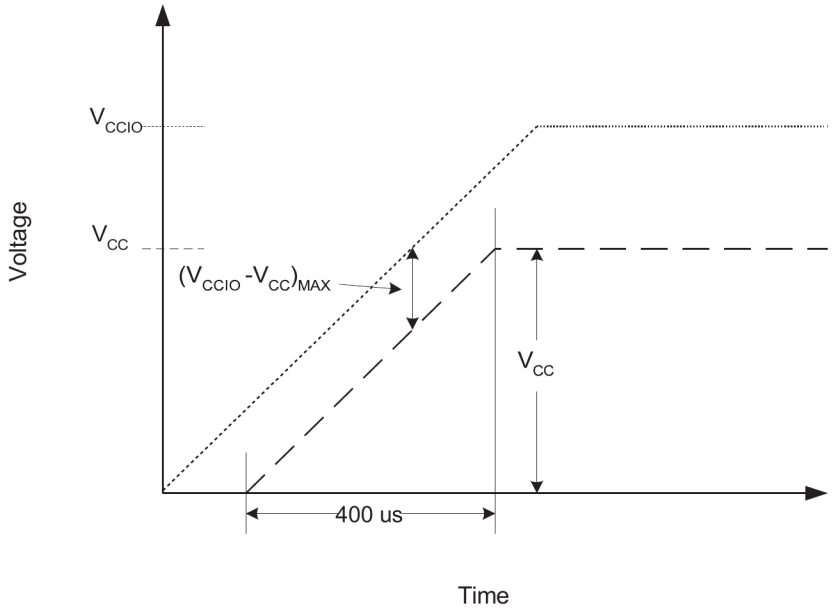
Power-Up Sequencing

Figure 8: Power-Up Requirements



When powering up a device, the V_{CC}/V_{CCIO} rails must take 400 µs or longer to reach the maximum value (refer to **Figure 7**).

NOTE: Ramping V_{CC}/V_{CCIO} to the maximum voltage faster than 400 µs can cause the device to behave improperly.

For users with a limited power budget, keep $(V_{CCIO} - V_{CC})_{MAX} \leq 500$ mV when ramping up the power supply.

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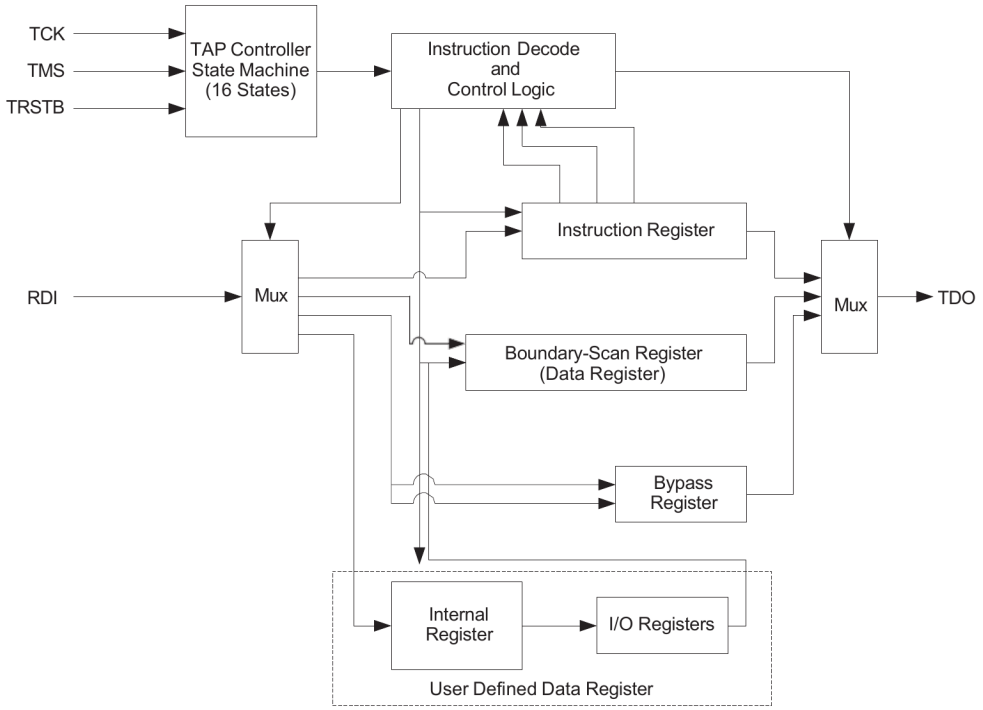
JTAG

Figure 9: JTAG Block Diagram



Microprocessors and Application Specific Integrated Circuits (ASICs) pose many design challenges, not the least of which concerns the accessibility of test points. The Joint Test Access Group (JTAG) formed in response to this challenge, resulting in IEEE standard 1149.1, the Standard Test Access Port and Boundary Scan Architecture.

The JTAG boundary scan test methodology allows complete observation and control of the boundary pins of a JTAG-compatible device through JTAG software. A Test Access Port (TAP) controller works in concert with the Instruction Register (IR); these allow users to run three required tests, along with several user-defined tests.

JTAG tests allow users to reduce system debug time, reuse test platforms and tools, and reuse subsystem tests for fuller verification of higher level system elements.

The 1149.1 standard requires the following three tests:

- **Extest Instruction.** The Extest Instruction performs a Printed Circuit Board (PCB) interconnect test. This test places a device into an external boundary test mode, selecting the boundary scan register to be connected between the TAP Test Data In (TDI) and Test Data Out (TDO) pins. Boundary scan cells are preloaded with test patterns (via the Sample/Preload Instruction), and input boundary cells capture the input data for analysis.
- **Sample/Preload Instruction.** The Sample/Preload Instruction allows a device to remain in its functional mode, while selecting the boundary scan register to be connected between the TDI and TDO pins. For this test, the boundary scan register can be accessed via a data scan operation, allowing users to sample the functional data entering and leaving the device.

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- **Bypass Instruction.** The Bypass Instruction allows data to skip a device boundary scan entirely, so the data passes through the bypass register. The Bypass instruction allows users to test a device without passing through other devices. The bypass register is connected between the TDI and TDO pins, allowing serial data to be transferred through a device without affecting the operation of the device.

Pin Descriptions

Table 14: Pin Descriptions

Pin	Function	Description
TDI/RSI	Test Data In for JTAG /RAM init. Serial Data In	Hold HIGH during normal operation. Connects to serial PROM data in for RAM initialization. Connect to V_{CC} if unused.
TRSTB/RRO	Active low Reset for JTAG /RAM init. reset out	Hold LOW during normal operation. Connects to serial PROM reset for RAM initialization. Connect to GND if unused.
TMS	Test Mode Select for JTAG	Hold HIGH during normal operation. Connect to V_{CC} if not used for JTAG.
TCK	Test Clock for JTAG	Hold HIGH or LOW during normal operation. Connect to V_{CC} or ground if not used for JTAG.
TDO/RCO	Test data out for JTAG /RAM init. clock out	Connect to serial PROM clock for RAM initialization. Must be left unconnected if not used for JTAG or RAM initialization.
STM	Special Test Mode	Must be grounded during normal operation.
I/ACLK	High-drive input and/or array network driver	Can be configured as either or both.
I/GCLK	High-drive input and/or global network driver	Can be configured as either or both.
I	High-drive input	Use for input signals with high fanout.
I/O	Input/Output pin	Can be configured as an input and/or output.
V_{CC}	Power supply pin	Connect to 3.3 V supply.
V_{CCIO}	Input voltage tolerance pin	Connect to 5.0 V supply if 5 V input tolerance is required, otherwise connect to 3.3 V supply.
GND	Ground pin	Connect to ground.
GND/THERM	Ground/Thermal pin	Available on 456-PBGA only. Connect to ground plane on PCB if heat sinking desired. Otherwise may be left unconnected.

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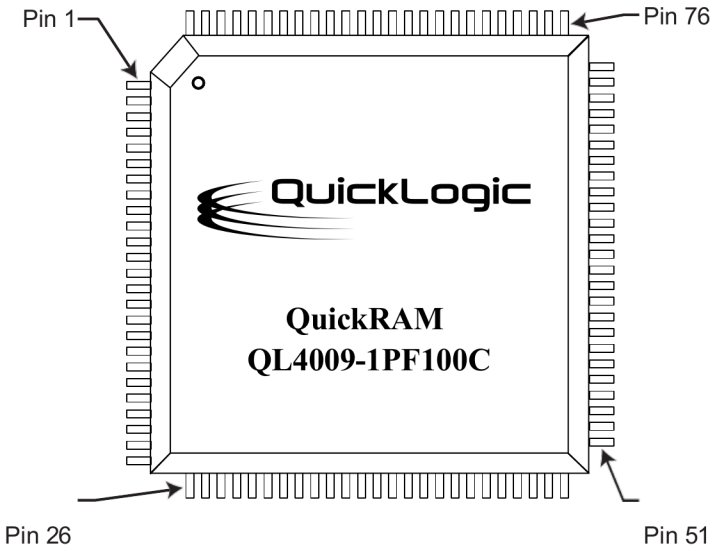
QL4009 – 100 TQFP Pinout Diagram

Figure 12: QL4009 – 100 Pin TQFP (Top View)



QL4009 – 100 TQFP Pinout Table

Table 17: QL4009 – 100 TQFP Pinout Table

100TQFP	Function	100TQFP	Function	100TQFP	Function	100TQFP	Function
1	I/O	26	TDI	51	I/O	76	TCK
2	I/O	27	I/O	52	I/O	77	STM
3	I/O	28	I/O	53	I/O	78	I/O
4	I/O	29	I/O	54	I/O	79	I/O
5	I/O	30	I/O	55	I/O	80	I/O
6	I/O	31	I/O	56	I/O	81	I/O
7	I/O	32	I/O	57	I/O	82	I/O
8	I/O	33	I/O	58	I/O	83	I/O
9	GND	34	I/O	59	GND	84	I/O
10	I/O	35	GND	60	I/O	85	GND
11	I	36	I/O	61	I	86	I/O
12	ACLK/I	37	I/O	62	ACLK/I	87	I/O
13	VCC	38	GND	63	VCC	88	GND
14	I	39	I/O	64	I	89	I/O
15	GCLK/I	40	I/O	65	GCLK/I	90	I/O
16	VCC	41	I/O	66	VCC	91	I/O
17	I/O	42	VCCIO	67	I/O	92	VCCIO
18	I/O	43	I/O	68	I/O	93	I/O
19	I/O	44	I/O	69	I/O	94	I/O
20	I/O	45	I/O	70	I/O	95	I/O
21	I/O	46	I/O	71	I/O	96	I/O
22	I/O	47	I/O	72	I/O	97	I/O
23	I/O	48	I/O	73	I/O	98	I/O
24	I/O	49	TRSTB	74	I/O	99	I/O
25	I/O	50	TMS	75	I/O	100	TDO

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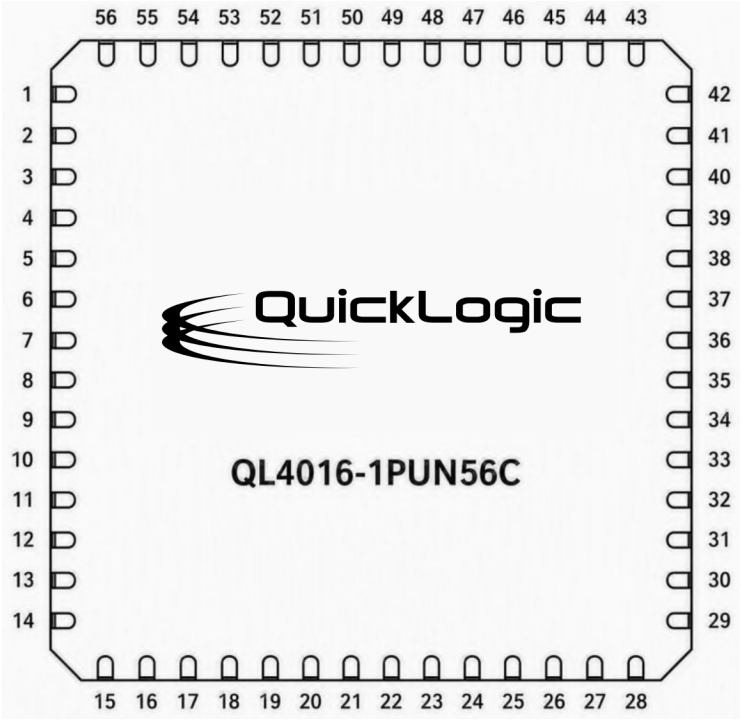
QL4016 – 56 QFN Pinout Diagram (Preliminary)

Figure 13: QL4016 – 56 Pin QFP (Top View)



QL4016 – 56 QFN Pinout Table (Preliminary)

Table 18: QL4016 – 56 QFN Pinout Table

56	Function	56	Function	56	Function	56	Function
1	TCK	15	I/O	29	TDI	43	I/O
2	STM	16	I/O	30	I/O	44	I/O
3	I/O	17	I/O	31	I/O	45	I/O
4	I/O	18	I/O	32	VCC	46	GND
5	VCC	19	GCLK/I	33	GND	47	I/O
6	I/O	20	ACLK/I	34	I/O	48	GCLK/I
7	I/O	21	GND	35	I/O	49	ACLK/I
8	GND	22	GCLK/I	36	I/O	50	GCLK/I
9	I/O	23	GCLK/I	37	VCCIO	51	GCLK/I
10	VCCIO	24	I/O	38	I/O	52	VCC
11	I/O	25	I/O	39	I/O	53	I/O
12	I/O	26	I/O	40	TRSTB	54	I/O
13	I/O	27	GND	41	TMS	55	I/O
14	TDO	28	I/O	42	I/O	56	I/O

Preliminary pinout — please confirm with QuickLogic before finalizing PCB layout.

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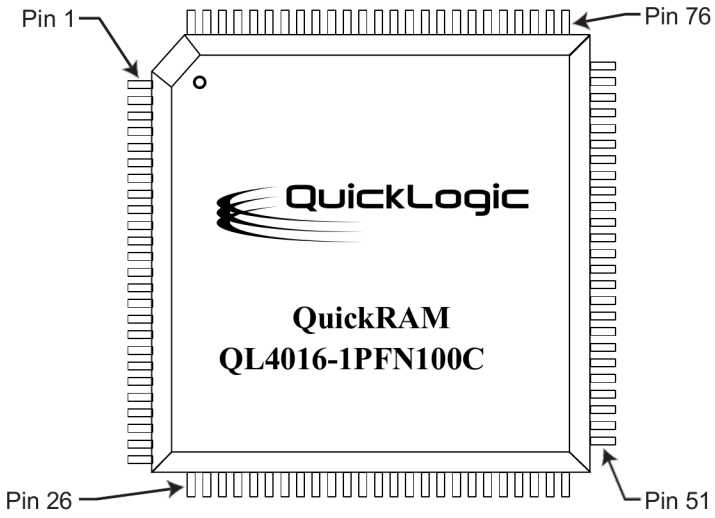
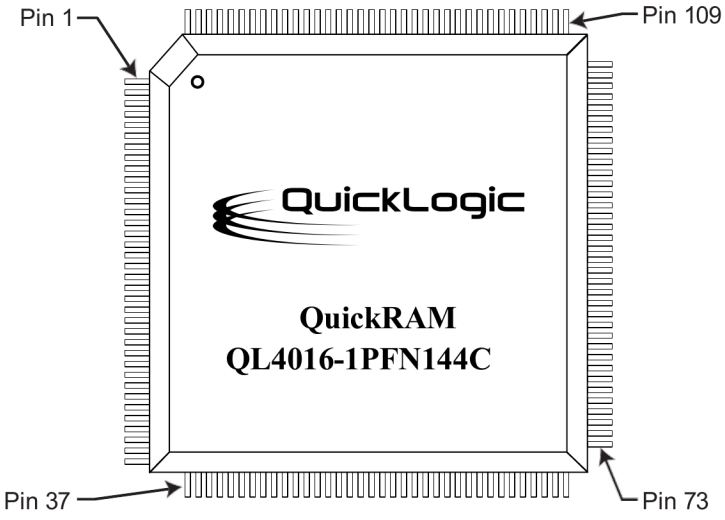
QL4016 – 100 TQFP Pinout Diagram

Figure 14: QL4016 – 100 Pin TQFP (Top View)



QL4016 – 144 TQFP Pinout Diagram

Figure 15: QL4016 – 144 Pin TQFP (Top View)



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QL4016 – 144 TQFP and 100 TQFP Pinout Table

Table 19: QL4016 – 144 TQFP and 100 TQFP Pinout Table

144TQFP	100TQFP	Function	144TQFP	100TQFP	Function	144TQFP	100TQFP	Function	144TQFP	100TQFP	Function
1	2	I/O	38	26	TDI	75	53	I/O	111	78	I/O
2	3	I/O	39	27	I/O	76	54	I/O	112	79	I/O
3	NC	I/O	40	28	I/O	77	55	I/O	113	80	I/O
4	4	I/O	41	29	I/O	78	NC	I/O	114	NC	VCC
5	NC	I/O	42	NC	VCC	79	NC	VCC	115	81	I/O
6	5	I/O	43	30	I/O	80	NC	I/O	116	82	I/O
7	NC	VCC	44	31	I/O	81	56	I/O	117	83	I/O
8	6	I/O	45	NC	I/O	82	NC	I/O	118	NC	I/O
9	NC	I/O	46	32	I/O	83	57	I/O	119	84	I/O
10	7	I/O	47	33	I/O	84	NC	I/O	120	NC	I/O
11	NC	I/O	48	NC	I/O	85	58	I/O	121	NC	I/O
12	NC	I/O	49	34	I/O	86	NC	I/O	122	85	GND
13	8	I/O	50	35	GND	87	59	GND	123	NC	I/O
14	NC	I/O	51	36	I/O	88	60	I/O	124	86	I/O
15	9	GND	52	NC	I/O	89	61	I	125	87	I/O
16	10	I/O	53	37	I/O	90	62	ACLK/I	126	88	GND
17	11	I	54	38	GND	91	63	VCC	127	89	I/O
18	12	ACLK/I	55	39	I/O	92	64	I	128	90	I/O
19	13	VCC	56	40	I/O	93	65	GCLK/I	129	91	I/O
20	14	I	57	41	I/O	94	66	VCC	130	92	VCCIO
21	15	GCLK/I	58	42	VCCIO	95	67	I/O	131	NC	I/O
22	16	VCC	59	NC	I/O	96	NC	I/O	132	93	I/O
23	17	I/O	60	43	I/O	NC	68	I/O	133	NC	I/O
24	18	I/O	61	44	I/O	97	NC	I/O	134	94	I/O
25	NC	I/O	62	45	I/O	98	69	I/O	135	NC	I/O
26	19	I/O	63	NC	I/O	99	NC	I/O	136	NC	I/O
27	NC	I/O	64	NC	I/O	100	70	I/O	NC	95	I/O
28	20	I/O	65	46	I/O	101	71	I/O	137	NC	I/O
29	21	I/O	66	NC	GND	102	NC	GND	138	NC	GND
30	NC	GND	67	NC	I/O	103	NC	I/O	139	96	I/O
31	NC	I/O	68	NC	I/O	104	72	I/O	140	97	I/O
32	22	I/O	69	47	I/O	105	NC	I/O	141	98	I/O
33	23	I/O	70	48	I/O	106	73	I/O	142	99	I/O
34	NC	I/O	71	49	TRSTB	107	74	I/O	143	100	TDO
35	NC	I/O	72	50	TMS	108	75	I/O	144	1	I/O
36	24	I/O	73	51	I/O	109	76	TCK			
37	25	I/O	74	52	I/O	110	77	STM			

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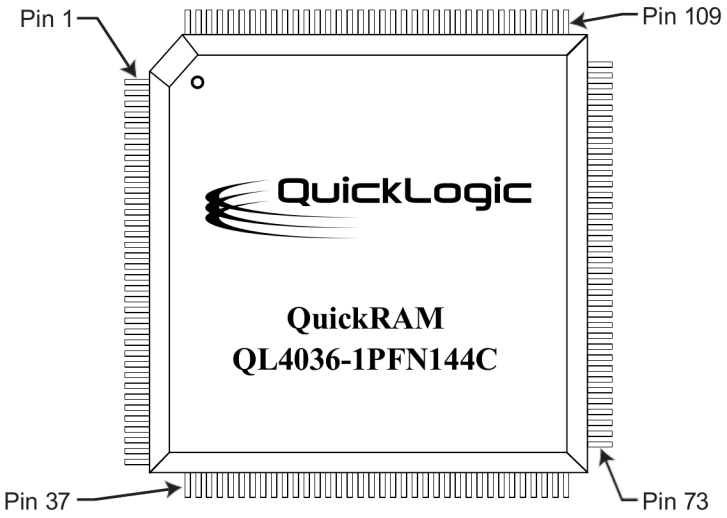
QL4036 – 144 TQFP Pinout Diagram

Figure 16: QL4036 – 144 Pin TQFP (Top View)



QL4036 – 208 PQFP Pinout Diagram

Figure 17: QL4036 – 208* Pin PQFP (Top View)

Note * 208-pin QFP package is in long-term obsolescence and not recommended for new designs.



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QL4036 – 144 TQFP and 208* PQFP Pinout Table

Table 20: QL4036 – 144 TQFP and 208* PQFP Pinout Table

208 PQFP	144 TQFP	Function	208* PQFP	144 TQFP	Function	208* PQFP	144 TQFP	Function	208* PQFP	144 TQFP	Function	208* PQFP	144 TQFP	Function
1	NC	I/O	43	30	GND	85	60	I/O	127	87	GND	169	117	I/O
2	1	I/O	44	31	I/O	86	61	I/O	128	88	I/O	170	118	I/O
3	2	I/O	45	NC	I/O	87	NC	I/O	129	89	GCLK/I	171	119	I/O
4	3	I/O	46	32	I/O	88	62	I/O	130	90	ACLK/I	172	120	I/O
5	NC	I/O	47	NC	I/O	89	63	I/O	131	91	VCC	173	NC	I/O
6	4	I/O	48	33	I/O	90	NC	I/O	132	92	GCLK/I	174	NC	I/O
7	5	I/O	49	NC	I/O	91	NC	I/O	133	93	GCLK/I	175	121	I/O
8	NC	I/O	50	34	I/O	92	64	I/O	134	94	VCC	176	NC	I/O
9	6	I/O	51	35	I/O	93	NC	I/O	135	95	I/O	177	122	GND
10	7	VCC	52	36	I/O	94	65	I/O	136	NC	I/O	178	123	I/O
11	NC	I/O	53	37	I/O	95	66	GND	137	96	I/O	179	124	I/O
12	NC	GND	54	38	TDI	96	67	I/O	138	NC	I/O	180	NC	I/O
13	8	I/O	55	39	I/O	97	NC	VCC	139	97	I/O	181	125	I/O
14	NC	I/O	56	NC	I/O	98	NC	I/O	140	98	I/O	182	126	GND
15	9	I/O	57	40	I/O	99	68	I/O	141	NC	I/O	183	127	I/O
16	NC	I/O	58	NC	I/O	100	69	I/O	142	99	I/O	184	128	I/O
17	10	I/O	59	NC	GND	101	NC	I/O	143	NC	I/O	185	129	I/O
18	11	I/O	60	41	I/O	102	70	I/O	144	100	I/O	186	NC	I/O
19	12	I/O	61	42	VCC	103	71	TRSTB	145	NC	VCC	187	130	VCCIO
20	13	I/O	62	43	I/O	104	72	TMS	146	101	I/O	188	131	I/O
21	NC	I/O	63	NC	I/O	105	NC	I/O	147	102	GND	189	132	I/O
22	14	I/O	64	44	I/O	106	73	I/O	148	103	I/O	190	NC	I/O
23	15	GND	65	45	I/O	107	NC	I/O	149	104	I/O	191	133	I/O
24	16	I/O	66	NC	I/O	108	74	I/O	150	NC	I/O	192	134	I/O
25	17	GCLK/I	67	46	I/O	109	75	I/O	151	105	I/O	193	NC	I/O
26	18	ACLK/I	68	47	I/O	110	76	I/O	152	106	I/O	194	135	I/O
27	19	VCC	69	48	I/O	111	77	I/O	153	NC	I/O	195	136	I/O
28	20	GCLK/I	70	NC	I/O	112	NC	I/O	154	107	I/O	196	NC	I/O
29	21	GCLK/I	71	49	I/O	113	78	I/O	155	NC	I/O	197	137	I/O
30	22	VCC	72	NC	I/O	114	79	VCC	156	108	I/O	198	NC	I/O
31	23	I/O	73	50	GND	115	80	I/O	157	109	TCK	199	138	GND
32	NC	I/O	74	51	I/O	116	NC	GND	158	110	STM	200	139	I/O
33	24	I/O	75	52	I/O	117	81	I/O	159	111	I/O	201	NC	VCC
34	NC	I/O	76	NC	I/O	118	82	I/O	160	NC	I/O	202	140	I/O
35	25	I/O	77	53	I/O	119	NC	I/O	161	112	I/O	203	NC	I/O
36	NC	I/O	78	54	GND	120	83	I/O	162	113	I/O	204	141	I/O
37	26	I/O	79	55	I/O	121	NC	I/O	163	NC	GND	205	142	I/O
38	27	I/O	80	56	I/O	122	84	I/O	164	NC	I/O	206	NC	I/O
39	28	I/O	81	NC	I/O	123	85	I/O	165	114	VCC	207	143	TDO
40	NC	I/O	82	57	I/O	124	NC	I/O	166	115	I/O	208	144	I/O
41	NC	VCC	83	58	VCCIO	125	86	I/O	167	116	I/O			
42	29	I/O	84	59	I/O	126	NC	I/O	168	NC	I/O			

Note * 208-pin QFP package is in long-term obsolescence and not recommended for new designs.

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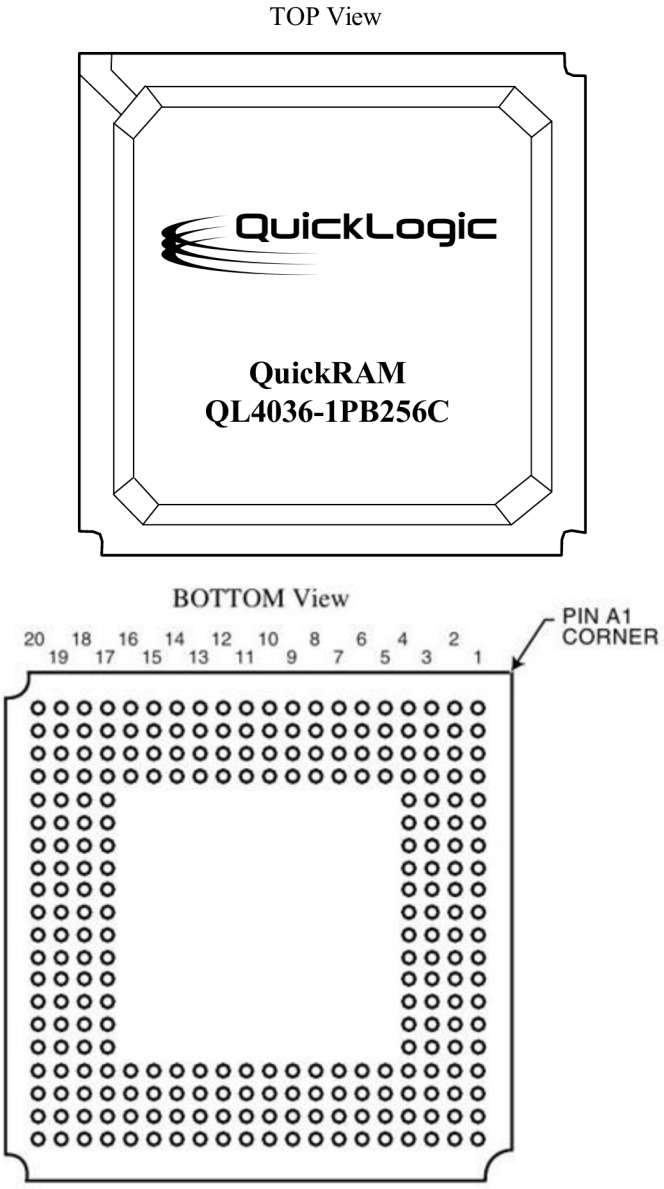
QL4036 – 256 PBGA Pinout Diagram

Figure 18: QL4036 – 256 PBGA Pinout Diagram



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QL4036 – 256 PBGA Pinout Table

Table 21: QL4036 – 256 PBGA Pinout Table

256 PBGA	Function	256 PBGA	Function	256 PBGA	Function	256 PBGA	Function	256 PBGA	Function	256 PBGA	Function
A1	VSS	C4	I/O	E19	I/O	L2	ACLK/I	T17	I/O	V20	I/O
A2	I/O	C5	I/O	E20	I/O	L3	GCLK/I	T18	I/O	W1	I/O
A3	I/O	C6	I/O	F1	I/O	L4	GCLK/I	T19	NC	W2	I/O
A4	I/O	C7	I/O	F2	I/O	L17	VCC	T20	I/O	W3	TDI
A5	I/O	C8	I/O	F3	I/O	L18	I/O	U1	I/O	W4	I/O
A6	I/O	C9	VCCIO	F4	VCC	L19	I/O	U2	I/O	W5	I/O
A7	I/O	C10	I/O	F17	VCC	L20	I/O	U3	I/O	W6	I/O
A8	I/O	C11	I/O	F18	NC	M1	I/O	U4	VSS	W7	I/O
A9	I/O	C12	I/O	F19	I/O	M2	I/O	U5	I/O	W8	I/O
A10	I/O	C13	I/O	F20	I/O	M3	I/O	U6	VCC	W9	I/O
A11	I/O	C14	I/O	G1	I/O	M4	NC	U7	I/O	W10	I/O
A12	I/O	C15	I/O	G2	NC	M17	NC	U8	VSS	W11	I/O
A13	I/O	C16	I/O	G3	I/O	M18	I/O	U9	I/O	W12	I/O
A14	I/O	C17	I/O	G4	I/O	M19	I/O	U10	VCC	W13	I/O
A15	I/O	C18	I/O	G17	I/O	M20	I/O	U11	I/O	W14	I/O
A16	I/O	C19	I/O	G18	I/O	N1	I/O	U12	I/O	W15	I/O
A17	I/O	C20	I/O	G19	NC	N2	I/O	U13	VSS	W16	I/O
A18	I/O	D1	I/O	G20	I/O	N3	I/O	U14	I/O	W17	I/O
A19	TCK	D2	I/O	H1	I/O	N4	VSS	U15	VCC	W18	I/O
A20	I/O	D3	I/O	H2	I/O	N17	VSS	U16	I/O	W19	I/O
B1	TDO	D4	VSS	H3	I/O	N18	I/O	U17	VSS	W20	TRSTB
B2	I/O	D5	I/O	H4	VSS	N19	I/O	U18	I/O	Y1	I/O
B3	I/O	D6	VCC	H17	VSS	N20	I/O	U19	I/O	Y2	NC
B4	I/O	D7	I/O	H18	I/O	P1	I/O	U20	I/O	Y3	I/O
B5	I/O	D8	VSS	H19	I/O	P2	I/O	V1	I/O	Y4	I/O
B6	I/O	D9	I/O	H20	I/O	P3	I/O	V2	NC	Y5	I/O
B7	I/O	D10	I/O	J1	I/O	P4	I/O	V3	I/O	Y6	I/O
B8	I/O	D11	VCC	J2	I/O	P17	I/O	V4	I/O	Y7	I/O
B9	I/O	D12	I/O	J3	NC	P18	I/O	V5	I/O	Y8	I/O
B10	I/O	D13	VSS	J4	I/O	P19	NC	V6	I/O	Y9	I/O
B11	I/O	D14	I/O	J17	NC	P20	I/O	V7	I/O	Y10	I/O
B12	I/O	D15	VCC	J18	I/O	R1	NC	V8	I/O	Y11	I/O
B13	I/O	D16	I/O	J19	I/O	R2	I/O	V9	I/O	Y12	I/O
B14	I/O	D17	VSS	J20	GCLK/I	R3	I/O	V10	I/O	Y13	I/O
B15	I/O	D18	I/O	K1	I/O	R4	VCC	V11	I/O	Y14	I/O
B16	I/O	D19	I/O	K2	I/O	R17	VCC	V12	VCCIO	Y15	I/O
B17	NC	D20	I/O	K3	I/O	R18	I/O	V13	I/O	Y16	I/O
B18	STM	E1	NC	K4	VCC	R19	I/O	V14	I/O	Y17	I/O
B19	NC	E2	I/O	K17	GCLK/I	R20	I/O	V15	I/O	Y18	I/O
B20	I/O	E3	I/O	K18	ACLK/I	T1	NC	V16	I/O	Y19	I/O
C1	I/O	E4	I/O	K19	GCLK/I	T2	I/O	V17	I/O	Y20	NC
C2	I/O	E17	I/O	K20	NC	T3	I/O	V18	I/O		
C3	I/O	E18	I/O	L1	GCLK/I	T4	NC	V19	TMS		

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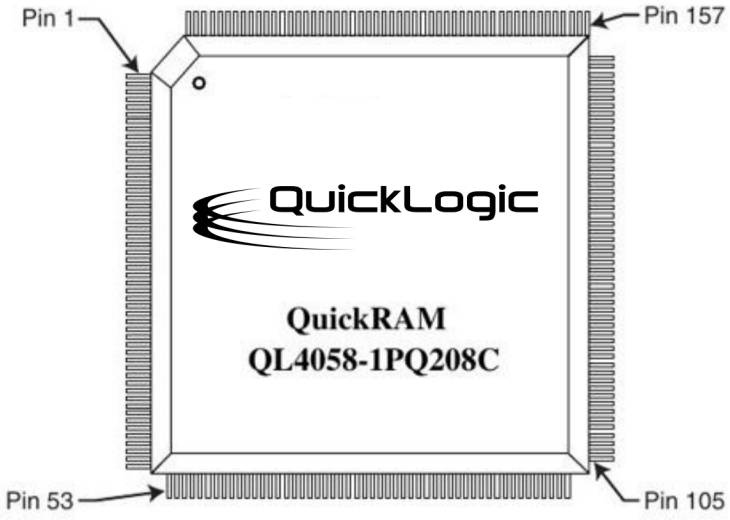
QL4058 – 208* PQFP Pinout Diagrams

Figure 19: QL4058 – 208 Pin PQFP (Top View)

Note * 208-pin QFP package is in long-term obsolescence and not recommended for new designs.



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QL4058 – 208* PQFP Pinout Table

Table 22: QL4058 – 208* PQFP Pinout Table

208* PQFP	Function	208* PQFP	Function	208* PQFP	Function	208* PQFP	Function	208* PQFP	Function
208	I/O	43	GND	84	I/O	125	I/O	168	I/O
1	I/O	44	I/O	85	I/O	126	I/O	169	I/O
2	I/O	45	I/O	86	I/O	127	GND	NC	I/O
3	I/O	46	I/O	87	I/O	128	I/O	170	I/O
4	I/O	47	I/O	88	I/O	NC	I/O	171	I/O
5	I/O	48	I/O	89	I/O	129	GLCK/I	172	I/O
NC	I/O	NC	I/O	90	I/O	130	ACLK/I	173	I/O
6	I/O	49	I/O	91	I/O	131	VCC	174	I/O
7	I/O	50	I/O	92	I/O	132	GLCK/I	175	I/O
8	I/O	51	I/O	NC	I/O	133	GLCK/I	NC	I/O
9	I/O	52	I/O	93	I/O	134	VCC	176	I/O
10	VCC	53	I/O	94	I/O	135	I/O	177	GND
11	I/O	54	TDI	95	GND	136	I/O	178	I/O
12	GND	NC	I/O	96	I/O	NC	I/O	179	I/O
13	I/O	NC	I/O	97	VCC	137	I/O	NC	I/O
14	I/O	55	I/O	98	I/O	NC	GND	180	I/O
NC	I/O	56	I/O	99	I/O	138	I/O	181	I/O
15	I/O	NC	I/O	100	I/O	139	I/O	182	GND
16	I/O	57	I/O	NC	I/O	140	I/O	NC	VCC
17	I/O	58	I/O	101	I/O	141	I/O	183	I/O
18	I/O	59	GND	NC	I/O	142	I/O	184	I/O
19	I/O	60	I/O	102	I/O	NC	I/O	185	I/O
20	I/O	61	VCC	NC	I/O	143	I/O	186	I/O
NC	I/O	62	I/O	NC	I/O	144	I/O	187	VCCIO
21	I/O	63	I/O	103	TRSTB	145	VCC	188	I/O
22	I/O	64	I/O	104	TMS	NC	I/O	NC	I/O
23	GND	NC	I/O	105	I/O	146	I/O	189	I/O
24	I/O	65	I/O	NC	I/O	147	GND	190	I/O
25	GCLK/I	66	I/O	106	I/O	148	I/O	191	I/O
26	ACLK/I	67	I/O	107	I/O	149	I/O	192	I/O
27	VCC	NC	I/O	108	I/O	150	I/O	193	I/O
28	GCLK/I	68	I/O	109	I/O	151	I/O	194	I/O
29	GCLK/I	69	I/O	NC	I/O	152	I/O	NC	I/O
30	VCC	70	I/O	110	I/O	153	I/O	195	I/O
31	I/O	NC	I/O	111	I/O	154	I/O	196	I/O
32	I/O	71	I/O	112	I/O	155	I/O	197	I/O
NC	GND	NC	I/O	113	I/O	156	I/O	198	I/O
33	I/O	72	I/O	114	VCC	157	TCK	NC	I/O
NC	I/O	73	GND	115	I/O	158	STM	199	GND
34	I/O	74	I/O	116	GND	NC	I/O	200	I/O
35	I/O	NC	VCC	117	I/O	159	I/O	201	VCC
36	I/O	75	I/O	NC	I/O	160	I/O	202	I/O
NC	I/O	76	I/O	118	I/O	161	I/O	203	I/O
37	I/O	77	I/O	119	I/O	162	I/O	204	I/O
38	I/O	78	GND	120	I/O	163	GND	205	I/O
39	I/O	79	I/O	121	I/O	164	I/O	206	I/O
NC	I/O	80	I/O	NC	I/O	165	VCC	207	TDO
40	I/O	81	I/O	122	I/O	166	I/O		
41	VCC	82	I/O	123	I/O	NC	I/O		
42	I/O	83	VCCIO	124	I/O	167	I/O		

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Note * 208-pin QFP package is in long-term obsolescence and not recommended for new designs.

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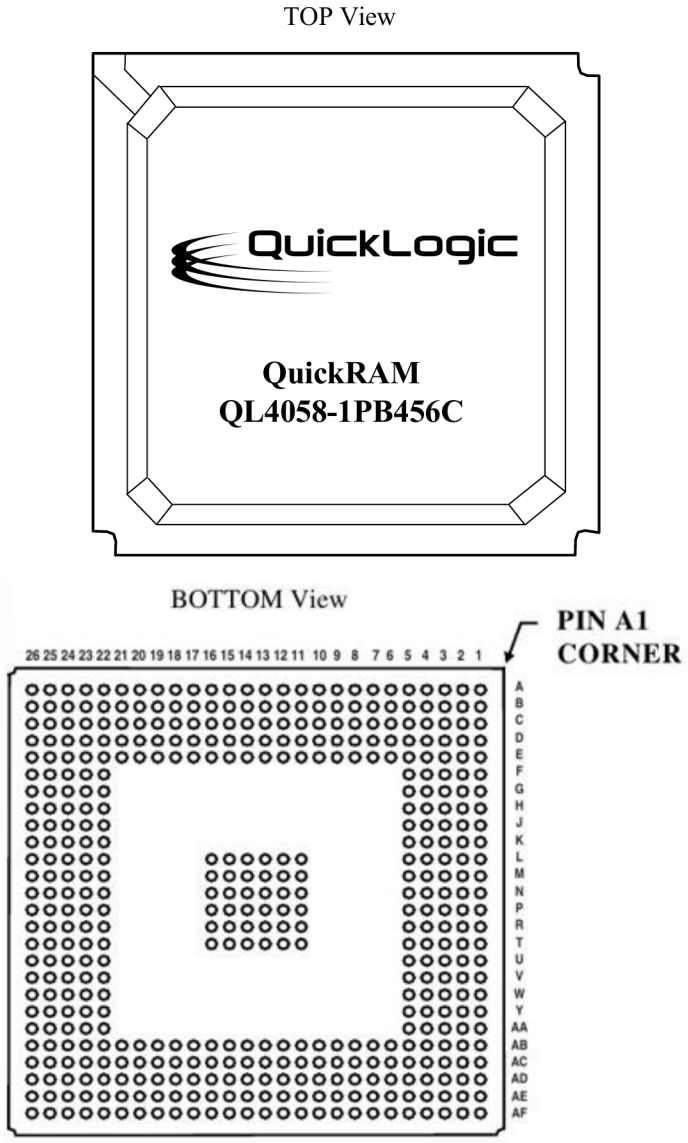
QL4058 – 456 PBGA Pinout Diagram

Figure 21: QL4058 – 456 PBGA Pinout Diagram



QL4058 – 456 PBGA Pinout Table

Table 23: QL4058 – 456 PBGA Pinout Table

456	Function	456	Function	456	Function	456	Function	456	Function
A1	I/O	C1	I/O	E1	I/O	H23	NC	M23	NC
A2	I/O	C2	I/O	E2	I/O	H24	I/O	M24	I/O
A3	I/O	C3	I/O	E3	I/O	H25	NC	M25	I/O
A4	I/O	C4	TDO	E4	I/O	H26	I/O	M26	I/O
A5	I/O	C5	I/O	E5	GND	J1	I/O	N1	GCLK/I
A6	I/O	C6	I/O	E6	VCC	J2	I/O	N2	I/O
A7	I/O	C7	I/O	E7	GND	J3	I/O	N3	I/O
A8	I/O	C8	I/O	E8	NC	J4	NC	N4	GCLK/I
A9	NC	C9	I/O	E9	GND	J5	GND	N5	VCC
A10	I/O	C10	I/O	E10	I/O	J22	NC	N11	GND/THERM
A11	I/O	C11	I/O	E11	GND	J23	NC	N12	GND/THERM
A12	VCCIO	C12	I/O	E12	GND	J24	I/O	N13	GND/THERM
A13	I/O	C13	I/O	E13	VCC	J25	I/O	N14	GND/THERM
A14	I/O	C14	I/O	E14	GND	J26	I/O	N15	GND/THERM
A15	NC	C15	I/O	E15	GND	K1	NC	N16	GND/THERM
A16	I/O	C16	I/O	E16	GND	K2	NC	N22	GND
A17	NC	C17	NC	E17	NC	K3	I/O	N23	I/O
A18	I/O	C18	NC	E18	GND	K4	I/O	N24	I/O
A19	I/O	C19	I/O	E19	NC	K5	VCC	N25	NC
A20	I/O	C20	I/O	E20	GND	K22	GND	N26	I/O
A21	NC	C21	I/O	E21	VCC	K23	I/O	P1	I/O
A22	I/O	C22	I/O	E22	GND	K24	I/O	P2	I/O
A23	NC	C23	I/O	E23	I/O	K25	NC	P3	NC
A24	I/O	C24	I/O	E24	I/O	K26	I/O	P4	I/O
A25	I/O	C25	TCK	E25	I/O	L1	I/O	P5	NC
A26	I/O	C26	NC	E26	I/O	L2	I/O	P11	GND/THERM
B1	I/O	D1	I/O	F1	I/O	L3	I/O	P12	GND/THERM
B2	NC	D2	I/O	F2	I/O	L4	I/O	P13	GND/THERM
B3	I/O	D3	I/O	F3	NC	L5	NC	P14	GND/THERM
B4	NC	D4	GND	F4	NC	L11	GND/THERM	P15	GND/THERM
B5	NC	D5	NC	F5	VCC	L12	GND/THERM	P16	GND/THERM
B6	NC	D6	NC	F22	VCC	L13	GND/THERM	P22	NC
B7	NC	D7	I/O	F23	NC	L14	GND/THERM	P23	GCLK/I
B8	NC	D8	I/O	F24	I/O	L15	GND/THERM	P24	GCLK/I
B9	I/O	D9	GND	F25	I/O	L16	GND/THERM	P25	NC
B10	NC	D10	I/O	F26	I/O	L22	NC	P26	ACLK/I
B11	NC	D11	I/O	G1	I/O	L23	I/O	R1	NC
B12	I/O	D12	GND	G2	I/O	L24	I/O	R2	I/O
B13	I/O	D13	I/O	G3	I/O	L25	NC	R3	I/O
B14	NC	D14	I/O	G4	I/O	L26	I/O	R4	NC
B15	I/O	D15	GND	G5	NC	M1	ACLK/I	R5	NC
B16	I/O	D16	I/O	G22	GND	M2	GCLK/I	R11	GND/THERM
B17	I/O	D17	I/O	G23	NC	M3	I/O	R12	GND/THERM
B18	I/O	D18	GND	G24	I/O	M4	NC	R13	GND/THERM
B19	I/O	D19	I/O	G25	I/O	M5	GND	R14	GND/THERM
B20	I/O	D20	NC	G26	I/O	M11	GND/THERM	R15	GND/THERM
B21	I/O	D21	NC	H1	NC	M12	GND/THERM	R16	GND/THERM
B22	I/O	D22	I/O	H2	I/O	M13	GND/THERM	R22	VCC
B23	NC	D23	GND	H3	NC	M14	GND/THERM	R23	NC
B24	I/O	D24	I/O	H4	I/O	M15	GND/THERM	R24	NC

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456	Function	456	Function	456	Function	456	Function	456	Function
B25	I/O	**D25**	I/O	**H5**	NC	**M16**	GND/THERM	**R25**	I/O
B26	STM	**D26**	I/O	**H22**	NC	**M22**	NC	**R26**	GCLK/I

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Table 23: QL4058 – 456 PBGA Pinout Table *(Continued)*

456	Function	456	Function	456	Function	456	Function	456	Function
T1	I/O	W5	NC	AB15	VCC	AD3	I/O	AE17	I/O
T2	I/O	W22	NC	AB16	I/O	AD4	I/O	AE18	I/O
T3	I/O	W23	I/O	AB17	NC	AD5	I/O	AE19	I/O
T4	I/O	W24	I/O	AB18	VCC	AD6	I/O	AE20	I/O
T5	VCC	W25	I/O	AB19	GND	AD7	I/O	AE21	I/O
T11	GND/THERM	W26	NC	AB20	NC	AD8	I/O	AE22	NC
T12	GND/THERM	Y1	NC	AB21	VCC	AD9	NC	AE23	NC
T13	GND/THERM	Y2	I/O	AB22	GND	AD10	I/O	AE24	TMS
T14	GND/THERM	Y3	NC	AB23	I/O	AD11	NC	AE25	I/O
T15	GND/THERM	Y4	I/O	AB24	NC	AD12	I/O	AE26	I/O
T16	GND/THERM	Y5	I/O	AB25	I/O	AD13	I/O	AF1	I/O
T22	GND	Y22	GND	AB26	I/O	AD14	I/O	AF2	NC
T23	I/O	Y23	I/O	AC1	I/O	AD15	I/O	AF3	I/O
T24	I/O	Y24	NC	AC2	I/O	AD16	I/O	AF4	NC
T25	NC	Y25	I/O	AC3	NC	AD17	I/O	AF5	I/O
T26	I/O	Y26	I/O	AC4	GND	AD18	I/O	AF6	I/O
U1	NC	AA1	I/O	AC5	NC	AD19	NC	AF7	I/O
U2	I/O	AA2	I/O	AC6	NC	AD20	NC	AF8	I/O
U3	I/O	AA3	NC	AC7	NC	AD21	I/O	AF9	I/O
U4	I/O	AA4	NC	AC8	NC	AD22	I/O	AF10	I/O
U5	GND	AA5	VCC	AC9	NC	AD23	TRSTB	AF11	NC
U22	NC	AA22	VCC	AC10	NC	AD24	NC	AF12	I/O
U23	I/O	AA23	NC	AC11	I/O	AD25	I/O	AF13	I/O
U24	I/O	AA24	I/O	AC12	NC	AD26	I/O	AF14	NC
U25	I/O	AA25	I/O	AC13	I/O	AE1	TDI	AF15	NC
U26	I/O	AA26	I/O	AC14	VCCIO	AE2	I/O	AF16	I/O
V1	I/O	AB1	NC	AC15	NC	AE3	I/O	AF17	I/O
V2	I/O	AB2	I/O	AC16	NC	AE4	I/O	AF18	I/O
V3	NC	AB3	I/O	AC17	NC	AE5	I/O	AF19	NC
V4	NC	AB4	I/O	AC18	NC	AE6	I/O	AF20	I/O
V5	NC	AB5	GND	AC19	I/O	AE7	I/O	AF21	I/O
V22	GND	AB6	VCC	AC20	I/O	AE8	I/O	AF22	I/O
V23	NC	AB7	NC	AC21	I/O	AE9	I/O	AF23	I/O
V24	I/O	AB8	NC	AC22	NC	AE10	I/O	AF24	I/O
V25	NC	AB9	NC	AC23	GND	AE11	I/O	AF25	I/O
V26	I/O	AB10	VCC	AC24	NC	AE12	I/O	AF26	I/O
W1	I/O	AB11	GND	AC25	I/O	AE13	I/O		
W2	I/O	AB12	NC	AC26	I/O	AE14	I/O		
W3	I/O	AB13	I/O	AD1	I/O	AE15	I/O		
W4	I/O	AB14	GND	AD2	NC	AE16	I/O		

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QL4090 – 208* PQFP Pinout Diagrams

Note * 208-pin QFP package is in long-term obsolescence and not recommended for new designs.



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QL4090 – 208* PQFP Pinout Table

Table 24: QL4090 – 208* PQFP Pinout Table

Note * 208-pin QFP package is in long-term obsolescence and not recommended for new designs.

208* PQFP	Function	208* PQFP	Function	208* PQFP	Function	208* PQFP	Function	208* PQFP	Function
208	I/O	43	GND	84	I/O	125	I/O	168	I/O
1	I/O	44	I/O	85	I/O	126	I/O	169	I/O
2	I/O	45	I/O	86	I/O	127	GND	NC	I/O
3	I/O	46	I/O	87	I/O	128	I/O	170	I/O
4	I/O	47	I/O	88	I/O	NC	I/O	171	I/O
5	I/O	48	I/O	89	I/O	129	GLCK/I	172	I/O
NC	I/O	NC	I/O	90	I/O	130	ACLK/I	173	I/O
6	I/O	49	I/O	91	I/O	131	VCC	174	I/O
7	I/O	50	I/O	92	I/O	132	GLCK/I	175	I/O
8	I/O	51	I/O	NC	I/O	133	GLCK/I	NC	I/O
9	I/O	52	I/O	93	I/O	134	VCC	176	I/O
10	VCC	53	I/O	94	I/O	135	I/O	177	GND
11	I/O	54	TDI	95	GND	136	I/O	178	I/O
12	GND	NC	I/O	96	I/O	NC	I/O	179	I/O
13	I/O	NC	I/O	97	VCC	137	I/O	NC	I/O
14	I/O	55	I/O	98	I/O	NC	GND	180	I/O
NC	I/O	56	I/O	99	I/O	138	I/O	181	I/O
15	I/O	NC	I/O	100	I/O	139	I/O	182	GND
16	I/O	57	I/O	NC	I/O	140	I/O	NC	VCC
17	I/O	58	I/O	101	I/O	141	I/O	183	I/O
18	I/O	59	GND	NC	I/O	142	I/O	184	I/O
19	I/O	60	I/O	102	I/O	NC	I/O	185	I/O
20	I/O	61	VCC	NC	I/O	143	I/O	186	I/O
NC	I/O	62	I/O	NC	I/O	144	I/O	187	VCCIO
21	I/O	63	I/O	103	TRSTB	145	VCC	188	I/O
22	I/O	64	I/O	104	TMS	NC	I/O	NC	I/O
23	GND	NC	I/O	105	I/O	146	I/O	189	I/O
24	I/O	65	I/O	NC	I/O	147	GND	190	I/O
25	GCLK/I	66	I/O	106	I/O	148	I/O	191	I/O
26	ACLK/I	67	I/O	107	I/O	149	I/O	192	I/O
27	VCC	NC	I/O	108	I/O	150	I/O	193	I/O
28	GCLK/I	68	I/O	109	I/O	151	I/O	194	I/O
29	GCLK/I	69	I/O	NC	I/O	152	I/O	NC	I/O
30	VCC	70	I/O	110	I/O	153	I/O	195	I/O
31	I/O	NC	I/O	111	I/O	154	I/O	196	I/O
32	I/O	71	I/O	112	I/O	155	I/O	197	I/O
NC	GND	NC	I/O	113	I/O	156	I/O	198	I/O
33	I/O	72	I/O	114	VCC	157	TCK	NC	I/O
NC	I/O	73	GND	115	I/O	158	STM	199	GND
34	I/O	74	I/O	116	GND	NC	I/O	200	I/O
35	I/O	NC	VCC	117	I/O	159	I/O	201	VCC
36	I/O	75	I/O	NC	I/O	160	I/O	202	I/O
NC	I/O	76	I/O	118	I/O	161	I/O	203	I/O
37	I/O	77	I/O	119	I/O	162	I/O	204	I/O
38	I/O	78	GND	120	I/O	163	GND	205	I/O
39	I/O	79	I/O	121	I/O	164	I/O	206	I/O
NC	I/O	80	I/O	NC	I/O	165	VCC	207	TDO
40	I/O	81	I/O	122	I/O	166	I/O		

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208* PQFP	Function	208* PQFP	Function	208* PQFP	Function	208* PQFP	Function	208* PQFP	Function
41	VCC	82	I/O	123	I/O	NC	I/O		
42	I/O	83	VCCIO	124	I/O	167	I/O		

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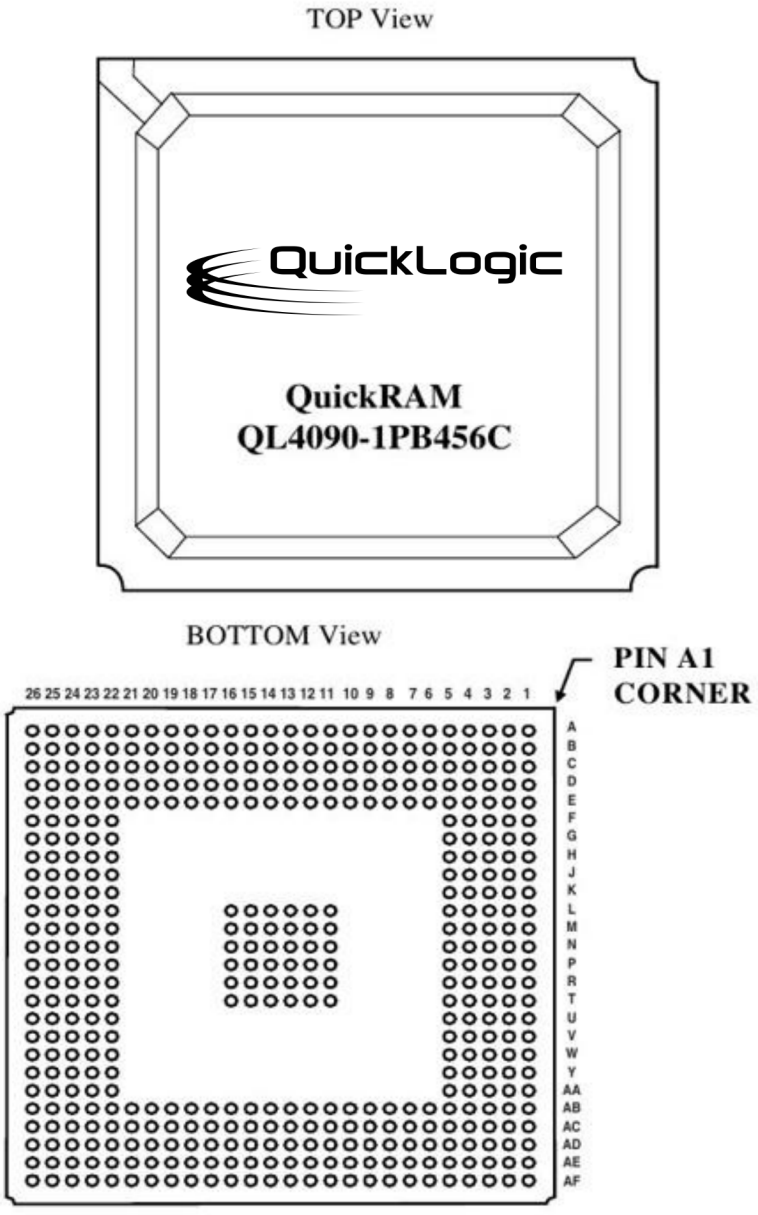
QL4090 – 456 PBGA Pinout Diagram

Figure 24: QL4090 – 456 PBGA Pinout Diagram



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QL4090 – 456 PBGA Pinout Table

Table 25: QL4090 – 456 PBGA Pinout Table

456	Function	456	Function	456	Function	456	Function	456	Function
A1	I/O	C1	I/O	E1	I/O	H23	I/O	M23	NC
A2	I/O	C2	I/O	E2	I/O	H24	I/O	M24	I/O
A3	I/O	C3	I/O	E3	I/O	H25	I/O	M25	I/O
A4	I/O	C4	TDO	E4	I/O	H26	I/O	M26	I/O
A5	I/O	C5	I/O	E5	GND	J1	I/O	N1	GCLK/I
A6	I/O	C6	I/O	E6	VCC	J2	I/O	N2	I/O
A7	I/O	C7	I/O	E7	GND	J3	I/O	N3	I/O
A8	I/O	C8	I/O	E8	NC	J4	NC	N4	GCLK/I
A9	I/O	C9	I/O	E9	GND	J5	GND	N5	VCC
A10	I/O	C10	I/O	E10	I/O	J22	NC	N11	GND/THERM
A11	I/O	C11	I/O	E11	GND	J23	NC	N12	GND/THERM
A12	VCCIO	C12	I/O	E12	GND	J24	I/O	N13	GND/THERM
A13	I/O	C13	I/O	E13	VCC	J25	I/O	N14	GND/THERM
A14	I/O	C14	I/O	E14	GND	J26	I/O	N15	GND/THERM
A15	I/O	C15	I/O	E15	GND	K1	I/O	N16	GND/THERM
A16	I/O	C16	I/O	E16	GND	K2	I/O	N22	GND
A17	I/O	C17	I/O	E17	NC	K3	I/O	N23	I/O
A18	I/O	C18	I/O	E18	GND	K4	I/O	N24	I/O
A19	I/O	C19	I/O	E19	NC	K5	VCC	N25	I/O
A20	I/O	C20	I/O	E20	GND	K22	GND	N26	I/O
A21	I/O	C21	I/O	E21	VCC	K23	I/O	P1	I/O
A22	I/O	C22	I/O	E22	GND	K24	I/O	P2	I/O
A23	I/O	C23	I/O	E23	I/O	K25	I/O	P3	I/O
A24	I/O	C24	I/O	E24	I/O	K26	I/O	P4	I/O
A25	I/O	C25	TCK	E25	I/O	L1	I/O	P5	NC
A26	I/O	C26	I/O	E26	I/O	L2	I/O	P11	GND/THERM
B1	I/O	D1	I/O	F1	I/O	L3	I/O	P12	GND/THERM
B2	I/O	D2	I/O	F2	I/O	L4	I/O	P13	GND/THERM
B3	I/O	D3	I/O	F3	I/O	L5	NC	P14	GND/THERM
B4	I/O	D4	GND	F4	NC	L11	GND/THERM	P15	GND/THERM
B5	I/O	D5	I/O	F5	VCC	L12	GND/THERM	P16	GND/THERM
B6	I/O	D6	NC	F22	VCC	L13	GND/THERM	P22	NC
B7	I/O	D7	I/O	F23	NC	L14	GND/THERM	P23	GCLK/I
B8	I/O	D8	I/O	F24	I/O	L15	GND/THERM	P24	GCLK/I
B9	I/O	D9	GND	F25	I/O	L16	GND/THERM	P25	I/O
B10	I/O	D10	I/O	F26	I/O	L22	NC	p26	ACLK/I
B11	I/O	D11	I/O	G1	I/O	L23	I/O	R1	I/O
B12	I/O	D12	GND	G2	I/O	L24	I/O	R2	I/O
B13	I/O	D13	I/O	G3	I/O	L25	I/O	R3	I/O
B14	I/O	D14	I/O	G4	I/O	L26	I/O	R4	NC
B15	I/O	D15	GND	G5	NC	M1	ACLK/I	R5	NC
B16	I/O	D16	I/O	G22	GND	M2	GCLK/I	R11	GND/THERM
B17	I/O	D17	I/O	G23	I/O	M3	I/O	R12	GND/THERM
B18	I/O	D18	GND	G24	I/O	M4	NC	R13	GND/THERM
B19	I/O	D19	I/O	G25	I/O	M5	GND	R14	GND/THERM
B20	I/O	D20	I/O	G26	I/O	M11	GND/THERM	R15	GND/THERM
B21	I/O	D21	NC	H1	I/O	M12	GND/THERM	R16	GND/THERM
B22	I/O	D22	I/O	H2	I/O	M13	GND/THERM	R22	VCC
B23	I/O	D23	GND	H3	I/O	M14	GND/THERM	R23	NC
B24	I/O	D24	I/O	H4	I/O	M15	GND/THERM	R24	I/O

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456	Function	456	Function	456	Function	456	Function	456	Function
B25	I/O	D25	I/O	H5	NC	M16	GND/THERM	R25	I/O
B26	STM	D26	I/O	H22	NC	M22	NC	R26	GCLK/I

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Table 25: QL4090 – 456 PBGA Pinout Table *(Continued)*

456	Function	456	Function	456	Function	456	Function	456	Function
T1	I/O	W5	NC	AB15	VCC	AD3	I/O	AE17	I/O
T2	I/O	W22	NC	AB16	I/O	AD4	I/O	AE18	I/O
T3	I/O	W23	I/O	AB17	NC	AD5	I/O	AE19	I/O
T4	I/O	W24	I/O	AB18	VCC	AD6	I/O	AE20	I/O
T5	VCC	W25	I/O	AB19	GND	AD7	I/O	AE21	I/O
T11	GND/THERMAL	W26	I/O	AB20	NC	AD8	I/O	AE22	I/O
T12	GND/THERMAL	Y1	I/O	AB21	VCC	AD9	I/O	AE23	NC
T13	GND/THERMAL	Y2	I/O	AB22	GND	AD10	I/O	AE24	TMS
T14	GND/THERMAL	Y3	I/O	AB23	I/O	AD11	I/O	AE25	I/O
T15	GND/THERMAL	Y4	I/O	AB24	I/O	AD12	I/O	AE26	I/O
T16	GND/THERMAL	Y5	I/O	AB25	I/O	AD13	I/O	AF1	I/O
T22	GND	Y22	GND	AB26	I/O	AD14	I/O	AF2	I/O
T23	I/O	Y23	I/O	AC1	I/O	AD15	I/O	AF3	I/O
T24	I/O	Y24	I/O	AC2	I/O	AD16	I/O	AF4	I/O
T25	I/O	Y25	I/O	AC3	NC	AD17	I/O	AF5	I/O
T26	I/O	Y26	I/O	AC4	GND	AD18	I/O	AF6	I/O
U1	I/O	AA1	I/O	AC5	I/O	AD19	I/O	AF7	I/O
U2	I/O	AA2	I/O	AC6	NC	AD20	I/O	AF8	I/O
U3	I/O	AA3	NC	AC7	I/O	AD21	I/O	AF9	I/O
U4	I/O	AA4	NC	AC8	I/O	AD22	I/O	AF10	I/O
U5	GND	AA5	VCC	AC9	NC	AD23	TRSTB	AF11	I/O
U22	NC	AA22	VCC	AC10	I/O	AD24	I/O	AF12	I/O
U23	I/O	AA23	NC	AC11	I/O	AD25	I/O	AF13	I/O
U24	I/O	AA24	I/O	AC12	NC	AD26	I/O	AF14	I/O
U25	I/O	AA25	I/O	AC13	I/O	AE1	TDI	AF15	I/O
U26	I/O	AA26	I/O	AC14	VCCIO	AE2	I/O	AF16	I/O
V1	I/O	AB1	I/O	AC15	NC	AE3	I/O	AF17	I/O
V2	I/O	AB2	I/O	AC16	I/O	AE4	I/O	AF18	I/O
V3	I/O	AB3	I/O	AC17	I/O	AE5	I/O	AF19	I/O
V4	NC	AB4	I/O	AC18	NC	AE6	I/O	AF20	I/O
V5	NC	AB5	GND	AC19	I/O	AE7	I/O	AF21	I/O
V22	GND	AB6	VCC	AC20	I/O	AE8	I/O	AF22	I/O
V23	NC	AB7	NC	AC21	I/O	AE9	I/O	AF23	I/O
V24	I/O	AB8	NC	AC22	NC	AE10	I/O	AF24	I/O
V25	I/O	AB9	NC	AC23	GND	AE11	I/O	AF25	I/O
V26	I/O	AB10	VCC	AC24	I/O	AE12	I/O	AF26	I/O
W1	I/O	AB11	GND	AC25	I/O	AE13	I/O		
W2	I/O	AB12	NC	AC26	I/O	AE14	I/O		
W3	I/O	AB13	I/O	AD1	I/O	AE15	I/O		
W4	I/O	AB14	GND	AD2	NC	AE16	I/O		

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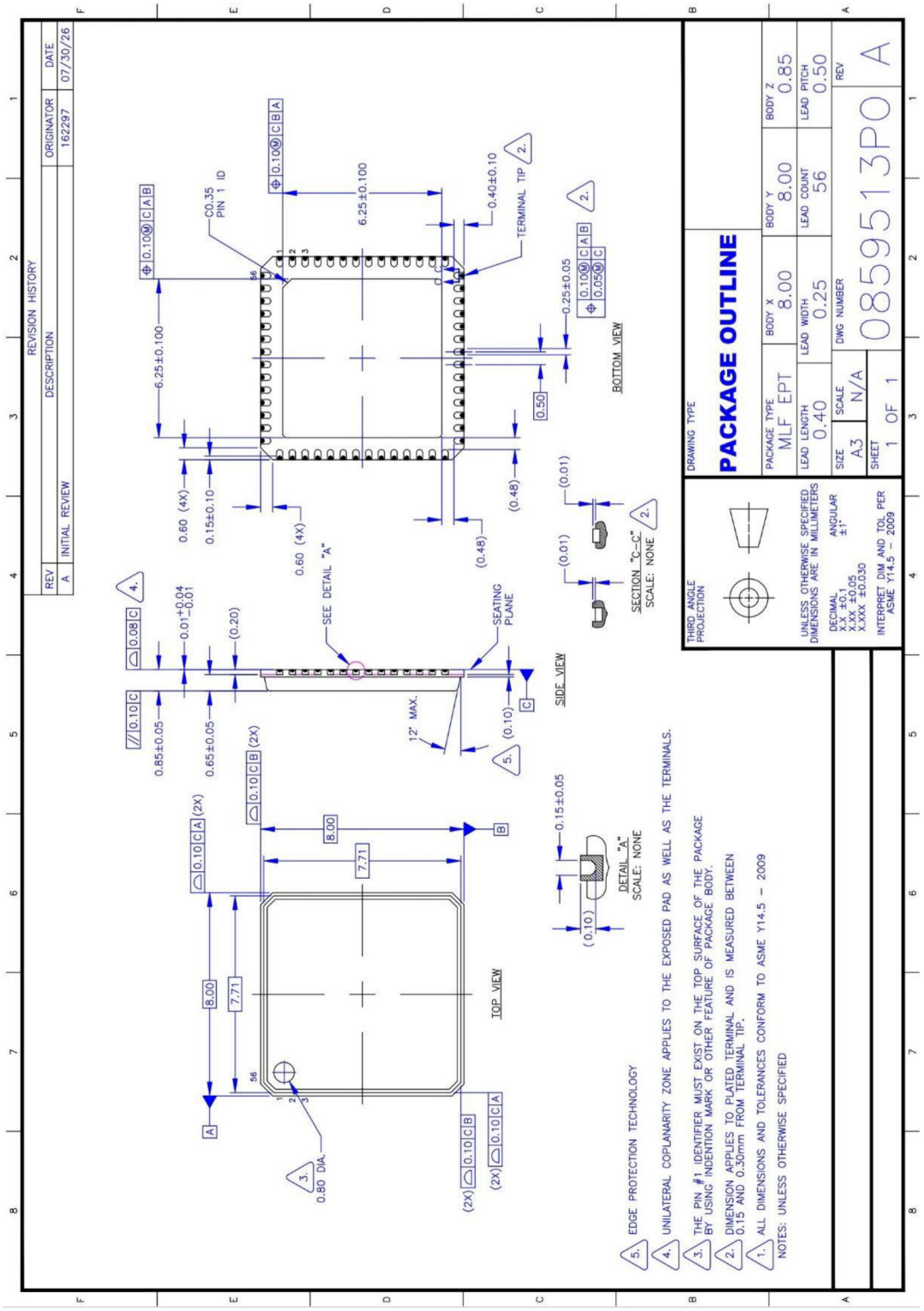
Package Mechanical Drawings

56-Pin QFN Mechanical Drawing



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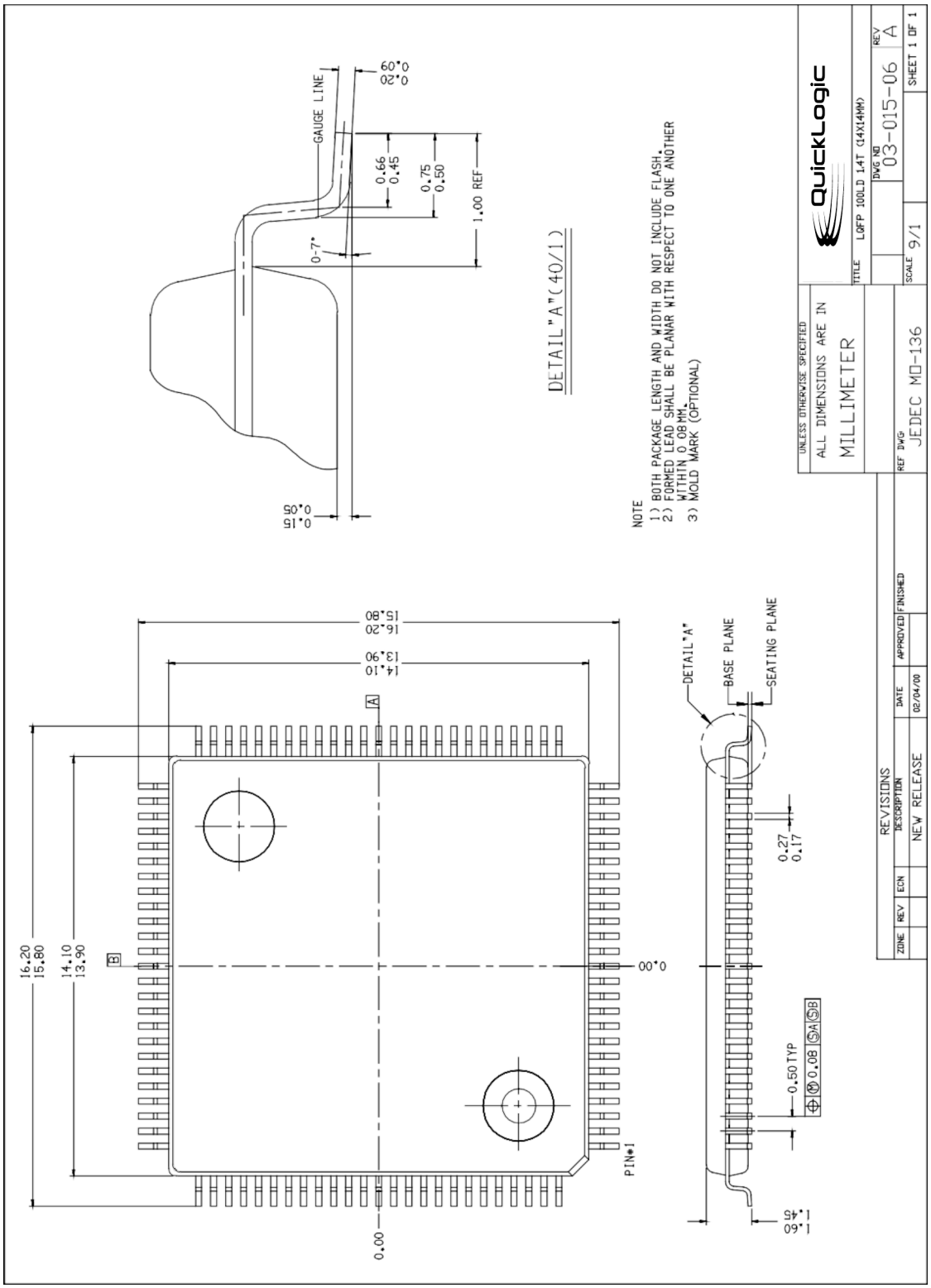
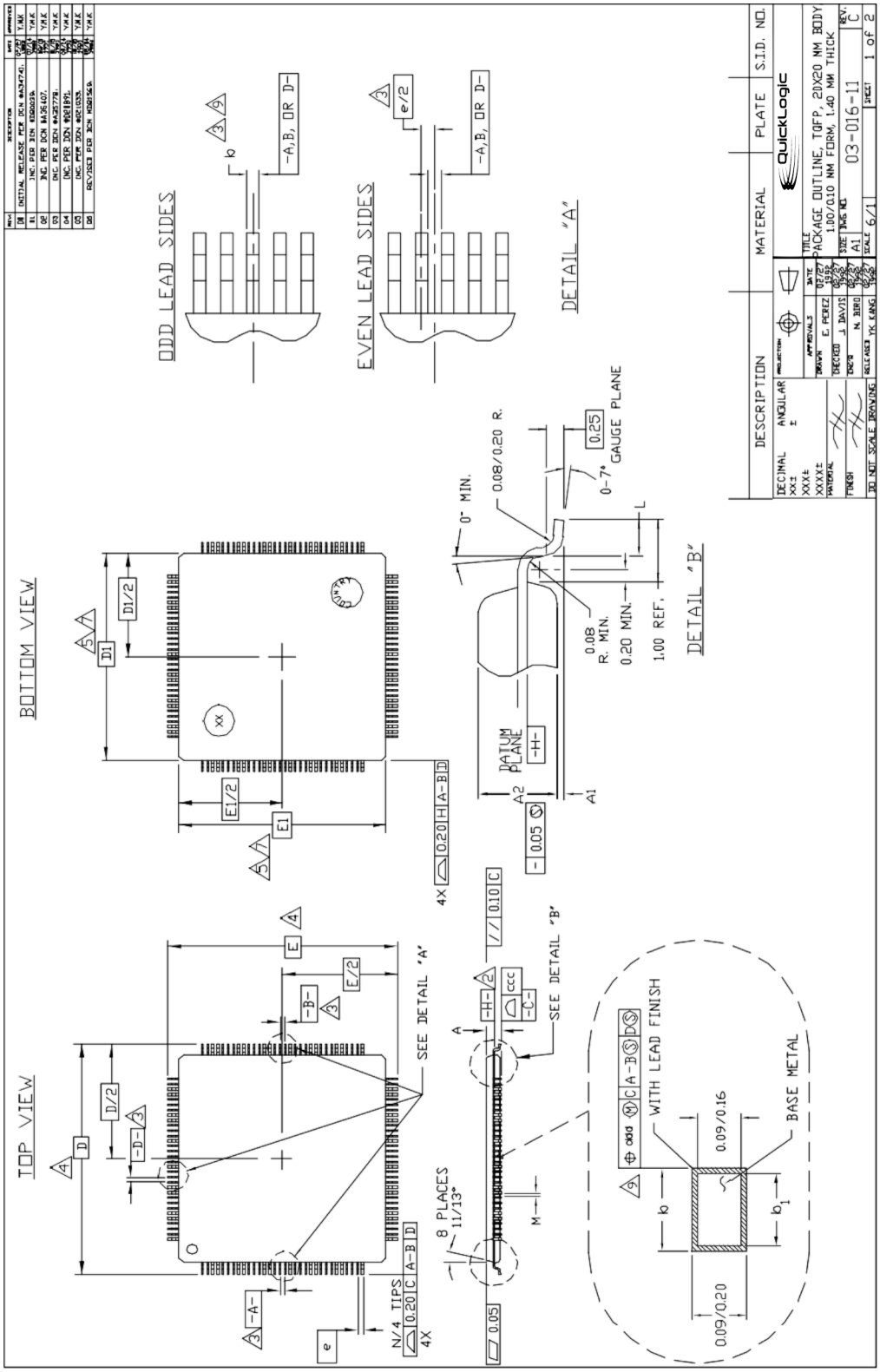
100 TQFP Mechanical Drawing



144 TQFP Packaging Drawing



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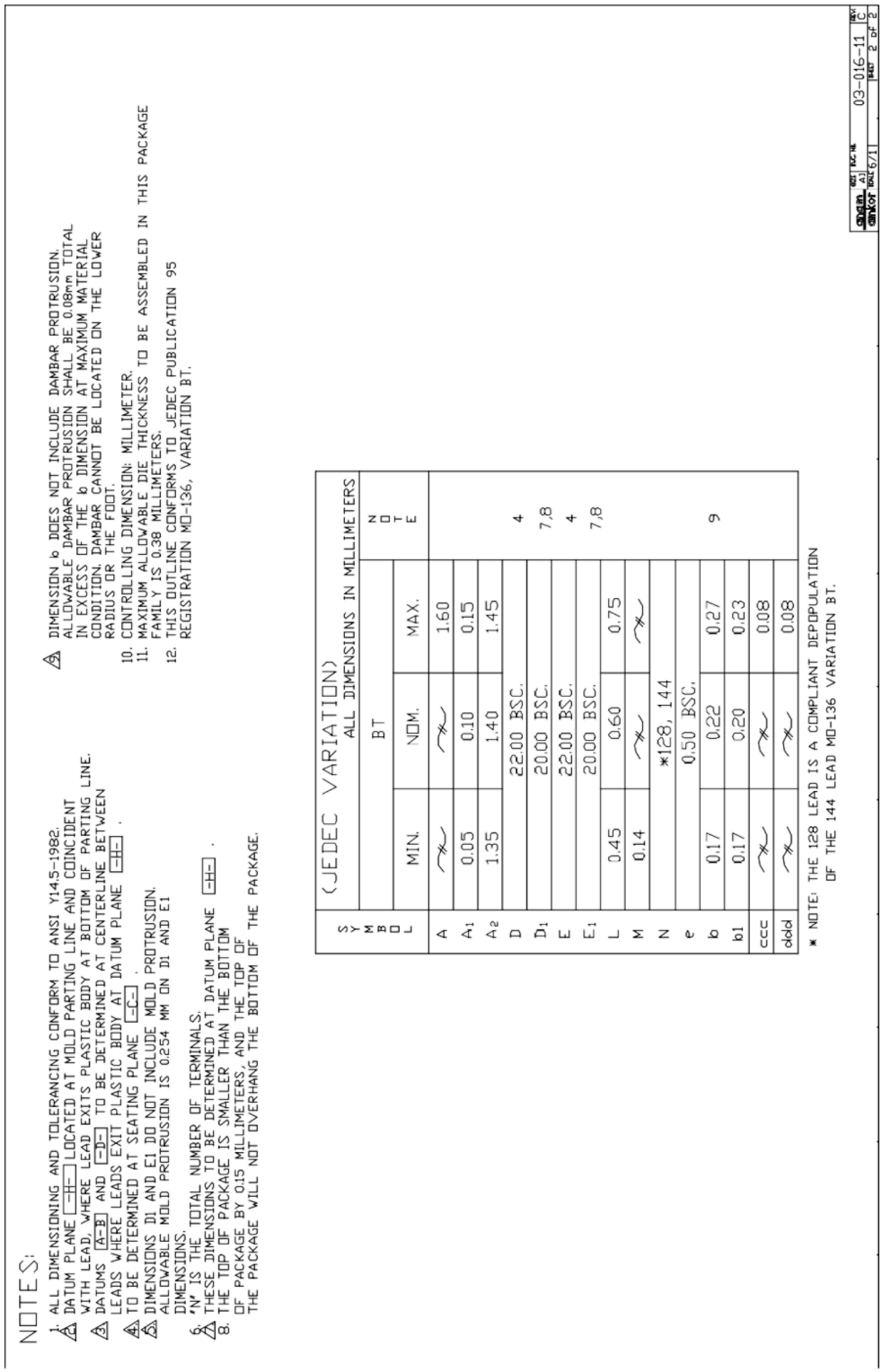
144 TQFP Packaging Drawing (Continued)



NOTES:

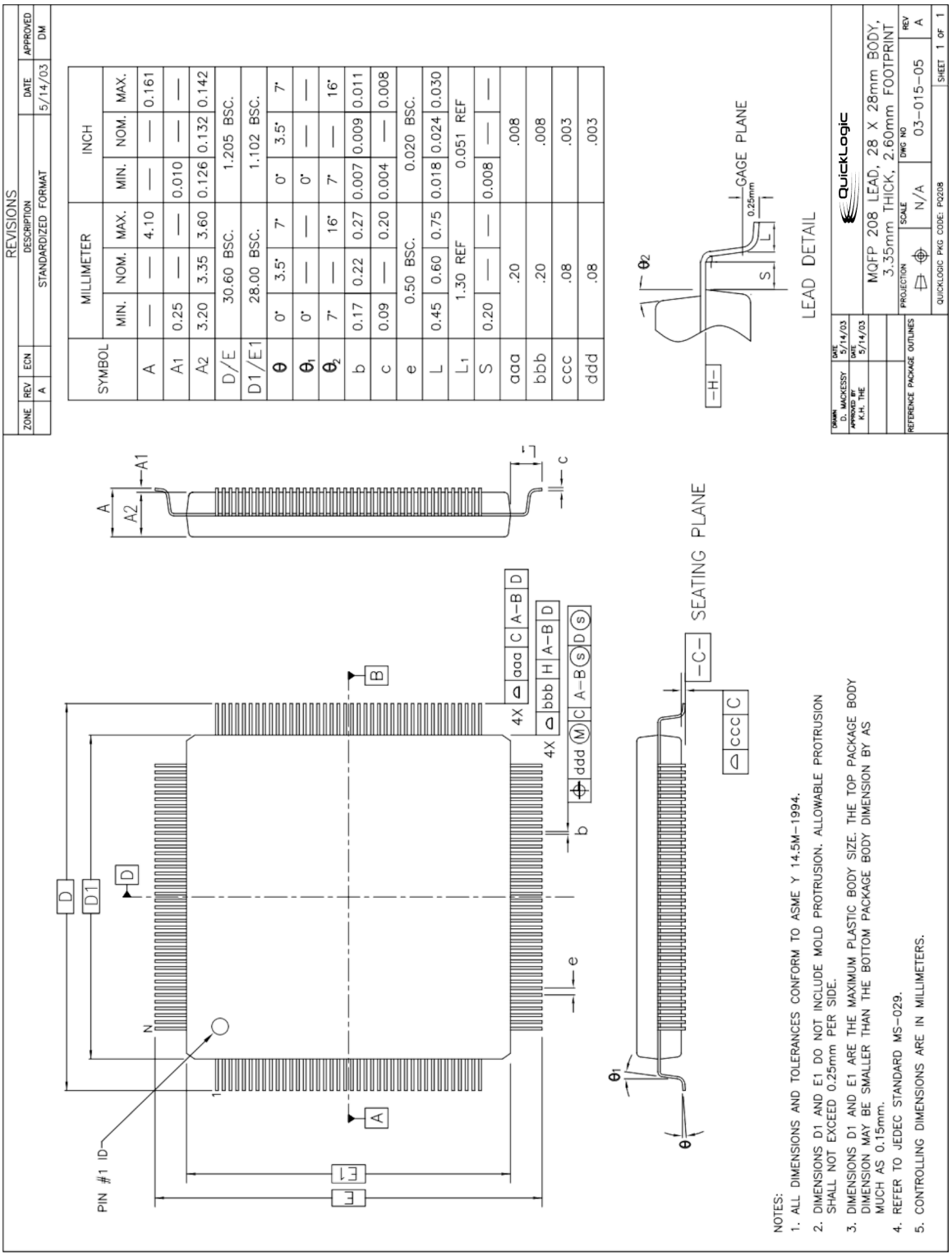
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE -H- LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DATUMS -A-B- AND -D- TO BE DETERMINED AT CENTERLINE BETWEEN LEADS WHERE LEADS EXIT PLASTIC BODY AT DATUM PLANE -H- .
4. TO BE DETERMINED AT SEATING PLANE -C- .
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254 MM ON D1 AND E1 DIMENSIONS.
6. 'N' IS THE TOTAL NUMBER OF TERMINALS.
7. THESE DIMENSIONS TO BE DETERMINED AT DATUM PLANE -H- .
8. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS, AND THE TOP OF THE PACKAGE WILL NOT OVERHANG THE BOTTOM OF THE PACKAGE.
9. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
10. CONTROLLING DIMENSION: MILLIMETER.
11. MAXIMUM ALLOWABLE DIE THICKNESS TO BE ASSEMBLED IN THIS PACKAGE FAMILY IS 0.38 MILLIMETERS.
12. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-136, VARIATION BT.

(JEDEC VARIATION)

SYMBOL	ALL DIMENSIONS IN MILLIMETERS			
	BT			NOTE
	MIN.	NOM.	MAX.	
A			1.60	
A_1	0.05	0.10	0.15	
A_2	1.35	1.40	1.45	
D		22.00 BSC.		4
D_1		20.00 BSC.		7,8
E		22.00 BSC.		4
E_1		20.00 BSC.		7,8
L	0.45	0.60	0.75	
M	0.14			
N		*128, 144		9
e		0.50 BSC.		
b	0.17	0.22	0.27	
b1	0.17	0.20	0.23	
ccc			0.08	
ddd			0.08	

* NOTE: THE 128 LEAD IS A COMPLIANT DEPOPULATION OF THE 144 LEAD MO-136 VARIATION BT.

208 PQFP Mechanical Drawing



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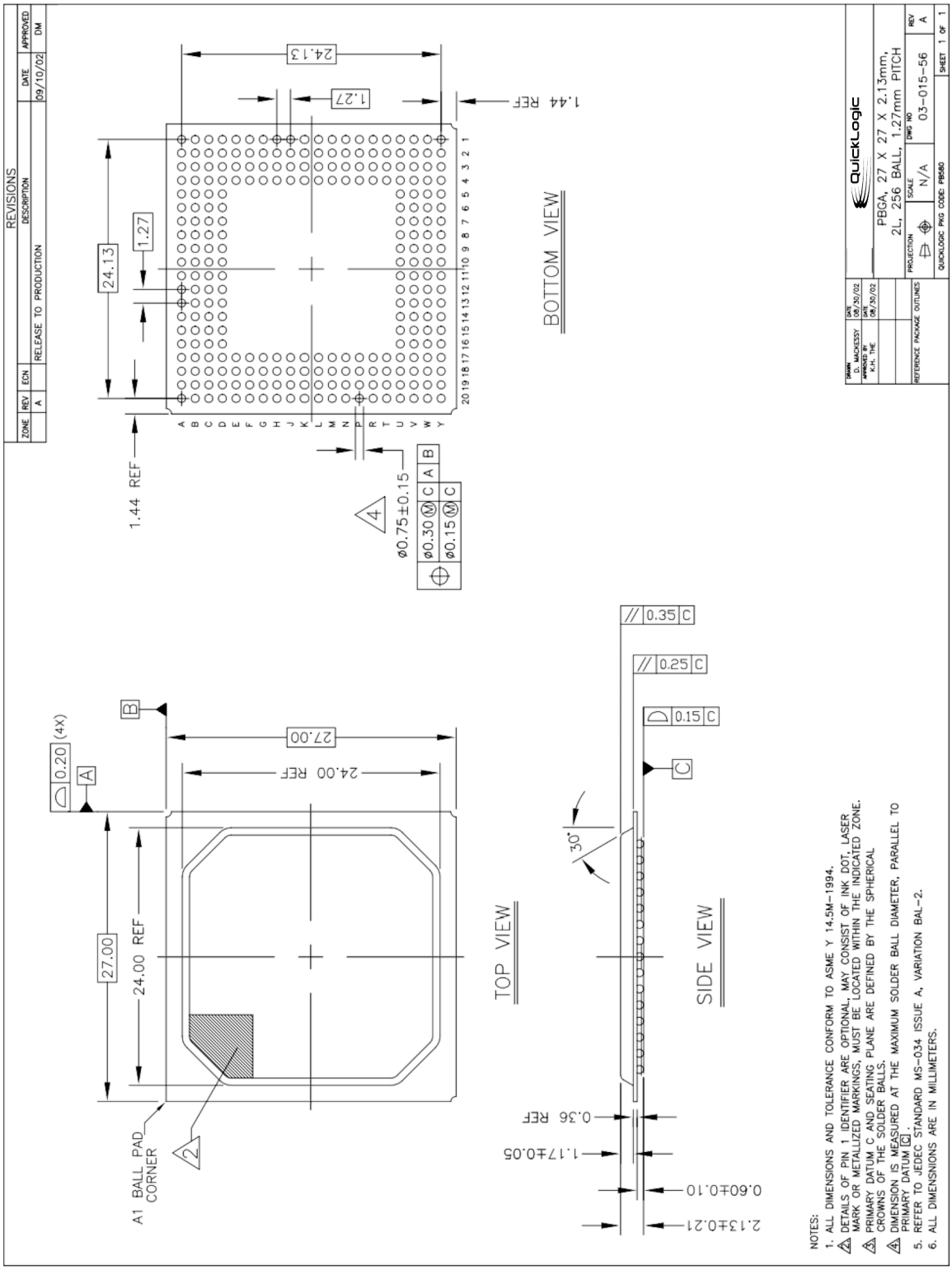
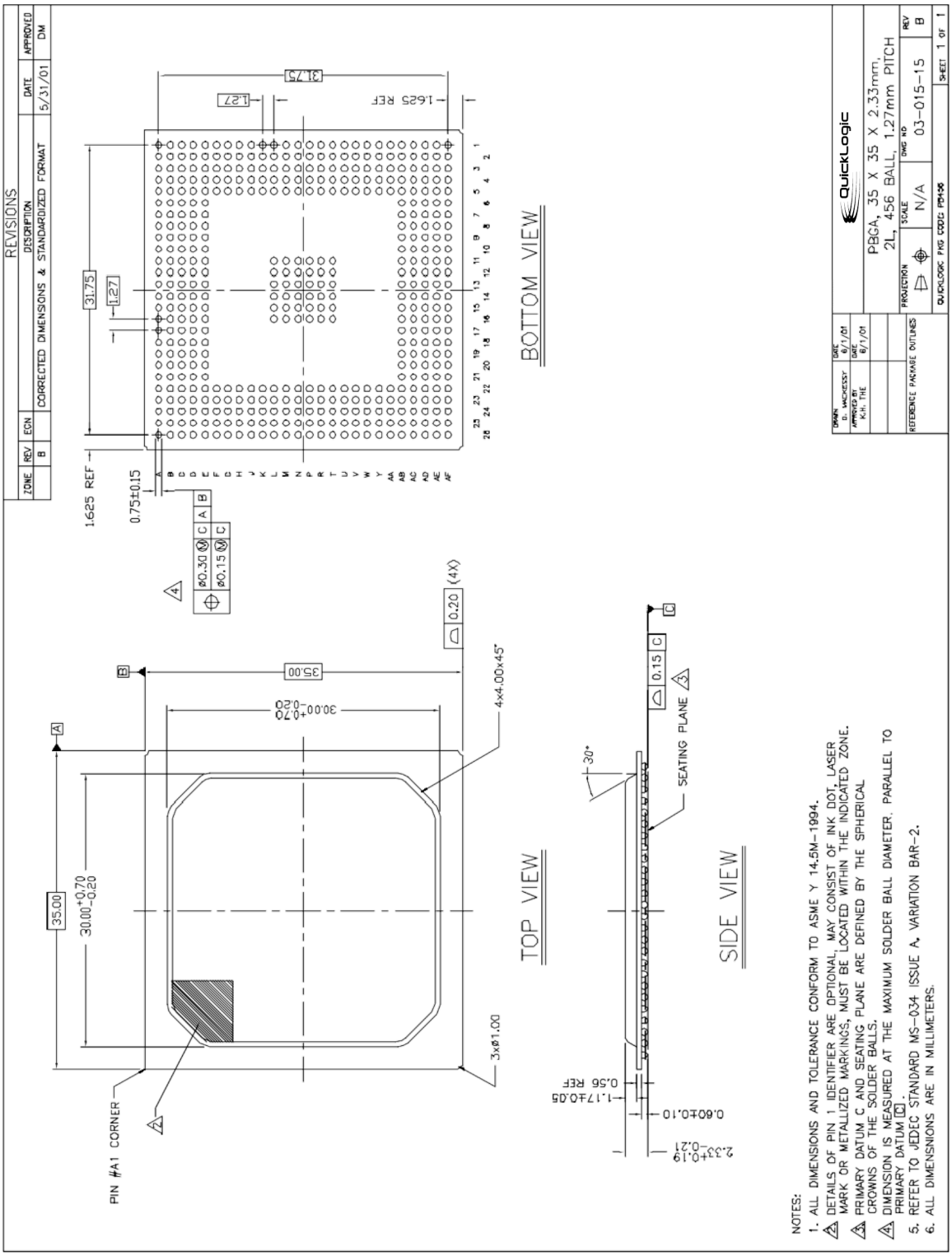
256 PBGA Mechanical Drawing



456 PBGA Mechanical Drawing



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Packaging Information

The QuickRAM product family packaging information is presented in **Table 26**.

Table 26: Packaging Options

Device Information	Device									
	QL4009		QL4016		QL4036		QL4058		QL4090	
	Pin	Pitch	Pin	Pitch	Pin	Pitch	Pin	Pitch	Pin	Pitch
Package Definitions[a]			56 QFN	0.5 mm	144 TQFP	0.5 mm	208 PQFP	0.5 mm	208 PQFP	0.5 mm
			100 TQFP	0.5 mm	208 PQFP	0.5 mm	456 PBGA	1.27 mm	456 PBGA	1.27 mm
	100 TQFP	0.5 mm	144 TQFP	0.5 mm	256 PBGA	1.27 mm				

a. QFN = Quad Flat No-lead
PQFP = Plastic Quad Flat Pack
PBGA = Plastic Ball Grid Array
TQFP = Thin Quad Flat Pack

Ordering Information

QL	4090	-1	PQN208	C
QuickLogic Device	Part Number: 4009, 4016, 4036, 4058, 4090	Speed Grade: 0 – Quick 1 – Fast 2 – Faster 3 – Fastest 4 – Wow**	Package Code: PUN56 = 56-pin QFN PFN100 = 100-pin TQFP PFN144 = 144-pin TQFP PQN208 = 208-pin PQFP PBN256 = 256-ball PBGA PBN456 = 456-ball PBGA	Operating Range: C = Commercial I = Industrial M = Military

** Contact QuickLogic regarding availability (see Contact Information).

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Revision History

Revision	Date	Originator and Comments
A through G	Not available	Not available
H	March 2002	Brian Faith and Andreea Rotaru
I	March 2005	Mehul Kochar and Kathleen Murchek
J	September 2005	Mehul Kochar and Kathleen Murchek Added lead free packaging information to Ordering Information section.
K	April 2006	Mehul Kochar and Kathleen Murchek Updated Max Gates row in Table 1: QuickRAM Product Family Members
L	May 2006	Kathleen Murchek Replaced pages 1 and 2 of 144-pin package drawing.
M	July 2007	Jason Lew and Kathleen Murchek Replaced 208-pin PQFP package drawing.
N	August 2026	Robert Dawson, removed PLCC,240 Pin QFP and CQFP packages, and added 56-Pin QFN package and drawing

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